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## DESCRIPTION

MP2935 is a high-efficiency, 4-phase, synchronous, buck-switching PWM controller with an SVID interface for high-performance Intel processors. The multi-phase PWM output signals can be configured for up to 4-phase operation with interleaved switching.

MP2935 adopts three-logic-level PWM outputs for enhanced noise immunity and flexible fault management. Depending on the power states set by SVID command, the multi-phase channel can switch between multiphase and single-phase operation. In addition, MP2935 supports programmable load-line resistance. As a result, the output voltage is always optimally positioned for a load transient.

The chip also provides accurate and reliable short-circuit protection with adjustable current limit threshold and a delayed VR_RDY output that is masked during on-the-fly output voltage changes to eliminate false triggering. MP2935 performance is specified over the junction temperature range of -10°C to 125°C. The chip is available in 40-lead QFN package.

## FEATURES

- VR12.5 compliant
- Multi-Phase Operation at up to 2MHz per Phase
- Tri-State PWM Outputs for Driving MPS Intelli-Phase™ Devices
- Power-Saving Modes Maximize Efficiency During Light Load and Deeper-Sleep Operation
- Active Current Balancing between Output Phases
- Independent Current Limit and Load Line Setting Inputs for Additional Design Flexibility
- 8-bit Digitally Programmable 0V to 3.04V Output through Serial VID Interface
- Overload and Short-Circuit Protection with Latch-Off Delay
- Output Current Monitor
- Fault Latch Output
- Regulator Temperature Monitor
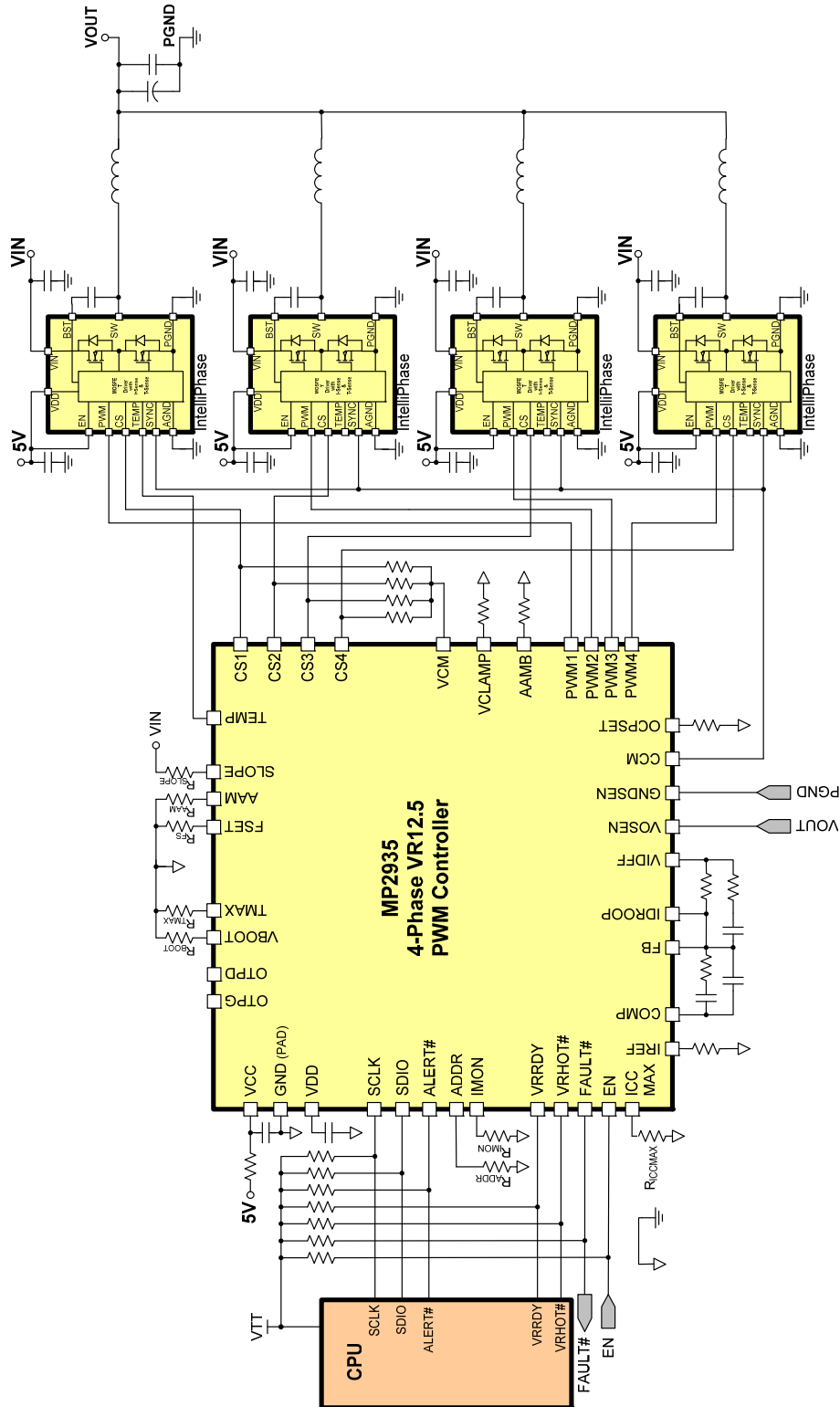- Available in a 6mmx6mm 40-lead QFN package

## APPLICATIONS

- Power supplies for next-generation Intel® processors

# TYPICAL APPLICATION CIRCUIT

# ORDERING INFORMATION

| Part Number* | Package | Top Marking | Junction Temperature ($T_J$) |
|---|---|---|---|
| MP2935DQK | 6x6mm QFN40 | MP2935 | -40°C to +125°C |
| MP2935ADQK | 6x6mm QFN40 | MP2935A | -40°C to +125°C |

\* For Tape & Reel, add suffix –Z (e.g. MP2935DQK–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP2935DQK–LF–Z)

# PACKAGE REFERENCE

**TOP VIEW**
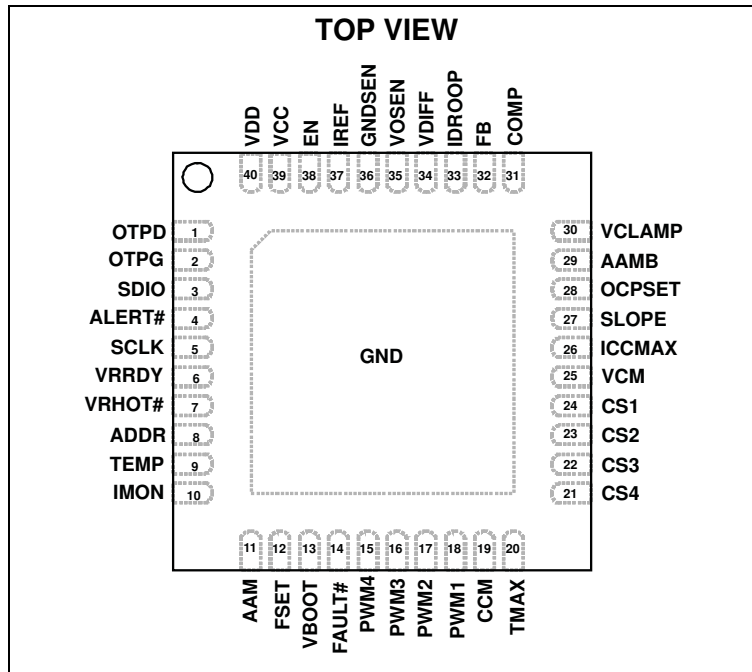


# ABSOLUTE MAXIMUM RATINGS [1]

VCC ..............................................0.3V to +6.5V
VDD ..............................................−0.3V to +4.0V
GNDSEN .....................................−0.3V to +0.3V
SLOPE ........................................−0.3V to +26V
All Other Pins ....................−0.3V to (VCC+0.3V)
Continuous Power Dissipation ($T_A$ = +25°C) [2]
................................................................. 3.9W
Junction Temperature..............................150°C
Lead Temperature ..................................260°C
Storage Temperature.............. −65°C to +150°C

## *Recommended Operating Conditions* [3]

VCC...........................................4.5V to 5.5V
Operating Junction Temp........ −40°C to +125°C

## *Thermal Resistance* [4]    $\theta_{JA}$    $\theta_{JC}$

6x6 QFN40............................. 32 .......8      °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$(MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$(MAX) = ($T_J$(MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

# ELECTRICAL CHARACTERISTICS

**VCC = 5 V, GNDSEN = GND, EN = VCC, VID = 0.50 V to 3.04 V, Current going into pin is positive.**
**$T_A$ = -10°C to +100°C, unless otherwise noted.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **VOLTAGE ERROR AMPLIFIER** | | | | | | |
| Error Amplifier Output Voltage Range[5] | $V_{COMP}$ | | 0.75 | | 4.6 | V |
| DC output Accuracy | $V_{OUT}$ | $t_A$ = 25°C. No load, closed-loop, measured at VOSEN pin to GNDSEN pin. Active mode range. VID=1.50V to 3.04V | -0.5 | | +0.5 | % |
| | | No load, closed-loop, measured at VOSEN pin to GNDSEN pin. Active mode range. VID=1.50V to 3.04V | -1 | | +1 | % |
| | | $t_A$ = 25°C. No load, closed-loop, measured at VOSEN pin to GNDSEN pin. Active mode range. VID=1.00V to 1.50V | -8 | | +8 | mV |
| | | No load, closed-loop, measured at VOSEN pin to GNDSEN pin. Active mode range. VID=1.00V to 1.50V | -15 | | +15 | mV |
| | | $t_A$ = 25°C. No load, closed-loop, measured at VOSEN pin to GNDSEN pin. Active mode range. VID=0.500V to 1.000V | -10 | | +10 | mV |
| | | No load, closed-loop, measured at VOSEN pin to GNDSEN pin. Active mode range. VID=0.500V to 1.000V | -15 | | +15 | mV |
| Line Regulation | $\Delta V_{FB}$ | $V_{CC}$ = 4.75 V to 5.25 V | | 0.3 | | % |
| Input Bias Current | $I_{FB}$ | | −1 | | +1 | μA |
| Output Source Current | $I_{COMP}$ | FB forced to ($V_{VID}$ − 3%), no droop | | -3 | | mA |
| Output Sink Current | $I_{COMP}$ | FB forced to ($V_{VID}$ + 3%), no droop | | +3 | | mA |
| Open Loop Gain[5] | | | | 80 | | dB |
| Unity Gain Bandwidth[5] | $GBW_{(ERR)}$ | COMP = FB | | 20 | | MHz |
| Slew Rate[5] | | $C_{COMP}$ = 10 pF | | 25 | | V/μs |
| **REMOTE SENSE AMPLIFIER** | | | | | | |
| Bandwidth[5] | $GBW_{(RSA)}$ | | | 20 | | MHz |
| GNDSEN Current | $I_{GNDSEN}$ | GNDSEN=0.3V | | 10 | 400 | μA |
| VOSEN Current | $I_{VOSEN}$ | VOSEN=1V | | 15 | 50 | μA |
| **OSCILLATOR** | | | | | | |
| FSET Voltage | $V_{FSET}$ | $R_{FSET}$ = 64.9kΩ to GND | 0.9 | 1.0 | 1.1 | V |
| Frequency Setting | $f_{SW}$ | $t_A$ = 25°C, $R_{FSET}$ = 64.9kΩ, 4-phase configuration | 540 | 600 | 660 | kHz |
| SLOPE Input Current Range [5] | $I_{SLP}$ | In normal mode | 0 | | 800 | μA |
| | | In shutdown, or in UVLO, SLOPE = 12 V | −1 | | +1 | μA |

## ELECTRICAL CHARACTERISTICS *(continued)*

**VCC = 5 V, GNDSEN = GND, EN = VCC, VID = 0.50 V to 3.04 V, Current going into pin is positive. $T_A$ = -10°C to +100°C, unless otherwise noted.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CURRENT-SENSE AND OVERCURRENT PROTRECTION** | | | | | | |
| Current Limit Level | $I_{VCM\_OC}$ | $R_{OCPSET}$=80.6kΩ, sink current from VCM pin | | 1.27 | | mA |
| Droop Current | $I_{DRP}$ | $I_{VCM}$= -400µA | -24 | -25 | -26 | µA |
| | | $I_{VCM}$= +400µA | 24 | 25 | 26 | µA |
| **CURRENT BALANCE AMPLIFIER** | | | | | | |
| Common Mode Range[5] | $V_{CS\_CM}$ | | 1.0 | | 3.5 | V |
| Input Current | $I_{CS}$ | CSx=4V | | | 1 | µA |
| Masked Off-Time[5] | $t_{OFFMSKD}$ | Measured from PWM turn-off | | 350 | | ns |
| **SYSTEM INTERFACE CONTROL INPUTS** | | | | | | |
| **EN** | | | | | | |
| EN Low Threshold Voltage | $VIL_{(EN)}$ | | | | 0.4 | V |
| EN High Threshold Voltage | $VIH_{(EN)}$ | | 0.8 | | | V |
| EN High Threshold Hysteresis Voltage | $VIH_{(EN)}$ | | | 100 | | mV |
| Enable High Leakage | $IIH_{(EN)}$ | EN=1.1V | | | 2 | µA |
| Enable Delay | $T_3$ | VCC≥UVLO, Vboot is not 0V, EN high to Vout ramping (see Figure 13) | | 2 | 5 | ms |
| **THERMAL THROTTLING CONTROL** | | | | | | |
| $V_{TEMP}$ ADC | | Register 17h=64h (100°C) | | 0.9 | | V |
| VRHOT# Low Output Impedance | | $I_{VRHOT\#}$ = 20mA, $T_A$=25°C | | 8 | 10 | Ω |
| VRHOT# High Leakage Current | | | -1 | | 1 | µA |
| **IMON OUTPUT** | | | | | | |
| IMON Current | $I_{MON}$ | $I_{VCM}$= +400µA | 24 | 25 | 26 | µA |
| IMON Clamp Voltage | $V_{IMONMAX}$ | IMON = Float, $I_{VCM}$ = 400µA | | 1.3 | | V |
| IMON ADC | | Register 15h=C8h | | 1 | | V |
| IMON ADC | | Register 15h=64h | | 0.5 | | V |
| **VRRDY COMPARATOR** | | | | | | |
| Under-Voltage Threshold | $VDIFF_{(UV)}$ | Relative to nominal DAC voltage | | −300 | | mV |
| Over Voltage Threshold | $VDIFF_{(OV)}$ | Relative to nominal DAC voltage | | 400 | | mV |
| | | Absolute voltage | | 3.30 | | V |
| Output Low Voltage | $V_{VRRDY}$ (L) | $I_{VRRDY}$(SINK) = 4mA | | 60 | 250 | mV |
| Output High Leakage | $I_{VRRDY}$ | $V_{VRRDY}$ = 3.3V | | | 1 | µA |
| Reverse Voltage Detection Threshold[5] | $V_{OSEN}$ (RV) | Relative to GNDSEN, VDIFF falling | | −300 | | mV |
| | | Relative to GNDSEN, VDIFF rising | | −100 | | mV |

# ELECTRICAL CHARACTERISTICS *(continued)*

**VCC = 5 V, GNDSEN = GND, EN = VCC, VID = 0.50 V to 3.04 V, Current going into pin is positive. $T_A$ = -10°C to +100°C, unless otherwise noted.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CCM OUTPUT** | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 400µA | | 10 | 200 | mV |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 400µA | 4.8 | 5 | | V |
| **PWM OUTPUTS** | | | | | | |
| Output Low Voltage | VOL (PWM) | $I_{PWM(SINK)}$ = 400µA | | 10 | 200 | mV |
| Output High Voltage[5] | VOH (PWM) | $I_{PWM(SOURCE)}$ = 400µA | 4.8 | 5 | | V |
| PWM Tri-State Leakage | | PWM = 2.5V | -1 | | 1 | µA |
| **SUPPLY** | | | | | | |
| VCC UVLO Threshold Voltage | $VCC_{UVLO}$ | VCC is rising | | 4.1 | 4.45 | V |
| UVLO Hysteresis | | | | 200 | | mV |
| Supply Current | $I_{VCC}$ | EN=high. Both SVID bus and internal ID bus are idle. No load condition. 4-phase configuration. PWMs not switching. | | 8 | 16 | mA |
| | | EN = 0V | | 50 | 250 | µA |
| **VDD REGULATOR** | | | | | | |
| VDD Regulator Output Voltage | VDD | | | 3.2 | | V |
| **SVID Interface (SCLK, SDIO, ALERT#)[5]** | | | | | | |
| Leakage current | IL | Pull-up voltage: 0V to 1.1V | -10 | | 10 | µA |
| Pin Capacitance[5] | $C_{PIN}$ | | | | 5 | pF |
| Buffer ON Resistance[5] | $R_{ON}$ | | 4 | 8 | 13 | Ω |
| VR Clock to Data Delay[5] | | | 4 | | 8.3 | ns |
| Setup Time[5] | | | | 7 | | ns |
| Hold Time[5] | | | | 14 | | ns |

## ELECTRICAL CHARACTERISTICS *(continued)*

**VCC = 5 V, GNDSEN = GND, EN = VCC, VID = 0.50 V to 3.04 V, Current going into pin is positive.**
**$T_A$ = -10°C to +100°C, unless otherwise noted.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **ADC** | | | | | | |
| Voltage Range | | Reads FF. | | 1.28 | | V |
| ADC Resolution | | | | 5 | | mV |
| ADC Sampling Rate[5] | | | | 3000 | | Hz |
| DNL[5] | | | | | 1 | LSB |
| Conversion Time[5] | | | | 30 | | μs |
| **DAC Slew rate (MP2935)** | | | | | | |
| Soft-Start Slew Rate | | | | 2.5 | | mV/μs |
| SetVID_Slow Slew Rate | | | | 2.5 | | mV/μs |
| SetVID_Fast Slew Rate | | | | 10 | | mV/μs |
| **DAC Slew rate (MP2935A)** | | | | | | |
| Soft-Start Slew Rate | | | | 5 | | mV/μs |
| SetVID_Slow Slew Rate | | | | 5 | | mV/μs |
| SetVID_Fast Slew Rate | | | | 20 | | mV/μs |
| **DAC** | | | | | | |
| DAC resolution | | | | 8 | | Bits |
| LSB | | | | 10 | | mV |
| DNL | | | | ±1 | | LSB |
| INL | | | | ±1 | | LSB |
| Tolerance | | | -1 | | 1 | mV |
| **1/2/3/4 Phase Detection** | | | | | | |
| PWM Sink Current | | | | 100 | | μA |
| PWM Detection Threshold Voltage | | | 2 | 2.5 | 3.2 | V |
| Phase Detect Timer[5] | | | | 50 | | μs |

**Notes**:
5) Guaranteed by design or characterization data, not tested in production.

## PIN DEFINITION

| Pin # | Name | I/O | Description |
|-------|------|-----|-------------|
| 1 | OTPD | I | Factory OTP programming only. Connect to VCC for normal operation. |
| 2 | OTPG | I | Factory OTP programming only. Connect to GND for normal operation. |
| 3 | SDIO | I/O | Data Signal between CPU and Serial VID Controller. |
| 4 | ALERT# | O | Alert Signal from VID Controller to CPU. |
| 5 | SCLK | I | Source Synchronous Clock from CPU. |
| 6 | VRRDY | O | VR Ready Output. Open drain output signal. |
| 7 | VRHOT# | O | Voltage Regulator Thermal Throttling Logic Output. Actively pulls low if temperature at the monitoring point connected to TEMP exceeds the programmed VRHOT# temperature threshold. |
| 8 | ADDR | I | SVID Address setting pin. Refer to Table 6 for address assignment. |
| 9 | TEMP | I/O | Analog Temperature Signal Input. |
| 10 | IMON | O | Analog Total Load Current Signal. Sources a current proportional to the sensed total load current. Connect a resistor from IMON to GND to program the gain. |
| 11 | AAM | I | Advanced Asynchronous Mode (AAM) Timing Control Input. A resistor between this pin to ground sets the AAM mode turn-on threshold voltage. |
| 12 | FSET | I | Multiphase Frequency-Setting Input. A resistor connected between FSET and GND sets the oscillator frequency. The phase switching frequency will be divided by number of the operating phase. |
| 13 | VBOOT | I/O | $V_{BOOT}$ Voltage Set. Refer to Table 3 for VBOOT voltage assignment. |
| 14 | FAULT# | O | VR Fault#. Asserts low to notify the platform of a VR fault condition. |
| 15 | PWM4 | O | Tri-State Logic-Level PWM Outputs. Connecting the PWM2 and/or PWM3 and/or PWM4 outputs to VCC turns off that phase, allowing MP2935 to change the number of operating phases. The operating phase number is decided when the part is enable. The number of operating phase cannot be changed on-the-fly. |
| 16 | PWM3 | O | |
| 17 | PWM2 | O | |
| 18 | PWM1 | O | |
| 19 | CCM | O | Forced CCM Operation Enable. CCM stays high in Power States 00 and 01. Actively pulls low when in Power States 02 and 03 to enable DCM operation of the power stage. Connect it to the SYNC pin of Intelli-Phases™. |
| 20 | TMAX | I | Max. Temp. Set. Connect a resistor from TMAX to GND to set the maximum temperature. |
| 21 | CS4 | I | Current Balance Inputs. Measures the current level in each phase. Float CS pins of unused phases. |
| 22 | CS3 | I | |
| 23 | CS2 | I | |
| 24 | CS1 | I | |
| 25 | VCM | O | Buffered 2.5V reference. |
| 26 | ICCMAX | I | ICCMAX setting. Set the pin voltage to program the desired ICCMAX level. |

## PIN DEFINITION *(continued)*

| Pin # | Name | I/O | Description |
|-------|------|-----|-------------|
| 27 | SLOPE | I | PWM Slope Current Input. Connect a 100KΩ resistor from VIN (system's 12V input voltage) to this pin to set the internal slope for PWM comparator. |
| 28 | OCPSET | I | Total Current Limit Setting. |
| 29 | AAMB | I | Combine with AAM pin, this pin sets the AAM mode threshold voltage. |
| 30 | VCLAMP | I | Connect a resistor to ground to set the per phase current limit. |
| 31 | COMP | I/O | Error Amplifier Output. |
| 32 | FB | I | Inverting Input of Error Amplifier. |
| 33 | IDROOP | O | Droop Current Output. Sources current that is proportional to the sensed output current. |
| 34 | VDIFF | O | Differential Amplifier Output. |
| 35 | VOSEN | I | Remote Core Voltage Sense Input. Connect to VCCSENSE at microprocessor die. |
| 36 | GNDSEN | I | Remote Voltage Sensing Return. Connect to ground at microprocessor die. |
| 37 | IREF | I | Internal Bias Current Set. Connect an 80.6kΩ resistor from IREF to GND. |
| 38 | EN | I | Chip Enable. |
| 39 | VCC | I | 5V supply voltage for the controller. Need a 1µF capacitor for decoupling. |
| 40 | VDD | O | 3.3V LDO output for internal digital circuit only. Need a 1µF capacitor for decoupling.  Do not connect to any other load. |
| PAD | GND | I/O | Ground. |

## TYPICAL PERFORMANCE CHARACTERISTICS

**Performance waveforms are tested on the evaluation board of the Design Example section.**
$V_{IN}$ = 12V, $V_{CC}$ = 5V, $V_{OUT}$ = 1.85V, $I_{OUT}$ = 0A, 600kHz, unless otherwise noted.
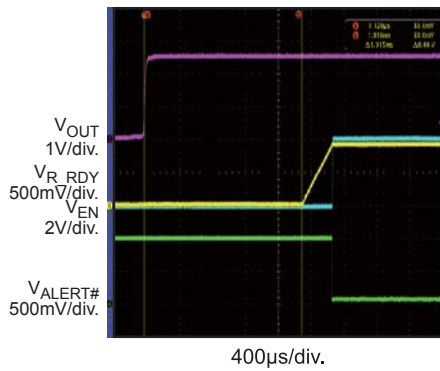
| Enable Startup | Enable Shutdown | Power State 1 |
|---|---|---|



400μs/div.



1μs/div.



1μs/div.
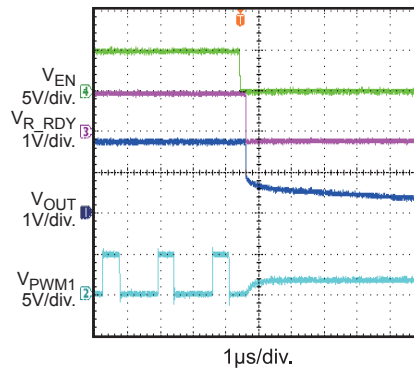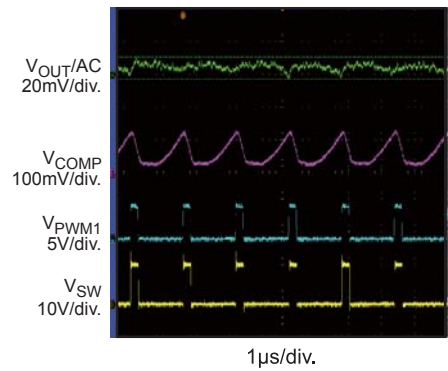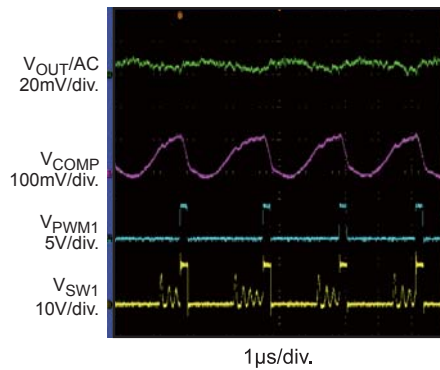
| Power State 2/3 | Phase Shift | Under Voltage Protection |
|---|---|---|
| | | Forced 1.55V to $V_{DIFF}$ |
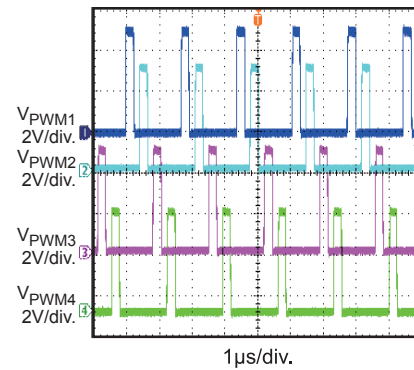


1μs/div.



1μs/div.



200μs/div.
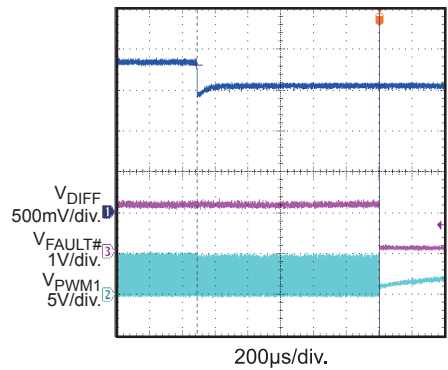
| Over Voltage Protection #1 | Over Voltage Protection #2 | Over Current Protection |
|---|---|---|
| Forced 2.25V to $V_{DIFF}$ | Forced 3.4V to $V_{DIFF}$ during VID Ramping | |
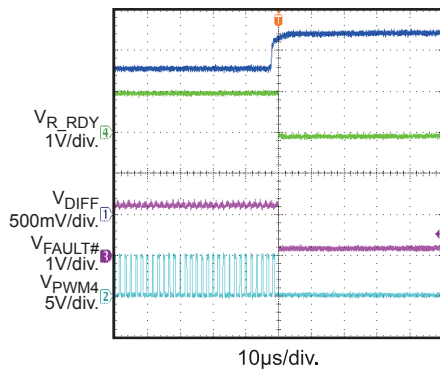


10μs/div.



20μs/div.



2μs/div.

**mPS**
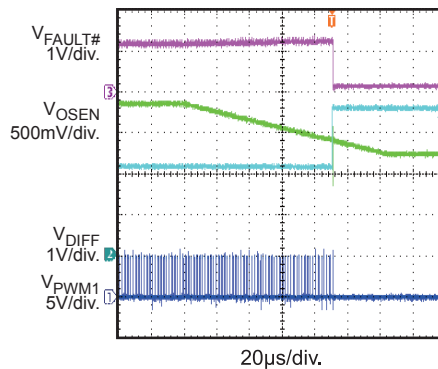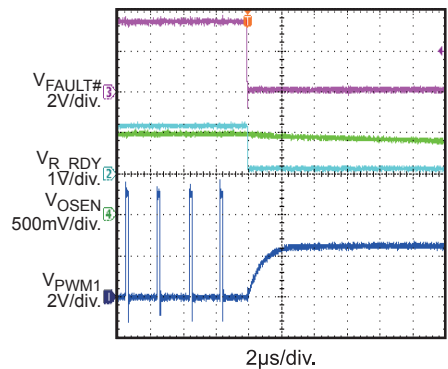
# FUNCTIONAL BLOCK DIAGRAM

VDD — 3.3V LDO — VCC

EN — UVLO SHUTDOWN BIAS

GND

BANDGAP

VRHOT# — VR_HOT# CONTROL

TEMP

FB — E/A
VID — +

COMP

GNDSEN — −
VOSEN — +
VDIFF

CCM — MODE CONTROL — 1-Ph

ADDR — 4-bits ADC — 4

SCLK
SDIO — Serial Data Link, Registers, And OTP Control
ALERT#
OTPD
OTPG

4MHz ID Clock

256 8-bits Registers

DAC — VID

8-bits ADC — 8-Channel MUX

IMON
TEMP
VDIFF
(TBD)
(TBD)
(TBD)
(TBD)
(TBD)

24kHz Clock

VRSET
DVID
VRRDY0
DECAY

AAM
FSET
SLOPE

OSCILLATOR

Clock Divider

CURRENT BALANCE

VOSEN — RVP
−300mV

OVP2 — 3.4V
VID+400mV — OVP1
VDIFF
VID−300mV — UVP

FAULT
OV  RV
OC  DCY

DECAY

SET/ EN

1-/2-/3-/4-PHASE DRIVER LOGIC

RESET
RESET
RESET
RESET

FAULT  1-Ph

PWM1
PWM2
PWM3
PWM4

CS1
CS2
CS3
CS4

OCPSET

CURRENT SENSE

VCLAMP
AAMB

IMON
IDROOP
IREF

2.5V — VCM

FAULT
DECAY
DVID
VRRDY0

VR_READY MONITOR & DELAY, 2ms — VRRDY

VID +10mV
V_FB
VID −10mV

VR SETTLED COMPARATOR — VRSET

FAULT#

FAULT

TMAX
ICCMAX

## OPERATION

MP2935 is a 4-phase VR12.5-compliant controller for Intel microprocessors. It is a multiphase controller for up to 4-phase operation and is capable for multi-mode PWM/advanced asynchronous mode (AAM) operation to maximize the efficiency over the load range. It includes blocks for a precision DAC, remote voltage-sense amplifiers, an error amplifier, a ramp generator with input voltage feed-forward, a PWM comparator, AAM control, load-line set, a VR-ready (VRRDY) monitor, a temperature monitor and serial VID (SVID) registers. It also includes dynamic-phase current balancing and phase shedding. Protection features include under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP) and reverse voltage protection (RVP).

### PWM Operation

MP2935 uses constant-switching–frequency current mode control and trailing-edge PWM operation with injected valley current signals. The PWM ramp of each phase combines with the sensed valley current to determine phase-current balance. Figure 1 shows the operation principles. The phase clock turns the PWM on. When the combined ramp voltage hits $V_{COMP}$ voltage the PWM turns off. The phase shift is applied between operating phases to minimize the input and output current ripple.

In general, the controller needs to wait for the next clock during a load step transient to turn on the PWM to support the load current. The waiting time causes the extra output voltage to drop. To maximize the current support to reduce the output voltage drop during the transient load, MP2935 employs FAST-PWM$^{TM}$ mode to respond immediately. During the load-step transient, the output voltage drop causes $V_{COMP}$ to rise. When $V_{COMP}$ rise fast enough to trigger the FAST-PWM threshold, the controller overrides the phase clock and turns on all PWMs without phase shifts. The PWM OFF of each phase is the same as for normal operation when the combined ramp hits $V_{COMP}$ voltage. This FAST-PWM mode maximizes the regulator's di/dt slew rate to support the output load transient step and minimize the $V_{OUT}$ drop.

When the power state is not PS0, the chip operates in single phase with AAM mode to maximize the efficiency in light load condition. A detailed description of AAM mode operation is described in "AAM Control Operation and Diode Emulation."
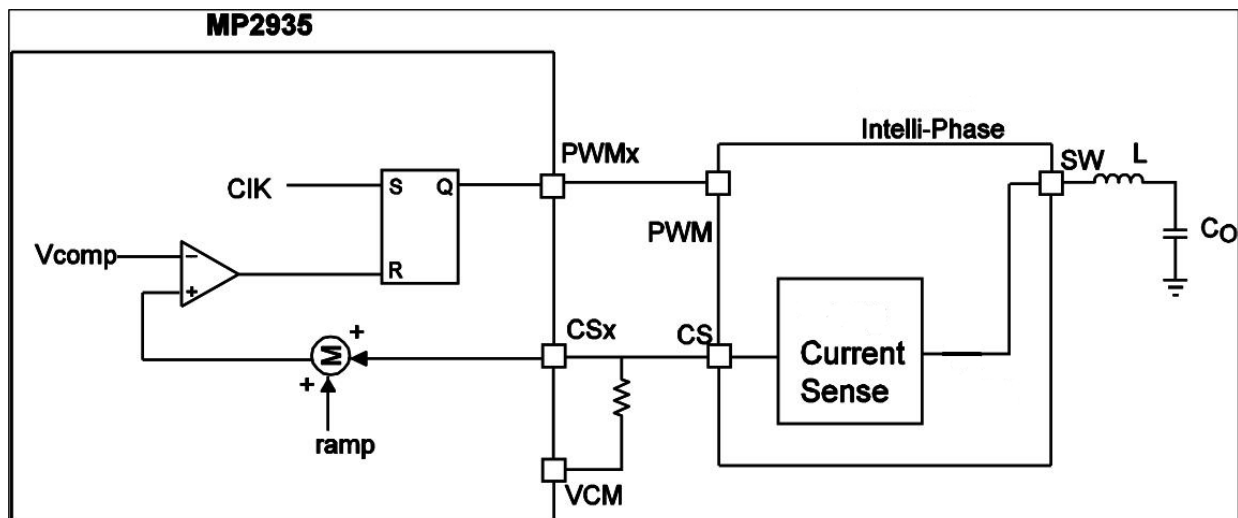


**Figure 1: Block Diagram of PWM Operation**

**PWM Operation and Power States**
The user can select the total number of operating phases for MP2935, as described in "Switching Frequency and the Number of Operating Phases." Based on the power states, the actual operating phase dynamically switches between full phases or single phase to optimize the power conversion efficiency at heavy and light CPU loads.

In PS0, MP2935 runs in full-phase PWM mode. While in light-load mode, PS1 to PS3, only Phase 1 is in operation to maximize power conversion efficiency. During the dynamic VID transition issued by SVID commands of either SetVID_Fast or SetVID_Slow, the power state changes to PS0 by default and runs in full-phase PWM mode.

In addition to changing the number of phases, the operation mode can change dynamically. In PS0 mode, MP2935 runs in multiphase PWM mode with switching frequency controlled by the master clock. In other power states, MP2935 switches to AAM mode where the switching frequency is no longer controlled by the master clock, but by the ripple voltage on the COMP pin. Thus, the switch frequency varies with the load current, resulting in maximum power conversion efficiency in low power states.

In PS2 and PS3, diode emulation mode is enabled to maximize the efficiency at light load condition.

The VR will switch back to AAM mode if the over current alarm is clear before latch-off.

Table 1 summarizes the dynamically changes to phase number and operation modes based on the power state register set through SVID commands.

The power states are listed in order of power savings:

• PS0 represents full power or Active mode
• PS1 is used in Active Mode or Idle Mode and represents a low current state, similar to PSI# definition in VR11.1 or IMVP6.5; it typically has a load < 20A. MP2935 runs in single phase (PWM1 only) AAM/continuous current modulation (CCM) mode.

• PS2 is used in Sleep Mode and it represents a lower current state than PS1; it typically has a load < 5A. MP2935 runs in single phase (PWM1 only) AAM with diode emulation enabled.
• PS3 (Mode[1,0]= "11") is ultra-low current mode, lower than PS2; it typically has a load < 1A. MP2935 runs in single phase (PWM1 only) AAM with diode emulation enabled.

**Table 1: Phase Number and Operation Modes**

| Power State | Operating Phases | CCM | PWM/AAM |
|---|---|---|---|
| 0 | Full phases | 1 | PWM |
| 1 | 1 | 1 | AAM |
| 2 | 1 | 0 | AAM |
| 3 | 1 | 0 | AAM |

**AAM Control Operation and Diode Emulation**

With the exception of PS0, all other power states enable AAM mode and run in single phase operation. Figure 2 shows typical AAM mode operation where switching frequency is no longer controlled by the master clock, but by the ripple voltage on the COMP pin.

PWM1 is set high when $V_{COMP}$ reaches the AAM threshold voltage which is set by two resistors, from AAM pin to GND and from AAMB pin to GND.

AAM Threshold Voltage
$$= \frac{15400 \times V_{OUT}}{R_{AAM}} + I_{MON} \times R_{AAMB} + V_{COMMON}$$

$$R_{AAMB} = \frac{16 \times R_{CS}}{N}$$

$$R_{AAM} = \frac{15400 \times V_{OUT}}{V_{AAM\_Fraction}}$$

$$V_{AAM\_Fraction} = \frac{V_{OUT}}{F_{SW} \times 3.424 \times 10^{-6}} - 0.5 \times I_{L\_PK-PK} \times R_{CS} \times 10 \times 10^{-6}$$

$V_{COMMON}$ is about 1V. $V_{AAM\_Fraction}$ is part of the AAM threshold voltage. N is the number of

active phase during PS0. $I_{L\_PK-PK}$ is the peak to peak inductor current.

$$I_{L\_PK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times L \times F_{SW}}$$

Whenever PWM is high, $V_{RAMP}$ ramps up from 1V with a slew rate programmed by the current flowing into the SLOPE pin. When $V_{RAMP}$ reaches $V_{COMP}$, PWM resets to low.

The CCM pin is tied to the SYNC pin of the Intelli-Phase[TM]. When the CCM pin is low, it enables diode emulation mode. In diode

emulation mode the low side MOSFET turns OFF once the inductor current reverses to keep the inductor current at 0A until the next PWM ON pulse.

In both PS0 and PS1, the CCM pin is high so the controller operates in CCM mode, which allows for negative inductor current.

In PS2 and PS3, the CCM pin is low to enable diode emulation mode on the Intelli-Phase[TM], allowing Diode Emulation mode operation.
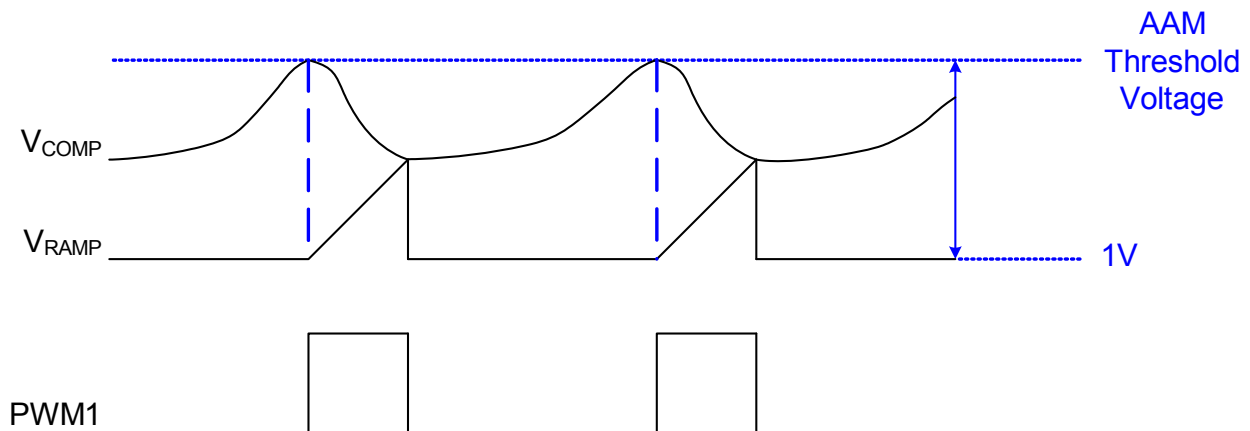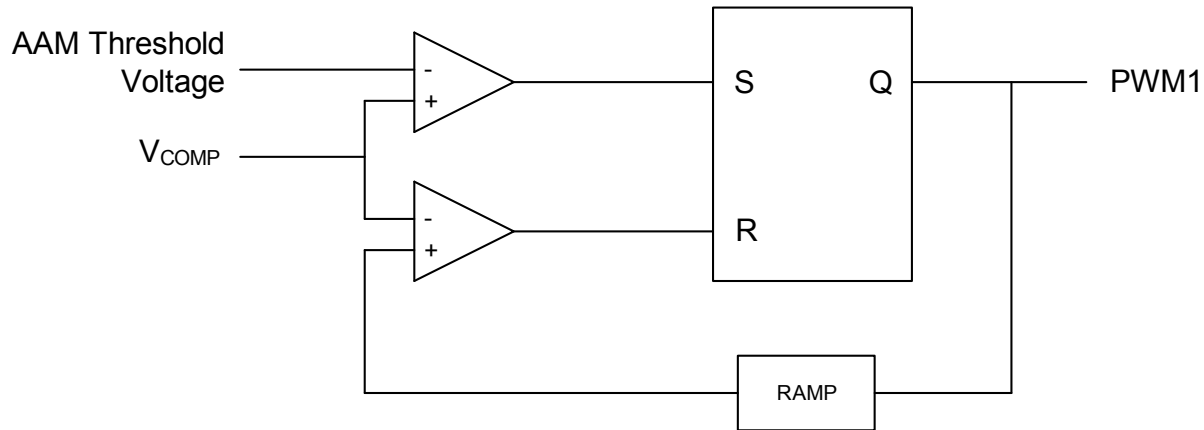


**Figure 2: Block Diagram of AAM Operation and Typical Waveforms**

## Switching Frequency and the Number of Operating Phases

In normal operation in the PS0 power state, an external resistor connected from the FSET pin to ground determines the clock frequency. To determine the switching frequency per phase, divide the clock by N, the number of phases, in use. If phase 4 is disabled by pulling up PWM4 to VCC, then divide the master clock by 3 for the frequency of the remaining phases. If both PWM3 and PWM4 are pulled up to VCC, then divide the master clock by 2 for the frequency of the remaining phases. If PWM2, PWM3 and PWM4 are pulled up to VCC, then the switching frequency of phase 1 equals the master clock frequency. If all phases are in use, then divide the master clock by 4.

$$R_{FSET} = 340000 \times (F_{SW} \times N)^{-1.106}$$

In single-phase AAM mode, the switching frequency is almost constant, until it enters DCM mode then the frequency decrease proportionally with load current.

## Current Sensing and IMON

MP2935's works seamlessly with the Intelli-Phase$^{TM}$ family to accurately sense output current to monitor the total output current to support Adaptive Voltage Positioning (AVP) and current limit detection. Simply direct the total sensed phase current from all of the Intelli-Phases's$^{TM}$ CS pins to VCM pin. When utilizing the Intelli-Phase's$^{TM}$ accurate current sense output, it eliminates sensing error due to inductor DCR variation and removes design effort on DCR thermal compensation. This simple configuration is shown in Figure 3.
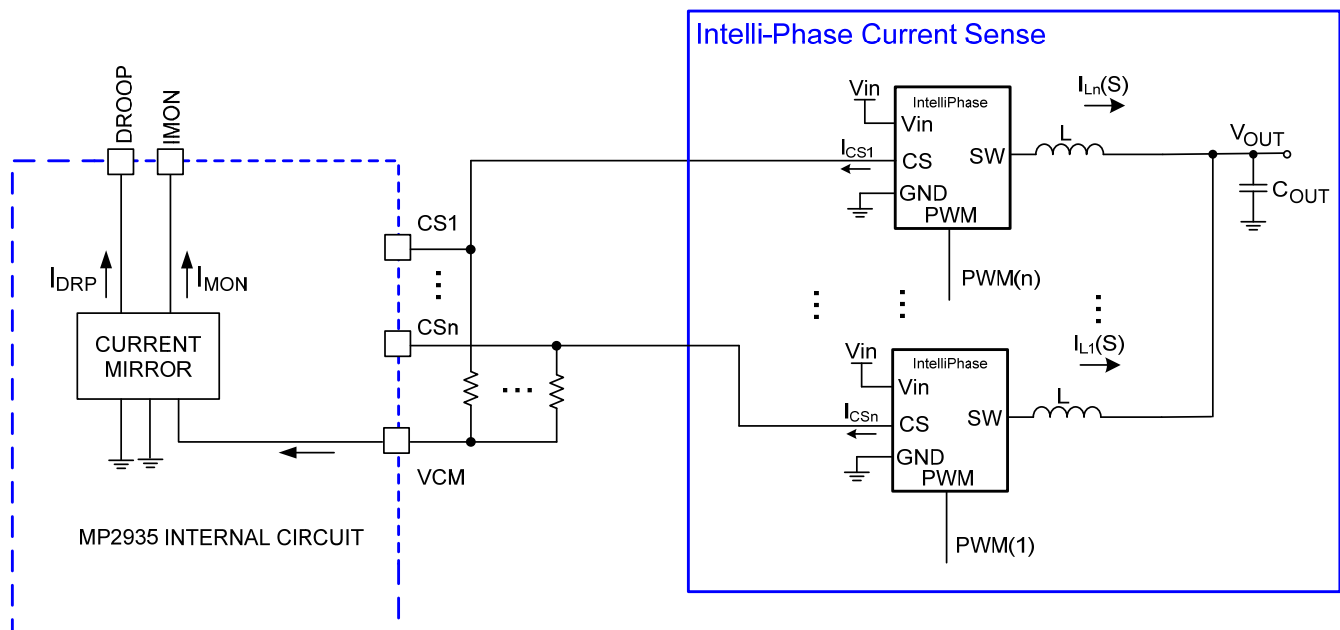


**Figure 3: Intelli-Phase$^{TM}$ Current Sensing Circuit**

The IMON current is a current proportional to VCM pin current, $I_{MON} = \dfrac{I_{VCM}}{16}$ . A resistor, $R_{IMON}$, from IMON pin to GND sets the gain from average sensed inductor current to IMON voltage. A 1nF capacitor added in parallel with $R_{IMON}$ filters the voltage ripple reflected from the inductor ripple current.

$$R_{IMON} = \frac{2048000}{ICCMAX}$$

If the desire ICCMAX is 100A, then select 20.5KΩ for $R_{IMON}$.

The voltage on the IMON pin is clamped to prevent it from going above 1.3V. An 8-bit ADC converts the IMON voltage to the $I_{OUT}$ register. An IMON voltage of 1.28V indicates the current has reached the value represented in the ICC_MAX register.
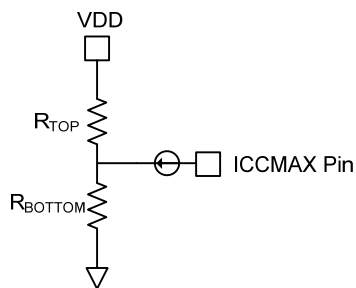


$$R_{TOP} = \frac{(VDD - 0.005xICCMAX)R_{BOTTOM}}{0.005xICCMAX - 2x10^{-5}xR_{BOTTOM}}$$

Set the ICCMAX register with a resistor divider

from VDD voltage. VDD is a 3.3V output voltage from the controller. Using a smaller resistance for $R_{BOTTOM}$ will reduce variation. Let's say we choose $R_{BOTTOM}$ to be 499Ω and the desired maximum current is 100A (ICCMAX=100A), then $R_{TOP}$ is calculated to be 2851Ω. To get the best possible accuracy, use two resistors to match the calculated resistance.

**Phase Current Sensing**

MP2935 has individual inputs to monitor the current in each phase. The phase current information is combined with an internal ramp to create a current-balancing feedback system that is optimized for initial current accuracy and dynamic thermal balance. The current balance information is independent of the total inductor current information used for voltage positioning. The magnitude of the internal ramp can be programmed to optimize the transient response of the system. MP2935 also monitors the supply voltage to achieve feed-forward control whenever the supply voltage changes. A resistor connected from the power input voltage rail to SLOPE pin determines the slope of the internal PWM ramp.

$$Slope = \frac{1}{8} \times \frac{V_{IN}}{R_{SLOPE} + 7000\Omega} \times \frac{1}{C_{SLOPE}} \quad (V/s)$$

$$C_{SLOPE} = 4pF$$

Figure 4 shows the block diagram of the phase current sense and the ramp generator, and the idealized waveforms.
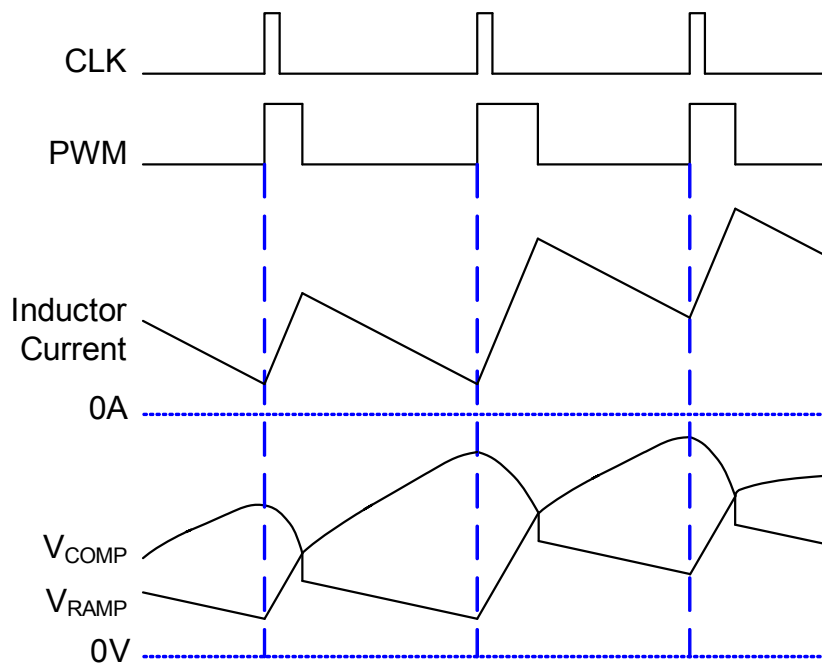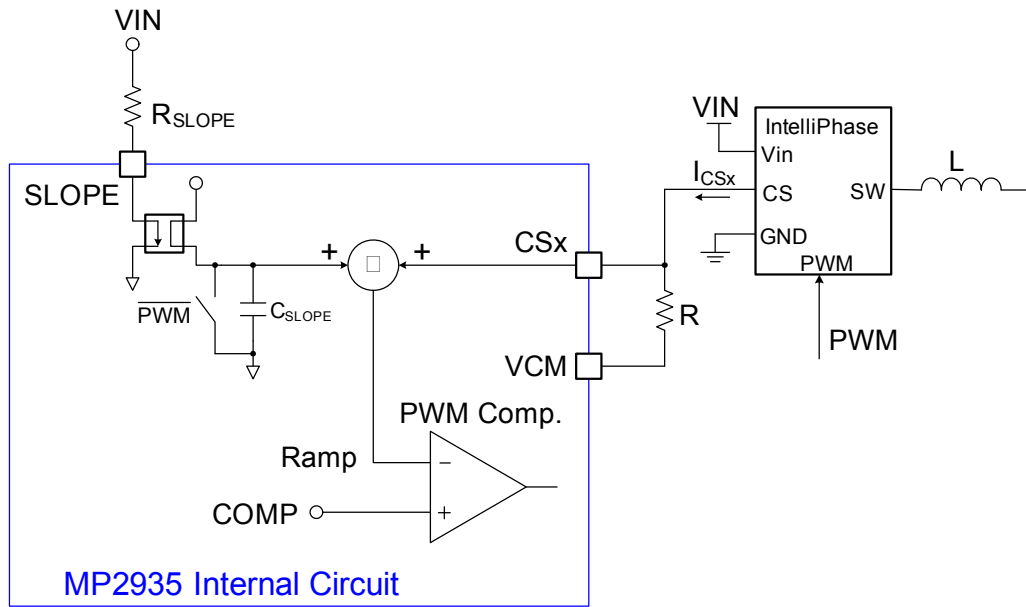
**Figure 4: Block Diagram of Phase Current Sense and Ramp Generator**

External resistors, R, from the CSx pin to the VCM reference pin can convert the $I_{CS}$ current to a related voltage. To increase the current in any given phase, reduce the R for that phase. Upon reaching the current limit, MP2935 switches to full phase PWM mode regardless of power state status to avoid inrush current stress to the phase 1 power stage.

### Voltage Regulation

Output voltage remote sensing is available. Remote sensing allows the voltage regulator to compensate for various resistive drops in the power path and ensure that the voltage seen at the CPU die is the correct level independent of the load current. The VOSEN and GNDSEN pins connect to the Kelvin sense leads at the die of the processor through the processor socket as the signals VCC_SENSE and VSS_SENSE, respectively. This allows the voltage regulator to tightly control the processor voltage at the die, independent of layout inconsistencies and drops. This Kelvin sense technique provides extremely tight load line regulation. Treat these traces as noise-sensitive. For optimal load-line regulation performance, lay out the traces connecting these

two pins to the Kelvin sense leads of the processor in parallel and away from rapidly-rising voltage nodes (switching nodes) and other noisy traces. To achieve optimal performance, place common mode and differential mode RC filters to analog ground on VOSEN and GNDSEN. Keep the filter resistors on the order of 10Ω so that they do not interact with the 50kΩ input resistance of the differential amplifier.

The voltage-mode control loop consists of a high-gain–bandwidth error amplifier. The 8-bit VID DAC sets the non-inverting input voltage. The VID codes are listed in Table 2. The output of the error amplifier goes to the COMP pin, which sets the termination voltage for the internal PWM ramps. The inverting input, FB, connects to the output of the remote sense amplifier through a resistor, $R_{FB}$, to sense and control the output voltage at the remote sense point. $R_{FB}$ generates the droop voltage as a function of the load current—commonly known as active voltage positioning —by injecting the droop current, $I_{DRP}$, into the FB pin. The main loop compensation is incorporated into the feedback network connected between the FB and COMP pins.

## Table 2: SVID Code Table

| DEC | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | $V_{OUT}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | OFF |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | 0.500 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 | 0.510 |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 | 0.520 |
| 4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 | 0.530 |
| 5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 | 0.540 |
| 6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 | 0.550 |
| 7 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 | 0.560 |
| 8 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 | 0.570 |
| 9 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09 | 0.580 |
| 10 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A | 0.590 |
| 11 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B | 0.600 |
| 12 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C | 0.610 |
| 13 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D | 0.620 |
| 14 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E | 0.630 |
| 15 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F | 0.640 |
| 16 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | 0.650 |
| 17 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 | 0.660 |
| 18 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 | 0.670 |
| 19 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13 | 0.680 |
| 20 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14 | 0.690 |
| 21 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 15 | 0.700 |
| 22 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 16 | 0.710 |
| 23 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 17 | 0.720 |
| 24 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 18 | 0.730 |
| 25 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 19 | 0.740 |
| 26 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1A | 0.750 |
| 27 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1B | 0.760 |
| 28 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1C | 0.770 |
| 29 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1D | 0.780 |
| 30 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E | 0.790 |
| 31 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1F | 0.800 |
| 32 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | 0.810 |
| 33 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21 | 0.820 |
| 34 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22 | 0.830 |
| 35 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23 | 0.840 |
| 36 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24 | 0.850 |
| 37 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25 | 0.860 |
| 38 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26 | 0.870 |
| 39 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 27 | 0.880 |
| 40 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28 | 0.890 |
| 41 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 | 0.900 |
| 42 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2A | 0.910 |
| 43 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2B | 0.920 |
| 44 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C | 0.930 |
| 45 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2D | 0.940 |
| 46 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2E | 0.950 |
| 47 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 2F | 0.960 |
| 48 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 | 0.970 |

| DEC | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | V$_{OUT}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 49 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31 | 0.980 |
| 50 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32 | 0.990 |
| 51 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33 | 1.000 |
| 52 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34 | 1.010 |
| 53 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 | 1.020 |
| 54 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36 | 1.030 |
| 55 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37 | 1.040 |
| 56 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38 | 1.050 |
| 57 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39 | 1.060 |
| 58 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3A | 1.070 |
| 59 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 3B | 1.080 |
| 60 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3C | 1.090 |
| 61 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 3D | 1.100 |
| 62 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3E | 1.110 |
| 63 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 3F | 1.120 |
| 64 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | 1.130 |
| 65 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41 | 1.140 |
| 66 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | 1.150 |
| 67 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 43 | 1.160 |
| 68 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 | 1.170 |
| 69 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45 | 1.180 |
| 70 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 46 | 1.190 |
| 71 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 47 | 1.200 |
| 72 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 48 | 1.210 |
| 73 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 49 | 1.220 |
| 74 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 4A | 1.230 |
| 75 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 4B | 1.240 |
| 76 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4C | 1.250 |
| 77 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 4D | 1.260 |
| 78 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 4E | 1.270 |
| 79 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 4F | 1.280 |
| 80 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50 | 1.290 |
| 81 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51 | 1.300 |
| 82 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52 | 1.310 |
| 83 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 | 1.320 |
| 84 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54 | 1.330 |
| 85 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55 | 1.340 |
| 86 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56 | 1.350 |
| 87 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 57 | 1.360 |
| 88 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 58 | 1.370 |
| 89 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 59 | 1.380 |
| 90 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 5A | 1.390 |
| 91 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5B | 1.400 |
| 92 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 5C | 1.410 |
| 93 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5D | 1.420 |
| 94 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5E | 1.430 |
| 95 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5F | 1.440 |
| 96 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 60 | 1.450 |

| DEC | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | V$_{OUT}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 97 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 61 | 1.460 |
| 98 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 62 | 1.470 |
| 99 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 63 | 1.480 |
| 100 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 64 | 1.490 |
| 101 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 65 | 1.500 |
| 102 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 66 | 1.510 |
| 103 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 67 | 1.520 |
| 104 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 68 | 1.530 |
| 105 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 69 | 1.540 |
| 106 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 6A | 1.550 |
| 107 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 6B | 1.560 |
| 108 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 6C | 1.570 |
| 109 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 6D | 1.580 |
| 110 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 6E | 1.590 |
| 111 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 6F | 1.600 |
| 112 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70 | 1.610 |
| 113 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71 | 1.620 |
| 114 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 72 | 1.630 |
| 115 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 73 | 1.640 |
| 116 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 74 | 1.650 |
| 117 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 75 | 1.660 |
| 118 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 76 | 1.670 |
| 119 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 77 | 1.680 |
| 120 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 78 | 1.690 |
| 121 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 79 | 1.700 |
| 122 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 7A | 1.710 |
| 123 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 7B | 1.720 |
| 124 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 7C | 1.730 |
| 125 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 7D | 1.740 |
| 126 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7E | 1.750 |
| 127 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7F | 1.760 |
| 128 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | 1.770 |
| 129 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81 | 1.780 |
| 130 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 82 | 1.790 |
| 131 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 83 | 1.800 |
| 132 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 84 | 1.810 |
| 133 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 85 | 1.820 |
| 134 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 86 | 1.830 |
| 135 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 87 | 1.840 |
| 136 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 88 | 1.850 |
| 137 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 89 | 1.860 |
| 138 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 8A | 1.870 |
| 139 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8B | 1.880 |
| 140 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 8C | 1.890 |
| 141 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 8D | 1.900 |
| 142 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 8E | 1.910 |
| 143 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 8F | 1.920 |
| 144 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 90 | 1.930 |

| DEC | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | $V_{OUT}$ |
|-----|------|------|------|------|------|------|------|------|-----|------|
| 145 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 91 | 1.940 |
| 146 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 92 | 1.950 |
| 147 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 93 | 1.960 |
| 148 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 94 | 1.970 |
| 149 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 95 | 1.980 |
| 150 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 96 | 1.990 |
| 151 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 97 | 2.000 |
| 152 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 98 | 2.010 |
| 153 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 99 | 2.020 |
| 154 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 9A | 2.030 |
| 155 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 9B | 2.040 |
| 156 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 9C | 2.050 |
| 157 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 9D | 2.060 |
| 158 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 9E | 2.070 |
| 159 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 9F | 2.080 |
| 160 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0 | 2.090 |
| 161 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A1 | 2.100 |
| 162 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | A2 | 2.110 |
| 163 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | A3 | 2.120 |
| 164 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | A4 | 2.130 |
| 165 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A5 | 2.140 |
| 166 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | A6 | 2.150 |
| 167 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | A7 | 2.160 |
| 168 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A8 | 2.170 |
| 169 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | A9 | 2.180 |
| 170 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | AA | 2.190 |
| 171 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | AB | 2.200 |
| 172 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | AC | 2.210 |
| 173 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | AD | 2.220 |
| 174 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | AE | 2.230 |
| 175 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | AF | 2.240 |
| 176 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0 | 2.250 |
| 177 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B1 | 2.260 |
| 178 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2 | 2.270 |
| 179 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | B3 | 2.280 |
| 180 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | B4 | 2.290 |
| 181 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | B5 | 2.300 |
| 182 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | B6 | 2.310 |
| 183 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7 | 2.320 |
| 184 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | B8 | 2.330 |
| 185 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B9 | 2.340 |
| 186 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | BA | 2.350 |
| 187 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | BB | 2.360 |
| 188 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | BC | 2.370 |
| 189 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | BD | 2.380 |
| 190 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | BE | 2.390 |
| 191 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | BF | 2.400 |
| 192 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0 | 2.410 |

| DEC | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | V$_{OUT}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 193 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | C1 | 2.420 |
| 194 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2 | 2.430 |
| 195 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C3 | 2.440 |
| 196 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4 | 2.450 |
| 197 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5 | 2.460 |
| 198 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | C6 | 2.470 |
| 199 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | C7 | 2.480 |
| 200 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | C8 | 2.490 |
| 201 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | C9 | 2.500 |
| 202 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | CA | 2.510 |
| 203 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | CB | 2.520 |
| 204 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | CC | 2.530 |
| 205 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | CD | 2.540 |
| 206 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | CE | 2.550 |
| 207 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | CF | 2.560 |
| 208 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | D0 | 2.570 |
| 209 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | D1 | 2.580 |
| 210 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D2 | 2.590 |
| 211 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D3 | 2.600 |
| 212 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | D4 | 2.610 |
| 213 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | D5 | 2.620 |
| 214 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | D6 | 2.630 |
| 215 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D7 | 2.640 |
| 216 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | D8 | 2.650 |
| 217 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | D9 | 2.660 |
| 218 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DA | 2.670 |
| 219 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DB | 2.680 |
| 220 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DC | 2.690 |
| 221 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | DD | 2.700 |
| 222 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | DE | 2.710 |
| 223 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | DF | 2.720 |
| 224 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0 | 2.730 |
| 225 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | E1 | 2.740 |
| 226 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | E2 | 2.750 |
| 227 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | E3 | 2.760 |
| 228 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | E4 | 2.770 |
| 229 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | E5 | 2.780 |
| 230 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | E6 | 2.790 |
| 231 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | E7 | 2.800 |
| 232 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | E8 | 2.810 |
| 233 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | E9 | 2.820 |
| 234 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | EA | 2.830 |
| 235 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | EB | 2.840 |
| 236 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | EC | 2.850 |
| 237 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | ED | 2.860 |
| 238 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | EE | 2.870 |
| 239 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | EF | 2.880 |
| 240 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F0 | 2.890 |

| DEC | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | $V_{OUT}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 241 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | F1 | 2.900 |
| 242 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | F2 | 2.910 |
| 243 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | F3 | 2.920 |
| 244 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | F4 | 2.930 |
| 245 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | F5 | 2.940 |
| 246 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | F6 | 2.950 |
| 247 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | F7 | 2.960 |
| 248 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | F8 | 2.970 |
| 249 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | F9 | 2.980 |
| 250 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | FA | 2.990 |
| 251 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | FB | 3.000 |
| 252 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | FC | 3.010 |
| 253 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | FD | 3.020 |
| 254 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FE | 3.030 |
| 255 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF | 3.040 |

## Load-line Regulation

The droop, known as Adaptive Voltage Positioning (AVP), on MP2935 can be generated by injecting the $I_{DRP}$ current to the feedback resistor.

The current output on the IDROOP pin is $\frac{1}{16}$ of the $I_{VCM}$ current, which is proportional to the total output current. Selecting the proper $R_{FB1}$ value can achieve the desired load-line. In the case of zero droop, floats the IDROOP pin. Figure 5 shows the block diagram of droop generation.

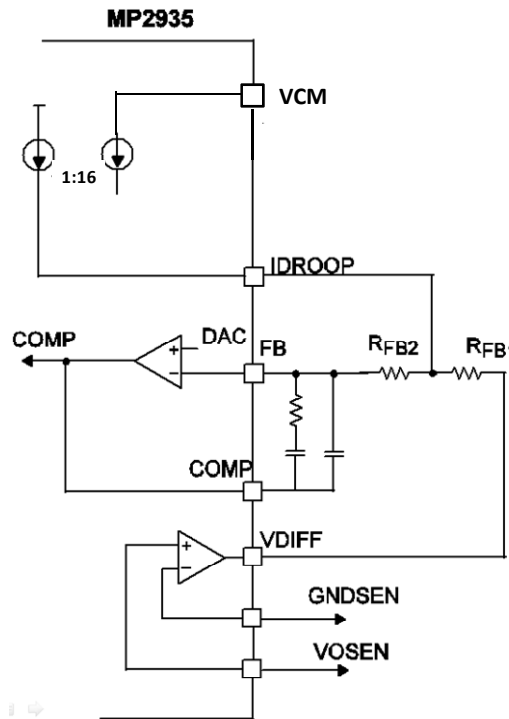$$R_{FB1} = 16 \times 10^5 \times Droop$$

For 1mΩ droop, $R_{FB1}$=1.6KΩ.



**Figure 5: Block Diagram of Droop Generator**

## Output Voltage Offset Programming

After receiving the SVID command for setting the offset (33h), the SVID controller compares the VID plus the proposed offset with the maximum VID of FFh (3.04V), and rejects the SVID command if this value exceeds FFh. If the VID plus proposed offset is less than FFh, the SVID updates the register 33h and the DAC ramps up/down to the new value of VID+Offset with slow slew rate defined in register 25h. During ramp up/down to the new DAC value, the SVID rejects all SVID commands, which is the same behavior as SetVID_Fast/Slow.

## Dynamic VID

The SVID bus sends out new target voltage and slew rate commands to the PWM IC. The VR responds by slewing to the new voltage in a controlled manner without falsely tripping VRRDY, over-voltage, or over-current protection circuits. To meet all market segment requirements, there are three different slew rates: fast, slow, and decay. During fast and slow VID transitions, the SVID controller ramps up/down the VID code step-by-step. There is a 4MHz ID clock for VID change, with defined VID step of 10mV, the maximum slew rate is up to 20mV/µs.

During VID decay, the VR output voltage converges to the new VID target, but does not control the slew rate; the output voltage decays at a rate proportional to the load current.

The VID change triggers a VR_RDY masking timer to prevent a VR_RDY failure. Each VID change resets and restarts the internal VR_RDY masking timer. During the VID transition except VID decay, MP2935 forces a full-phase PWM operation and reset the power state to PS0 by default.

## SetVID_Fast/Slow

If the VR is in a low-power state and receives a new SetVID_Fast/Slow command, then the VR exits the low-power state to normal mode (PS0), operating in full-phase PWM mode to move the voltage by the preset slew rate. The VR remains in PS0, until it receives a new power state command.

## SetVID_Decay

In the case of a SetVID_Decay command, the VR automatically goes to PS2 or remain at PS3. SetVID_Decay command steps up the VID DAC to the target VID at 10mV/step, with each step triggered by VR_SETTLE assert. In the event of a SetPS command during the $V_{OUT}$ decay, MP2935 will enter into the requested power state after $V_{OUT}$ reaches the requested VID value. Whenever the VR exits decay mode whenever it receives a SetVID_Fast/Slow, enters PS0 power state, and ramps up/down to the new VID from its current VID.

Figure 6 shows the detailed diagram of the operation modes with the VID Transition taken into consideration.

Figure 7(a) to 7(d) show the detailed signals of Decay mode operation for different cases.