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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Power Operational Amplifier

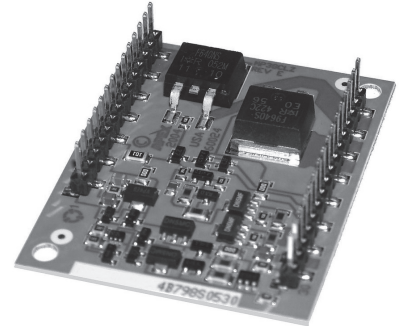


FEATURES

- High Internal Dissipation — 125 Watts
- High Voltage, High Current — 100V, 10A
- Slew Rate — 10V/ μ s
- 4 Wire Current Limit Sensing
- Optional Boost Voltage Inputs

APPLICATIONS

- Linear And Rotary Motor Drives
- Yoke/Magnetic Field Excitation
- Programmable Power Supplies to \pm 45V
- Industrial Audio



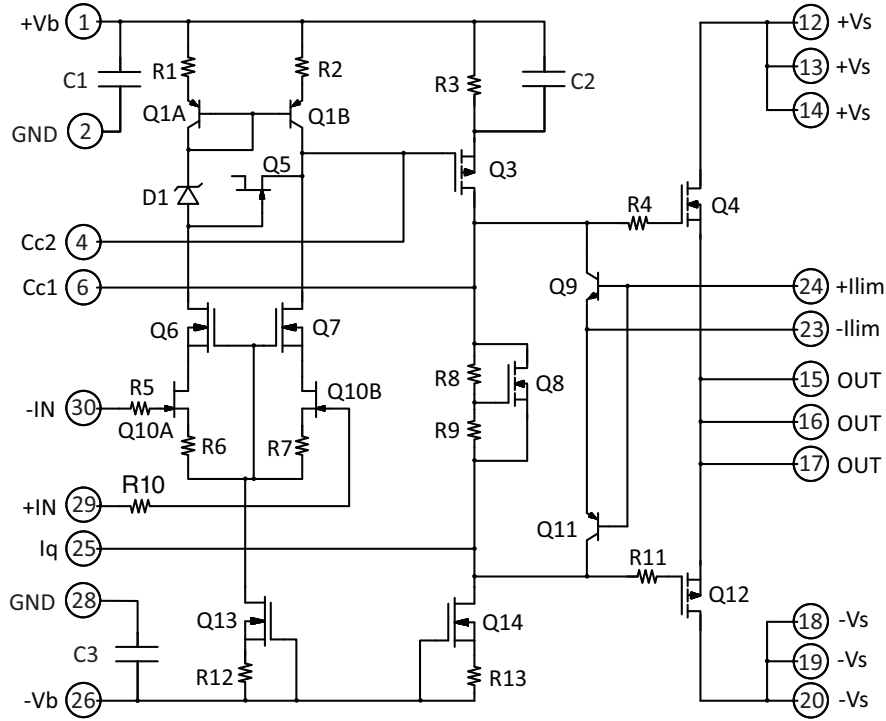
DESCRIPTION

The MP39 is a cost-effective high voltage MOSFET power operational amplifier constructed with surface mount components on a thermally conductive but electrically isolated substrate.

While the cost is low the MP39 offers many of the same features and performance specifications found in much more expensive hybrid power amplifiers.

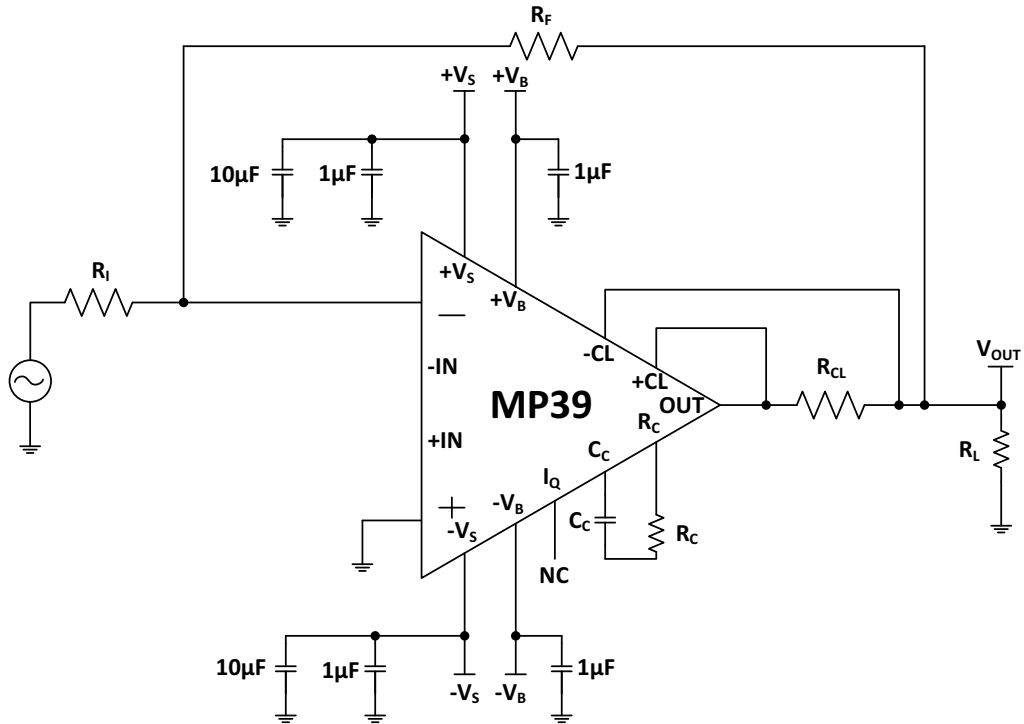
The metal substrate allows the MP39 to dissipate power up to 125 watts and its power supply voltages can range up to \pm 50 Volts (100V total). Optional boost voltage inputs allow the small signal portion of the amplifier to operate at higher supply voltages than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high current for extra efficient operation. External compensation tailors performance to the user needs. A four-wire sense technique allows current limiting without the need to consider internal or external mili-ohm parasitic resistance in the output line. An Iq pin is available which can be used to shut off the quiescent current in the output stage. The output stage then operates class C and lowers quiescent power dissipation. This is useful in applications where output crossover distortion is not important.

Figure 1: Equivalent Schematic



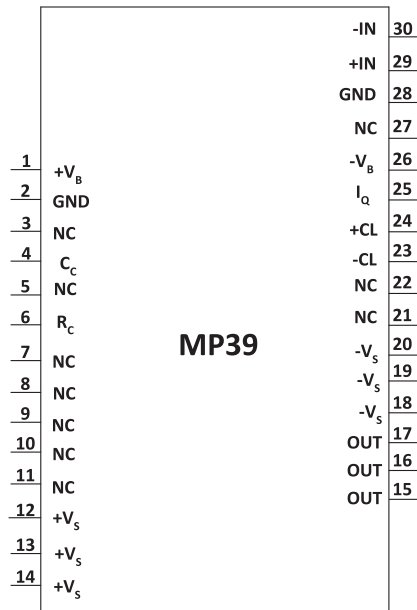
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Viewed from Backplate

Pin Number	Name	Description
1	+VB	The positive boost supply rail. Short to +Vs if unused. See applicable section.
2, 28	GND	Ground. Pins 2 and 28 are not connected on the unit. Connect both pins to system signal ground.
4	CC	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
6	RC	Compensation resistor connection. Select value based on Phase Compensation. See applicable section.
12, 13, 14	+Vs	The positive supply rail.
15, 16, 17	OUT	The output. Connect these pins to load and to the feedback resistor.
18, 19, 20	-Vs	The negative supply rail.
23	-CL	Connect to the load side of the current limit resistor. Current limit will activate as the voltage across R_{CL} increases.
24	+CL	Connect to the OUT side of the current limit resistor. Current limit will activate as the voltage across R_{CL} increases.
25	IQ	Quiescent current reduction pin. Connect to pin 6 to disable the AB bias. See applicable section.
26	-VB	The negative boost supply rail. Short to -Vs if unused. See applicable section.
29	+IN	The non-inverting input.
30	-IN	The inverting input.
All Others	NC	No connection.

SPECIFICATIONS

Unless otherwise noted: $T_C = 25^\circ\text{C}$, $R_C = 100\ \Omega$, $C_C = 470\text{pF}$. DC input specifications are \pm value given. Power supply voltage is typical rating. $\pm V_B = \pm V_S$.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, $+V_S$ To $-V_S$	$+V_S$ to $-V_S$		100	V
Boost Voltage			$\pm V_S \pm 20$	V
Output Current, within SOA	I_O		25	A
Power Dissipation, internal	P_D		125	W
Input Voltage, differential	V_{IN} (Diff)	-20	+20	V
Input Voltage, common mode	V_{cm}	$-V_B$	$+V_B$	V
Temperature, pin solder, -10s			200	$^\circ\text{C}$
Temperature, junction ¹	T_J		175	$^\circ\text{C}$
Temperature, storage		-40	+105	$^\circ\text{C}$
Operating Temperature Range, case	T_C	-40	+85	$^\circ\text{C}$

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.

CAUTION

The MP39 is constructed from MOSFET transistors. ESD handling procedures must be observed.

INPUT

Parameter	Test Conditions	MP39			MP39A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial			5	10		*	3	mV
Offset Voltage vs. temperature	Full temp range		50			*		$\mu\text{V}/^\circ\text{C}$
Offset Voltage vs. supply			15			*		$\mu\text{V}/\text{V}$
Offset Voltage vs. power	Full temp range		30			*		$\mu\text{V}/\text{W}$
Bias Current, initial			10	200		*	100	μA
Bias Current vs. Supply			0.01			*		$\mu\text{A}/\text{V}$
Offset Current, initial			10	50		*	30	μA
Input Impedance, DC			10^{10}			*		Ω
Input Capacitance			20			*		pF
Common Mode Voltage Range	Full temp range	$\pm V_B \mp 15$	$\pm V_B \mp 12$		*	*		V
Common Mode Rejection, DC	Full temp range, $V_{CM} = \pm 20\text{V}$	86	98		*	*		dB
Input Noise	100 kHz BW, $R_S = 1\ \text{k}\Omega$		10			*		$\mu\text{V RMS}$

GAIN

Parameter	Test Conditions	MP39			MP39A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop, @ 15Hz	Full temp range, $C_C = 100\text{pF}$	94	113		*	*		dB
Gain Bandwidth Product	$I_O = 10\text{A}$		2			*		MHz
Power Bandwidth	$R_L = 10\ \Omega$, $V_O = 90\text{V}_{\text{P-P}}$, $C_C = 100\text{pF}$		40			*		kHz
Phase Margin	Full temp range		60			*		°

OUTPUT

Parameter	Test Conditions	MP39			MP39A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing	$I_O = 10\text{A}$	$\pm V_S \mp 8.8$	$\pm V_S \mp 6.0$		*	*		V
Voltage Swing	$\pm V_B = \pm V_S \pm 10\text{V}$, $I_O = 10\text{A}$	$\pm V_S \mp 6.8$	$\pm V_S \mp 1.1$		*	*		V
Settling Time to 0.1%	$A_V = +1$, 10V step, $R_L = 4\ \Omega$		2.5			*		μs
Slew Rate	$A_V = -10$, $C_C = 100\text{pF}$	10			*			V/ μs
Capacitive Load	Full temp range, $A_V = +1$	10			*			nF
Resistance			4			*		Ω
Current, Continuous				10			11	A

POWER SUPPLY

Parameter	Test Conditions	MP39			MP39A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	Full temp range	± 15	± 40	± 50	*	*	*	V
Current, quiescent, boost supply				22			*	mA
Current, quiescent, total				26			*	mA

MP39 • MP39A



THERMAL

Parameter	Test Conditions	MP39			MP39A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case ¹	Full temp range, F>60 Hz			0.9			*	°C/W
Resistance, DC, junction to case	Full temp range, F<60 Hz			1.2			*	°C/W
Resistance, junction to air ²	Full temp range		12		*			°C/W
Temperature Range, case	Meets full range specs	-40		+85	*		*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
2. The MP39 must be used with a heat sink or the quiescent power may drive the unit to junction temperatures higher than 175°C.

Note: *The specification of MP39A is identical to the specification for MP39 in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

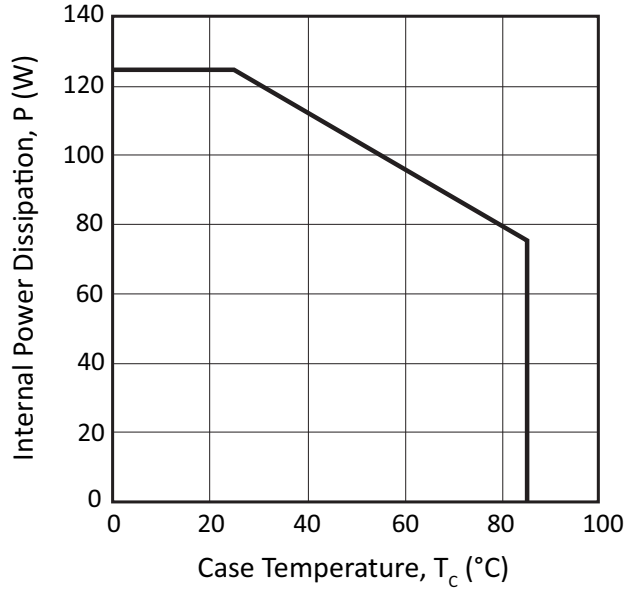


Figure 5: Harmonic Distortion

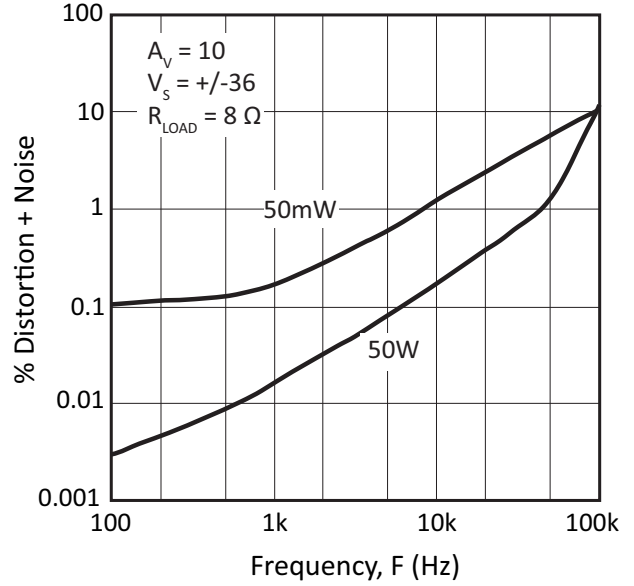


Figure 6: Small Signal Response

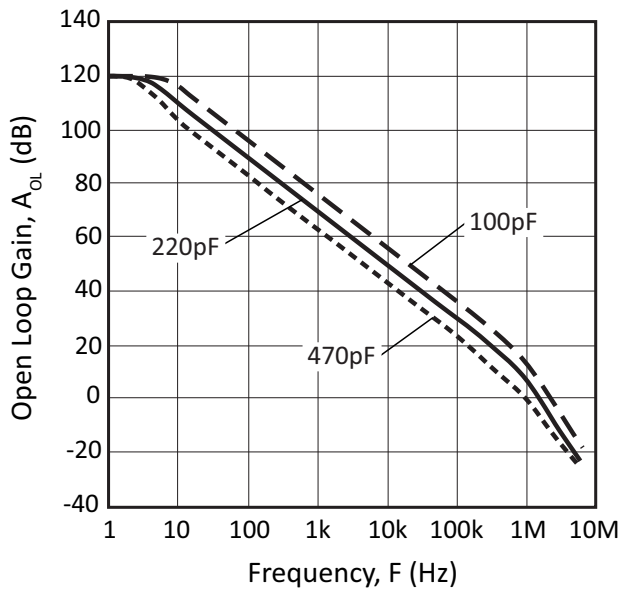


Figure 7: Phase Response

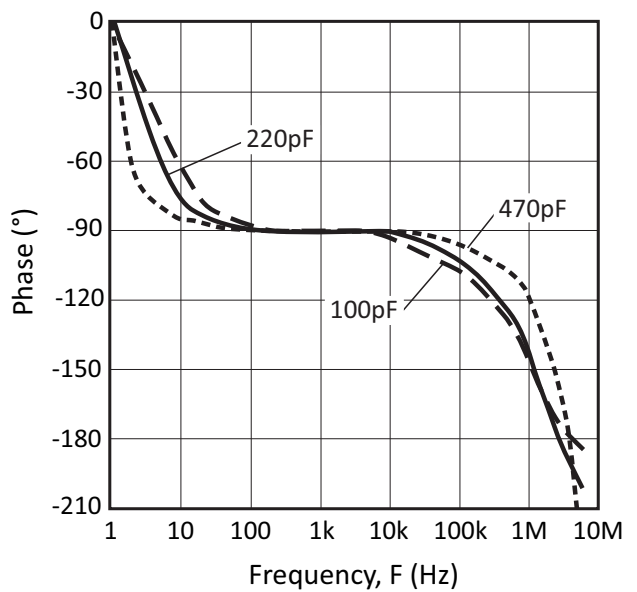


Figure 8: Power Response

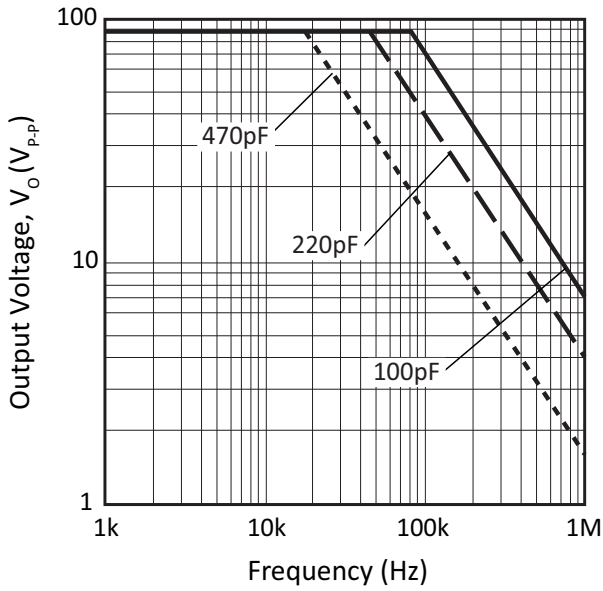


Figure 9: Slew Rate vs. Comp.

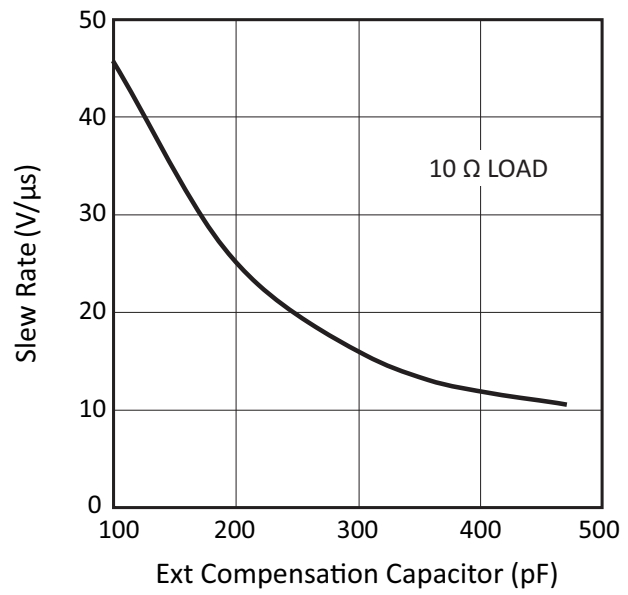
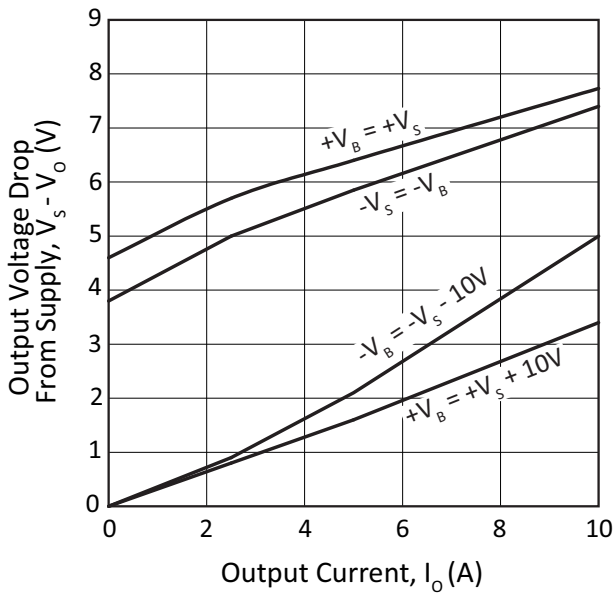
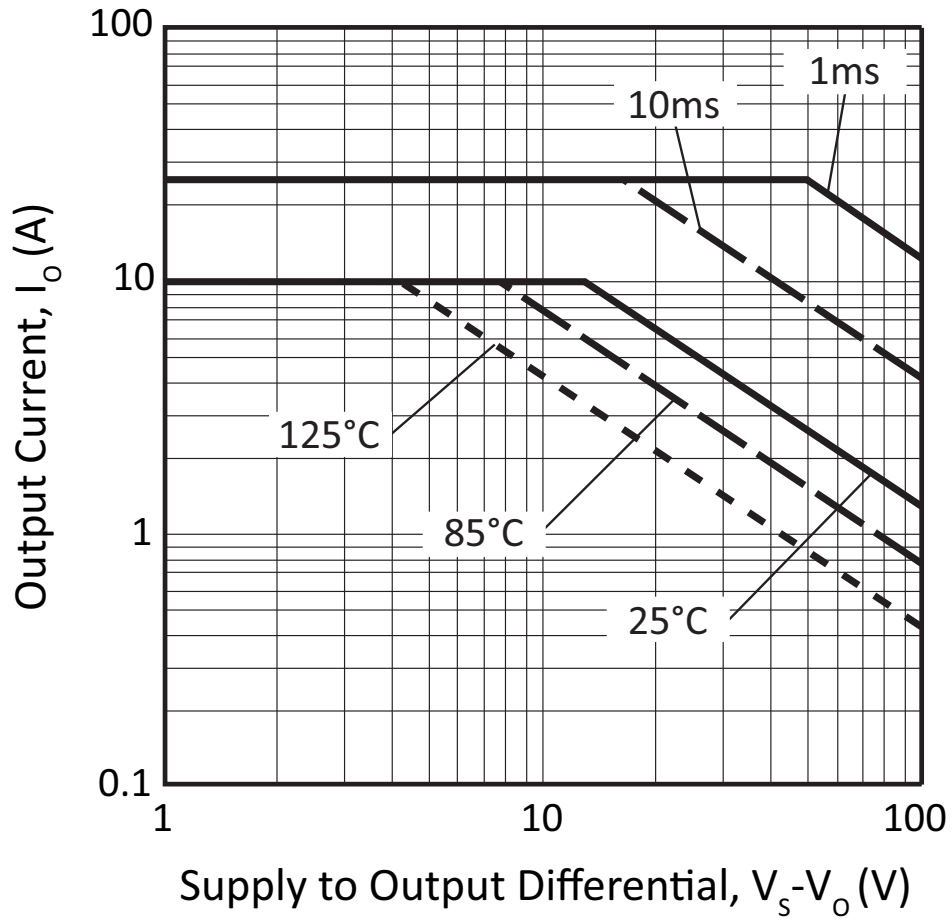


Figure 10: Output Voltage Swing



SAFE OPERATING AREA (SOA)



GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

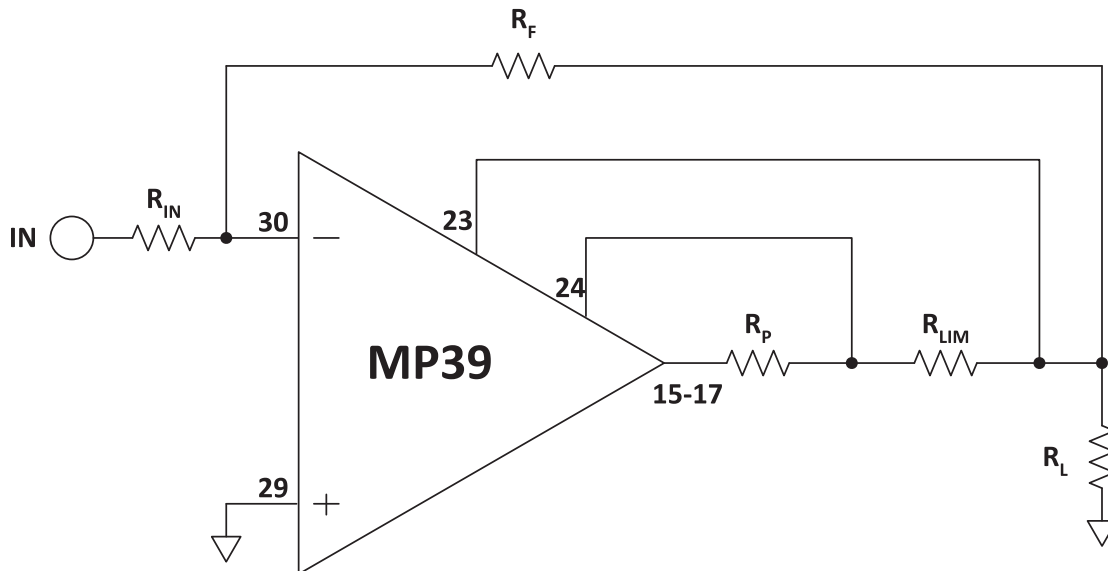
CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 24 must be connected to the amplifier output side and pin 23 connected to the load side of the current limit resistor, R_{LIM} , as shown in Figure 11. This connection will bypass any parasitic resistances, R_p , formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 11.

The value of the current limit resistor can be calculated as follows:

$$R_{LIM}(\Omega) = \frac{0.7V}{I_{LIMIT}(A)}$$

Figure 11: Current Limit

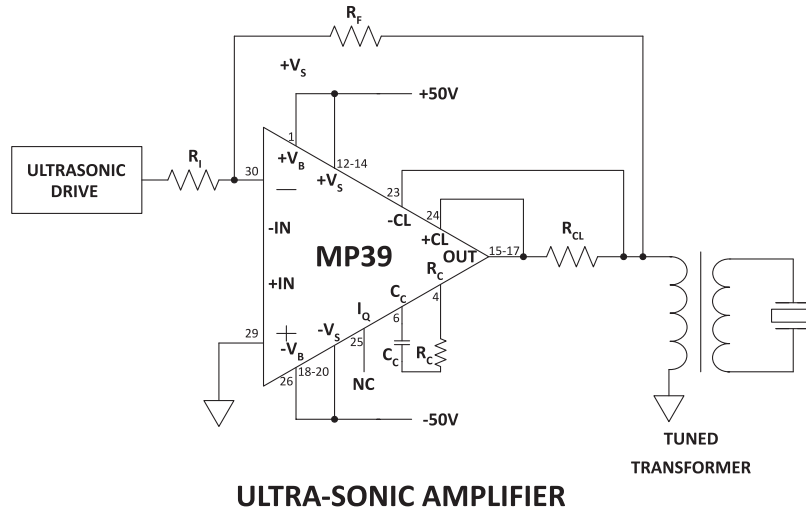


TYPICAL APPLICATION

Ref: Application Note 25

The high power bandwidth and high voltage output of the MP39 allows driving ultra-sonic transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the MP39.

Figure 12: Typical Application



BOOST OPERATION

With the V_b feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_s$ (pins 12-14) and $-V_s$ (pins 18-20) are connected to the high current output stage. An additional 10V on the V_b pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swing to the supply rails is not required the $+V_b$ and $+V_s$ pins must be strapped together as well as the $-V_b$ and $-V_s$ pins. The boost voltage pins must not be at a voltage lower than the V_s pins.

BYPASSING

Proper bypassing of the power supply pins is crucial for proper operation. Bypass the $\pm V_s$ pins with a aluminum electrolytic capacitor with a value of at least $10\mu F$ per amp of expected output current. In addition a $0.47\mu F$ to $1\mu F$ ceramic capacitor should be placed in parallel with each aluminum electrolytic capacitor. Both of these capacitors have to be placed as close to the power supply pins as physically possible. If not connected to the V_s pins (See BOOST OPERATION) the V_b pins should also be bypassed with a $.47\mu F$ to $1\mu F$ ceramic capacitor.

USING THE I_q PIN FUNCTION

Pin 25 (I_q) can be tied to pin 6 (C_c) to eliminate the class AB biasing current from the output stage. Typically this would remove 1-4 mA of quiescent current. The resulting decrease in quiescent power dissipation may be important in some applications. Note that implementing this option will raise the output impedance of the amplifier and increase crossover distortion as well.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 4 and 6. Unity gain stability can be achieved at any compensation capacitance greater than 470 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate.

Gain	C_C	R_C
1	470pF	100 Ω
≥ 3	220pF	Short
≥ 10	100pF	Short

APPLICATION REFERENCES

For additional technical information please refer to the following application notes.

AN01 General Operating Considerations

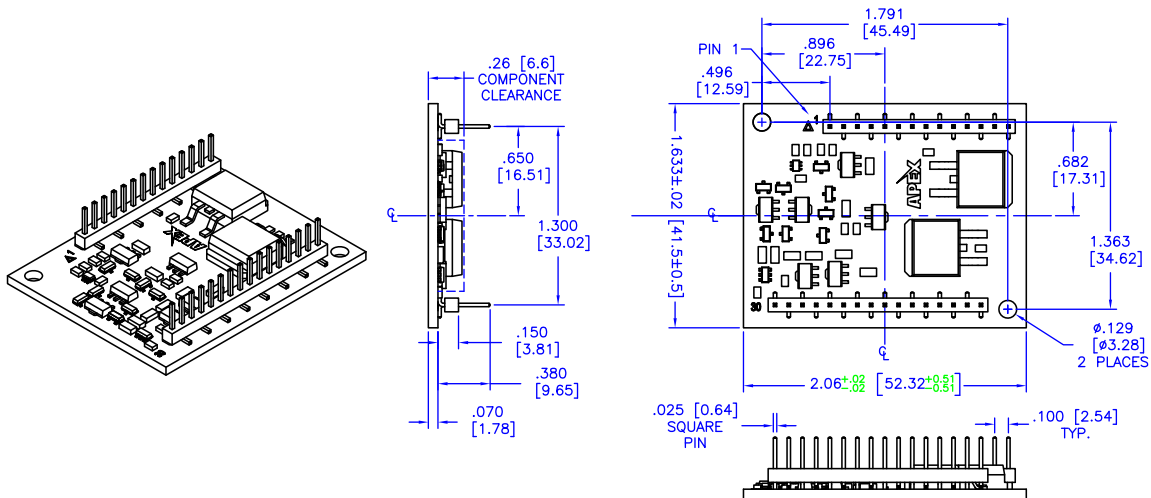
AN11 Thermal Techniques

AN38 Loop Stability with Reactive Loads

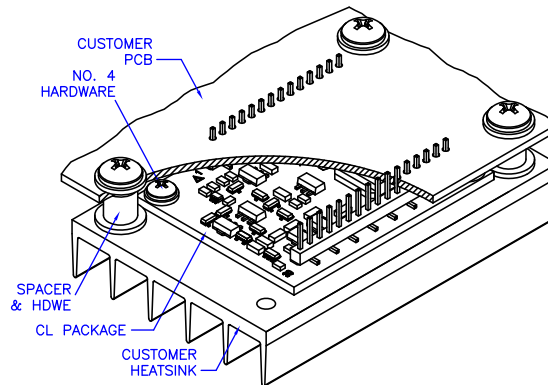
PACKAGE OPTIONS

Part Number	Apex Package Style	Description
MP39	CL	30-pin Open Frame
MP39A	CL	30-pin Open Frame

PACKAGE STYLE CL



SUGGESTED MOUNTING METHOD



NOTES:

1. Dimensions are inches; alternate units are [mm].
2. Recommended PCB hole diameter for pins: .050"
3. 2 oz. copper over 600V dielectric over aluminum substrate
4. Tin-nickel plated phosphor bronze pins
5. Package weight: 0.56 oz. [15.9 g]
6. Mount with #4 or equivalent screws.
7. It is not recommended that mounting of the package rely on the pins for mechanical support. The mounting method shown does not represent a specific design solution or the only way to mount the package.
8. Care must be exercised in designing the mating board, to avoid interference among board components.

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