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MP6501A

8V to 35V, 2.5A Stepper Motor Driver with Integrated MOSFETs

The Future of Analog IC Technology

DESCRIPTION

The MP6501A is a stepper motor driver with a built-in micro stepping translator. It operates from a supply voltage of up to 35V and can deliver motor current up to 2.5A. The MP6501A can operate a bipolar stepper motor in full-, half-, quarter-, and eighth- step modes. Internal safety features include over-current protection, input over-voltage protection, UVLO and thermal shutdown. The part has a fixed 3.3V reference output, which allows it to operate without any control power supply and work with any microcontroller. Ron of the switches is as low as 220mΩ. Current sensing is done by external resistors.

The MP6501A comes in a space-saving TSSOP-28 package with exposed thermal pad.

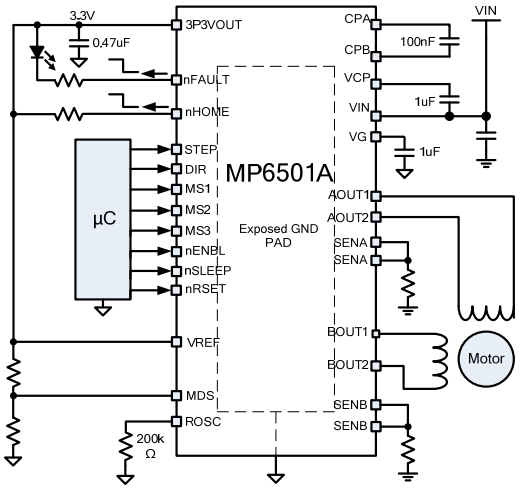
FEATURES

- Wide 8V to 35V Input Voltage Range
- Two Internal Full Bridge PWM Converters
- Low On Resistance(HS:220mΩ; LS:220mΩ)
- No Control Power Supply Required
- Simple Logic Interface
- 3.3 and 5 V Compatible Logic Supply
- Full-, Half-, Quarter-, and Eighth- Step Functionality
- 2.5A Maximum Output Current
- Adjustable Mixed Decay Ratio
- Over-Current Protection
- Input OVP Function
- Thermal Shutdown and UVLO Protection
- Space-saving TSSOP-28 EP Package
- Fault Indication Output

APPLICATIONS

- Bipolar Stepper Motors
- Printers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6501AGF	TSSOP-28 EP	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP6501AGF–Z)

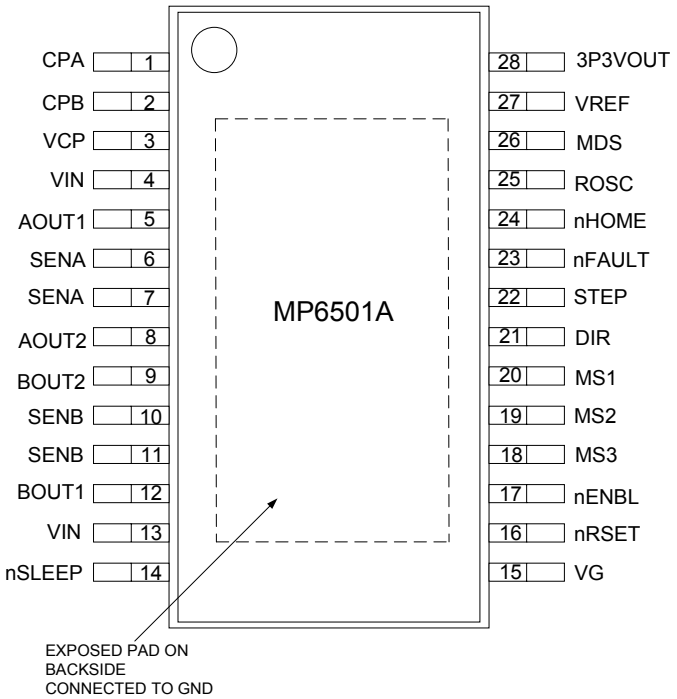
TOP MARKING

MPSYYWW
MP6501A
LLLLLLLLL

MPS: MPS prefix:
YY: year code;
WW: week code:
MP6501A: part number;
LLLLLLLLL: lot number;

PACKAGE REFERENCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} ..... –0.3V to 40V
xOUTx Voltage $V_{A/BOUT1/2}$ ..... -0.7V to 40V
VCP, CPB ..... V_{IN} to V_{IN}+6.5V
ESD Rating (HBD) 2kV
SENA, SENB 700mV
All Other Pins to AGND
(Except for 3P3VOUT and VG)
..... -0.3V to 6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 3.9W
Storage Temperature ..... -55°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Solder) ..... +260°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 8V to 35V
Output Current $I_{A,BOUT}$ ..... ±2.5A
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP-28 EP (9.7mmx6.4mm)
..... 32 ..... 6.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input Supply Voltage	V_{IN}		8	24	35	V
Quiescent Current	I_Q	V_{IN}=24V; nENBL=0; nSLEEP=1, with no load		7	10	mA
	I_{SLEEP}	V_{IN}=24V; nSLEEP=0			1	µA
Voltage Regulator						
3P3VOUT Reference Output	V_{3P3}	IOUT=1mA	3.2	3.3	3.45	V
Internal MOSFETs						
Output On Resistance	R_{HS}	V_{IN}=24V, I_{OUT}=1A, T_J=25°C		0.22	0.35	Ω
		V_{IN}=24V, I_{OUT}=1A, T_J=85°C		0.25		Ω
	R_{LS}	V_{IN}=24V, I_{OUT}=1A, T_J=25°C		0.22	0.35	Ω
		V_{IN}=24V, I_{OUT}=1A, T_J=85°C		0.25		Ω
Body Diode Forward Voltage	V_F	I_{OUT}=1.5A			1.3	V
Control Logic						
Input Logic 'Low' Threshold	V_{IL}	All Logic Pins			0.6	V
Input Logic 'High' Threshold	V_{IH}	All Logic Pins	2			V
Logic Input Current	$I_{IN(H)}$	V_{IH}=5V	-25		25	µA
	$I_{IN(L)}$	V_{IL}=0.8V	-8		8	µA
Internal Pull Down Resistance	R_{PD}	All Logic Pins		530		kΩ
nHOME nFAULT Outputs(Open-Drain Outputs)						
Output Low Voltage	V_{OL}	I_O=5mA			0.5	V
Output High Leakage Current	I_{OH}	V_O=3.3V			1	µA
Protection Circuit						
UVLO Rising Threshold	V_{IN_RISE}		6.5	7	7.7	V
UVLO Hysteresis[5]	V_{HYS}			970		mV
Input OVP Threshold	V_{OVP}		36	37.9	40	V
Input OVP Hysteresis	ΔV_{OVP}			600		mV
Over-Current Trip Level	I_{OCP1}	Sinking	3.5	6.75	10	A
	I_{OCP2}	Sourcing	3.5	6.75	10	A
Over-Current Deglitch Time[5]	t_{OCP}			1		µs
Thermal Shutdown[5]	T_{TSD}			165		°C
Thermal Shutdown Hysteresis[5]	ΔT_{TSD}			30		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN}=24V, T_A = +25°C, unless otherwise noted.

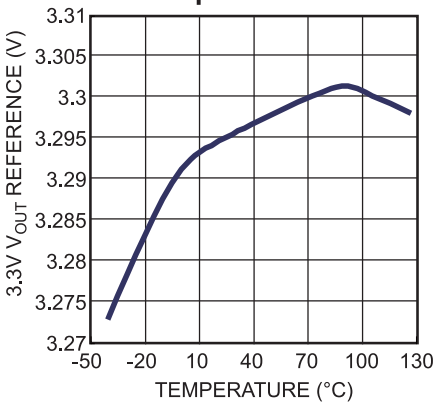
Current Control						
Constant Off Time	t_{OFF}	R_t=200kΩ	20	30	40	µs
Blanking time	t_{BLANK}			2		µs
Crossover Dead Time	t_{DT}	HS off to LS on or LS off to HS on for one bridge arm		400		ns
VREF Input Current	I_{REF}	V_{REF}=3.3V			3.5	µA
SENx Trip Voltage	V_{TRIP}	V_{REF}=3.3V, 100% (no switch in test mode)	600	645	700	mV
Current Trip Accuracy	ΔI_{TRIP}	V_{REF}=3.3V, 70%-100%	-5		5	%
		V_{REF}=3.3V, 38%-64%	-10		10	%
		V_{REF}=3.3V, 19%-30%	-15		15	%
		V_{REF}=3.3V, <10%	-20		20	%
Charge Pump Frequency	f_{CP}			525		kHz

Notes:

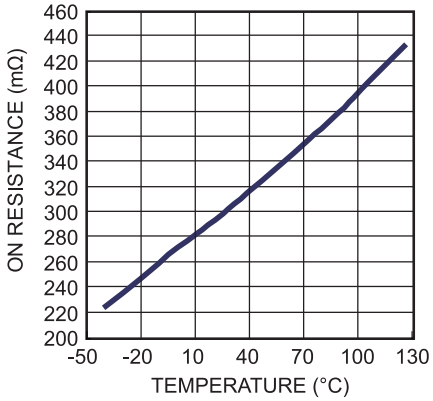
5) Not tested in production.

TYPICAL CHARACTERISTICS

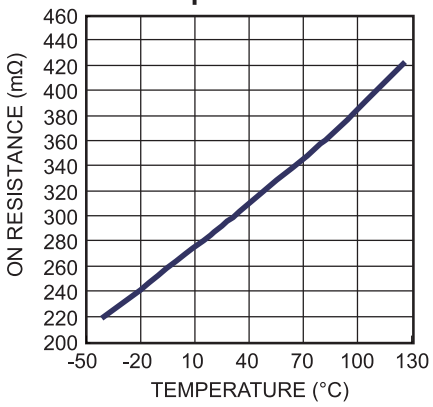
3.3V V_{OUT} Reference vs. Temperature



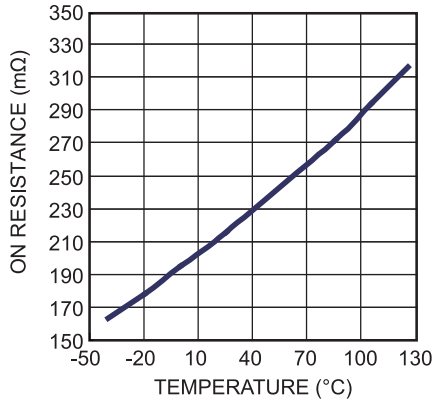
Bridge A HS On Resistance vs. Temperature



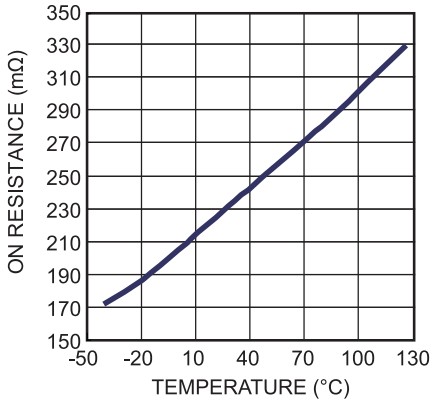
Bridge B HS On Resistance vs. Temperature



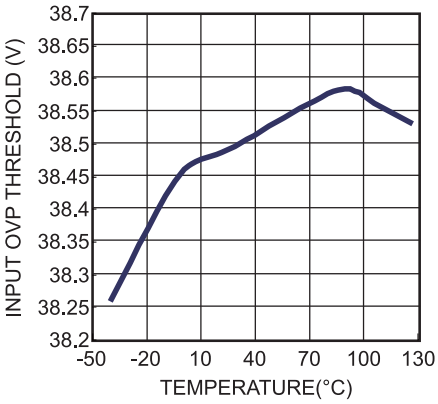
Bridge A LS On Resistance vs. Temperature



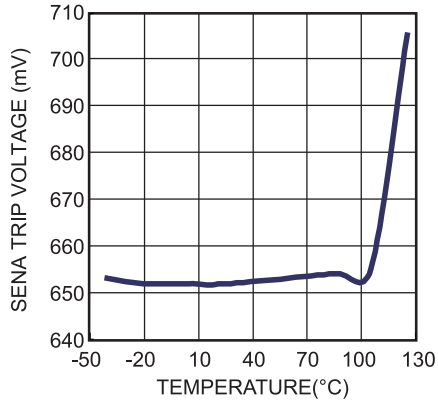
Bridge B LS On Resistance vs. Temperature



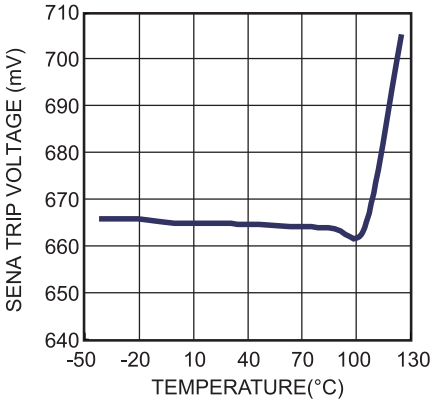
Input OVP Threshold vs. Temperature



SENA Trip Voltage vs. Temperature



SENB Trip Voltage vs. Temperature

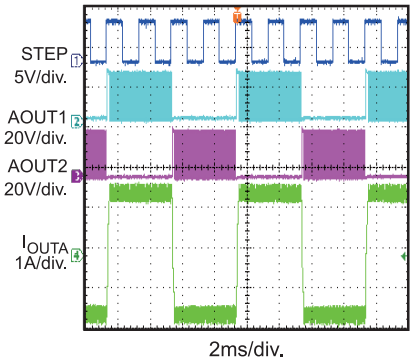


TYPICAL PERFORMANCE CHARACTERISTICS

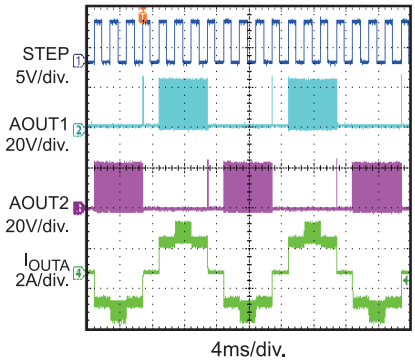
V_{IN}=24V, I_{OUT}=2.5A, T_A=25°C, F_{STEP}=500Hz, Resistor+Inductor Load: R=3.3ohm, L=1.5mH/channel, Automatic Decay, unless otherwise noted.

Steady State-Full Step

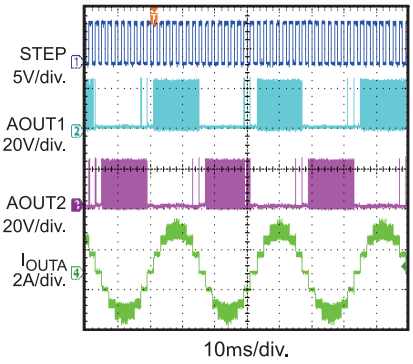
I_{OUT} = 1.8A



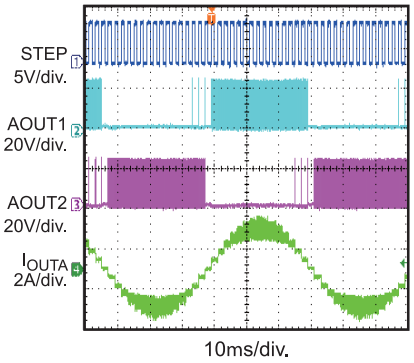
Steady State-Half Step



Steady State-Quarter Step

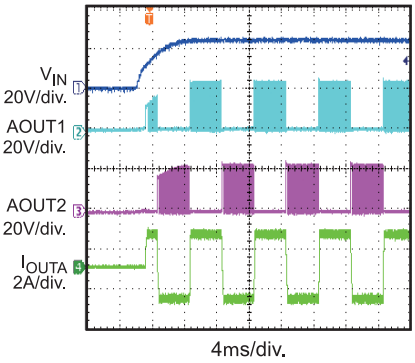


Steady State-Eighth Step

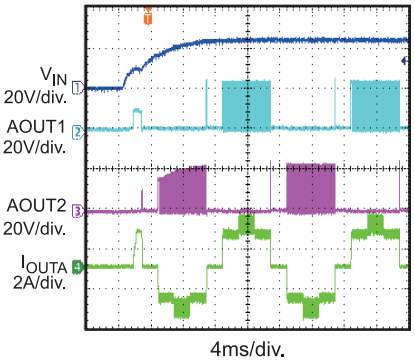


Power Ramp Up-Full Step

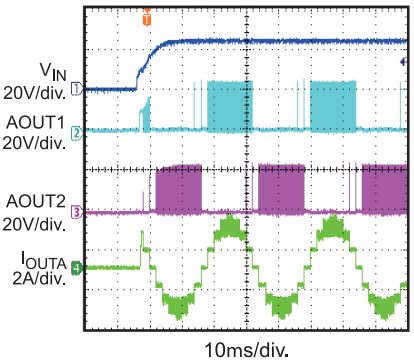
I_{OUT} = 1.8A



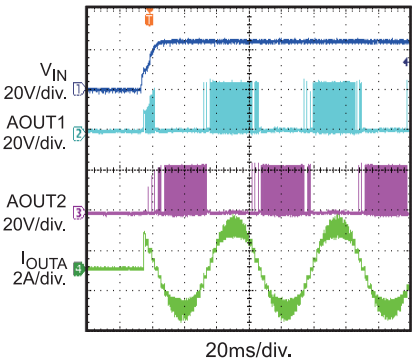
Power Ramp Up-Half Step



Power Ramp Up-Quarter Step

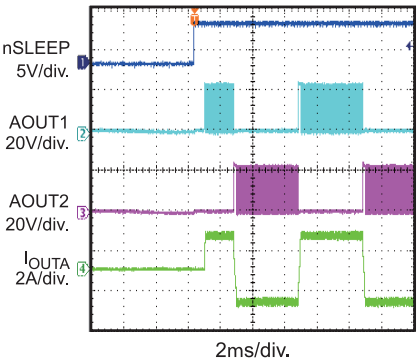


Power Ramp Up-Eighth Step



Sleep Recovery-Full Step

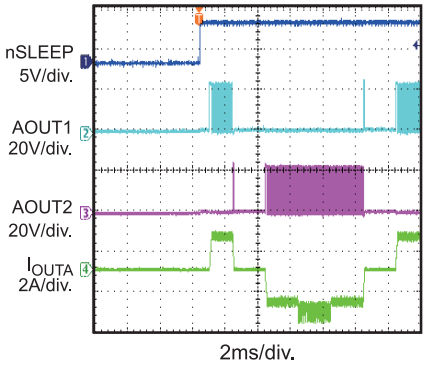
I_{OUT} = 1.8A



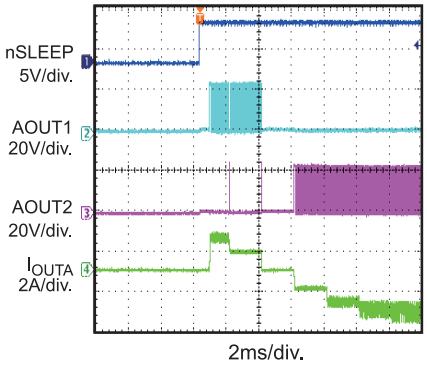
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=24V, I_{OUT}=2.5A, T_A=25°C, F_{STEP}=500Hz, Resistor+Inductor Load: R=3.3ohm, L=1.5mH/channel, Automatic Decay, unless otherwise noted.

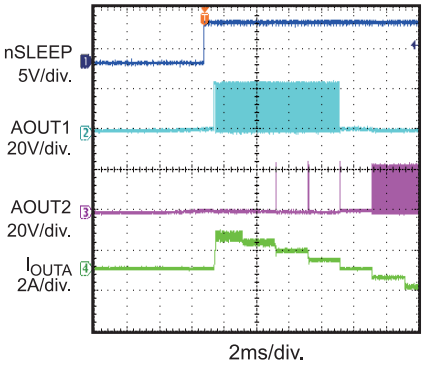
Sleep Recovery-Half Step



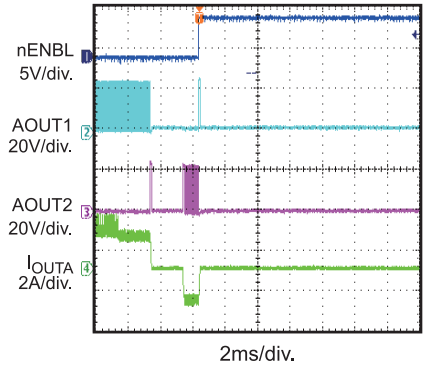
Sleep Recovery-Quarter Step



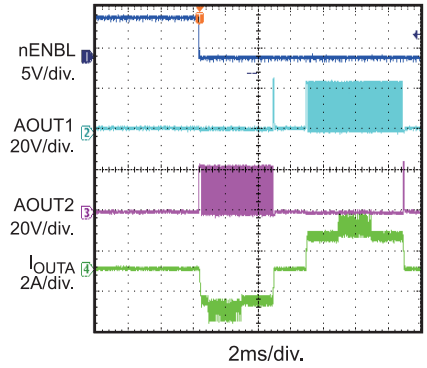
Sleep Recovery-Eighth Step



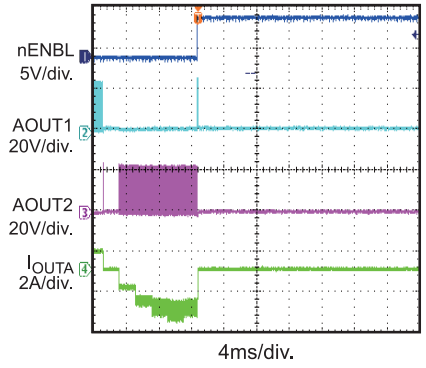
Disable-Half Step



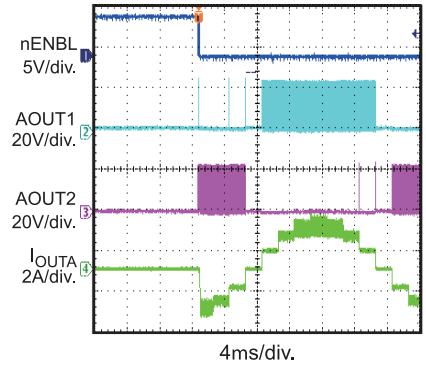
Enable-Half Step



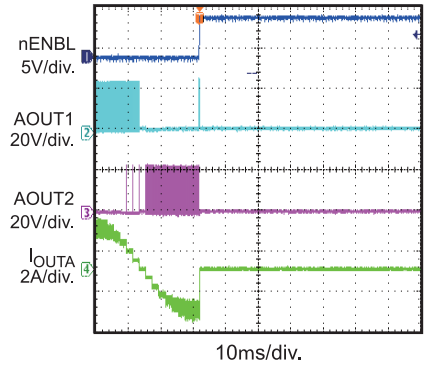
Disable-Quarter Step



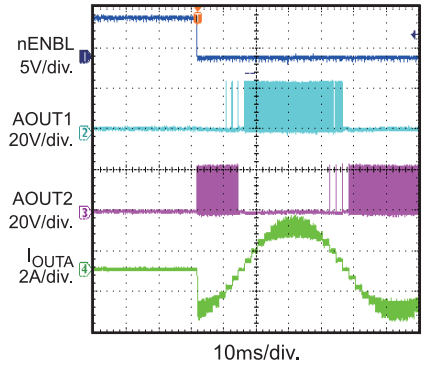
Enable-Quarter Step



Disable-Eighth Step



Enable-Eighth Step



PIN FUNCTIONS

Pin #	Name	Description
1	CPA	Charge Pump Capacitor. Connect a 100nF ceramic capacitor between these pins. The capacitor needs to be rated for at least the voltage applied to VIN.
2	CPB	
3	VCP	Charge Pump Output. Requires a 1uF 16V ceramic capacitor to VIN.
4,13	VIN	Input Supply Voltage. Both VIN pins must be connected to the same supply.
5	AOUT1	Bridge A Output Terminal 1.
6,7	SENA	Bridge A Sense Resistor Connector. Connect to current sensor resistor for bridge A.
8	AOUT2	Bridge A Output Terminal 2.
9	BOUT2	Bridge B Output Terminal 2.
10,11	SENB	Bridge B Sense Resistor Connector. Connect to current sensor resistor for bridge B.
12	BOUT1	Bridge B Output Terminal 1.
14	nSLEEP	Sleep Mode Input. Logic low to enter low-power sleep mode. Internal pull down.
15	VG	Low Side MOSFETs Gate Driver. Decouple with a 1uF 16V ceramic capacitor to GND.
16	nRSET	Reset Input. Logic low initializes the translator and control logic circuit. Internal pull down.
17	nENBL	Enable Input. Logic high to disable the bridge outputs and translator operation, logic low to enable. Internal pull down.
18	MS3	Mode Select. See ”Microstep Select” below for details. MS1-MS3 sets the step mode – full-, half-, quarter-, or eighth- step. Internal pull down.
19	MS2	
20	MS1	
21	DIR	Direction Input. Logic level sets direction of rotation. Internal pull down.
22	STEP	Step Input. Rising edge sequences the translator and advances the motor one increment. Internal pull down.
23	nFAULT	Fault Indication. Open-drain output type, logic low when in fault condition (OCP, OTP, OVP).
24	nHOME	Home Position. Open-drain output type, logic low when at home state of step table.
25	ROSC	Constant Off Time Setting Input. Connect a resistor to GND.
26	MDS	Mixed Decay Setting. See “Decay Modes” below for details.
27	VREF	Reference Voltage Input. Voltage applied to this pin defines the current through the motor. Can be connected to 3P3VOUT.
28	3P3VOUT	3.3V Regulator Output. Decouple with a 0.47μF 6.3V ceramic capacitor to GND.

BLOCK DIAGRAM

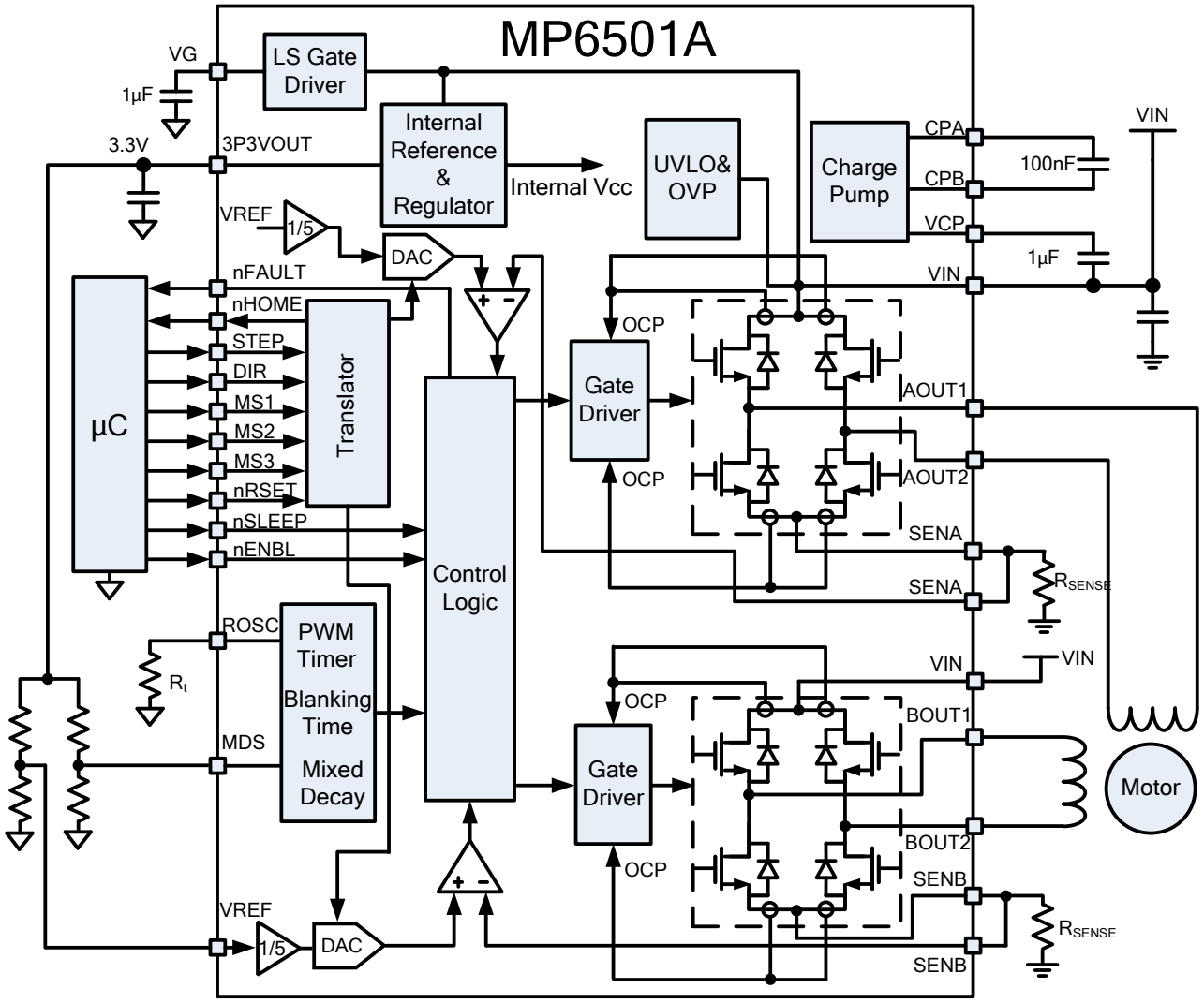


Figure 1: Functional Block Diagram

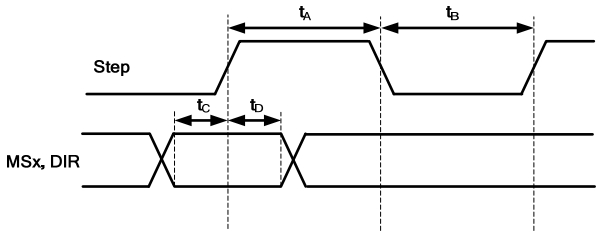
OPERATION

The MP6501A is a bipolar stepper motor driver that integrates 8 N-Channel power MOSFETs arranged as 2 full-bridges, with 2.5A current capability over a wide input voltage range of 8V to 35V. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth- step modes. The current in each of the two output full-bridges is regulated with programmable constant off-time PWM (pulse width modulated) control circuitry. At each step, the current for each full-bridge is set by the value of its external current sense resistor, a reference voltage (V_{REF}), and the output voltage of its DAC which is controlled by the output of the translator.

Stepping

The motor moves step by step by applying a series of pulses to the STEP pin. A rising edge on the STEP input sequences the translator one increment in the direction set by the level of the DIR input. The translator controls the input to the DACs and the direction of current flow in each winding. The amplitude of the increment is determined by the state of inputs MS1, MS2 and MS3 (see Table 1).

The STEP input minimum high/low pulse width is 1us. The logic control signals MSx and DIR require at least 200ns setup time and hold time to the STEP rising edge.



Time Duration	Symbol	Typ.	Unit
Step minimum HIGH pulse width	t_A	1	µs
Step minimum LOW pulse width	t_B	1	µs
Setup time, input change to STEP	t_C	200	ns
Hold time, input change to STEP	t_D	200	ns

Figure 2: Logic Timing Diagram

The motor winding currents are regulated by a programmable constant off-time PWM current control circuit. This operates as follows:

- Initially, a diagonal pair of MOSFETs turns on so current can flow through the motor winding.
- The current increases in the motor winding, which is sensed by an external sense resistor (R_{SENSE}). During the initial blanking time t_{BLANK}, the high-side MOSFET always turns on regardless of current limit detection.
- When the voltage across R_{SENSE} reaches the current regulation threshold, the internal current comparator either shuts off the high-side MOSFET so the winding inductance current freewheels through the two low-side MOSFETs (slow decay), or turns on the opposite diagonal pair of MOSFETs so the current flows back to the input (fast decay).
- The current keeps decreasing for the constant off-time.
- The cycle then repeats.

The constant off-time, t_{off}, is determined by the selection of an external resistor R_t which is approximated by

$$t_{OFF}(ns) = 190 \times R_t(k\Omega)$$

The full-scale (100%) current limit threshold is calculated by

$$I_{Max-LIMIT} = \frac{V_{REF}}{5 \times R_{SENSE}}$$

The DAC output reduces the V_{REF} output to the current sense comparator in precise steps (see table 2 for $\%I_{Trip-LIMIT}$ at each step).

$$I_{Trip-LIMIT} = \%I_{Trip-LIMIT} I_{Max-LIMIT}$$

Microstep Select (MS1, MS2, MS3)

The step mode is selected by applying logic high and low voltages to the MS1, MS2 and MS3 pins as shown in Table 1. The MP6501A supports full-, half-, quarter-, and eighth- step modes for progressively finer step

resolution and control. Full step has four states with each motor winding driven with either 70.7% maximum positive current or 70.7% maximum negative current. This provides four steps per electrical rotation. Half step creates 8 steps per electrical rotation. Quarter- and eighth- step provide 16 and 32 steps per rotation respectively. Table 2 shows the relative current level sequence for different settings of MSx.

Table 1: Stepping Format

MS3	MS2	MS1	STEP MODE
L	L	L	Full Step
L	L	H	Half Step
L	H	L	Quarter Step
L	H	H	Eighth Step
H	L	L	Reserved
H	L	H	Reserved
H	H	L	Reserved
H	H	H	Reserved

Decay Modes

During the PWM off time, the output current decay can operate in slow, fast, or mixed decay, depending on the voltage level at the MDS input, and any current change commanded by a STEP transition.

If the voltage on the MDS input pin is less than 2.5V, then mixed decay mode with adjustable fast decay ratio is selected. The time that the device operates in fast decay is approximated by:

$$t_{FD} = V_{mds}(V) \times 0.4 \times t_{OFF}$$

After this fast decay portion t_{FD}, the device will switch to slow decay mode for the remainder of the constant off-time period. Note that if the MDS pin is set to 0V (connected to ground), slow decay is used for the entire off time.

If the voltage at the MDS input is greater than 2.8 V, then automatic decay mode is selected.

In automatic decay mode, if the commanded current level is equal or higher than the level at the previous step, then slow decay is selected; if current level is lower than previous level, then mixed decay with fixed 30% fast decay ratio is selected.

nRSET, nSLEEP, and nENBL Operation

When the nRSET pin is set to low, the excitation position is forcibly set to the home position. The step input signal is ignored during this period.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the gate drive charge pump and 3P3VOUT regulator is stopped; all the internal circuits and H-bridge outputs are disabled. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, some time (approximately 1 ms) needs to pass before issuing a STEP command, to allow the internal circuitry to stabilize.

The nENBL pin is used to control the output drivers. When nENBL is low, the output H-bridge outputs are enabled, and rising edges on the STEP pin are recognized. When nENBL is high, the H-bridge outputs are disabled, and the STEP input is ignored.

Blanking Time

There is usually a current spike during the switching transition due to the body diode's reverse-recovery current or the distributed inductance or capacitance. This current spike requires filtering to prevent it from erroneously shutting down the high-side MOSFET. An internal fixed blanking time t_{BLANK} blanks the output of the current sense comparator when the outputs are switched, which is also the minimum on time for high-side MOSFET.

In automatic decay mode, if the current limit is reached within the blanking time, the mixed decay with 30% fast decay ratio is performed after the blanking time.

Charge Pump

The MP6501A integrates an internal charge pump to generate gate drive voltage for the high-side MOSFETs. The charge pump requires a 100nF ceramic capacitor (rated for at least the voltage applied to VIN) to be connected between the CPA and CPB pins, and a 1uF 16V ceramic capacitor connected between VCP and VIN.

Fault

MP6501A provides a nFAULT pin, which reports the system if the protection circuit operates by detecting a fault condition such as OCP, OTP and OVP. This pin is of the open-drain output type and will be driven low once

the fault condition occurs. If the fault condition is released, the nFAULT pin would be pulled to high level.

Over-Current Protection

The over-current protection circuit limits the current through the FET by disabling the gate driver. If the over-current limit threshold is reached and lasts for longer than the over-current deglitch time, all MOSFETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The driver will remain disabled and is reset to enable state after 5ms(typ). After 5 times auto-recovery, the chip will shutdown if the over-current condition still exists.

Over-current conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an over-current shutdown. Note that over-current protection does not use the current sense circuitry used for PWM current control, and is independent of the sense resistor value or VREF voltage.

Over-Voltage Protection

If the input voltage on the VIN pin is higher than the OVP threshold, the H-bridge output will be disabled and the nFAULT pin will be driven low. This protection is released when VIN drops to a safe level.

Input UVLO Protection

If at any time the voltage on the VIN pin falls below the under-voltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when VIN rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, all MOSFETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

Table 2: Relative Current Level Sequence

Home position is at step angle 45°

1/8 Step #	1/4 Step #	Half Step #	Full Step #	Phase A Current $\%I_{Trip-LIMIT}$ (%)	Phase B Current $\%I_{TRIP-LIMIT}$ (%)	Step Angle (°C)
1	1	1		100.00	0.00	0.0
2				98.08	19.51	11.3
3	2			92.39	38.27	22.5
4				83.15	55.56	33.8
5	3	2	1	70.71	70.71	45.0
6				55.56	83.15	56.3
7	4			38.27	92.39	67.5
8				19.51	98.08	78.8
9	5	3		0.00	100.00	90.0
10				-19.51	98.08	101.3
11	6			-38.27	92.39	112.5
12				-55.56	83.15	123.8
13	7	4	2	-70.71	70.71	135.0
14				-83.15	55.56	146.3
15	8			-92.39	38.27	157.5
16				-98.08	19.51	168.8
17	9	5		-100.00	0.00	180.0
18				-98.08	-19.51	191.3
19	10			-92.39	-38.27	202.5
20				-83.15	-55.56	213.8
21	11	6	3	-70.71	-70.71	225.0
22				-55.56	-83.15	236.3
23	12			-38.27	-92.39	247.5
24				-19.51	-98.08	258.8
25	13	7		0.00	-100.00	270.0
26				19.51	-98.08	281.3
27	14			38.27	-92.39	292.5
28				55.56	-83.15	303.8
29	15	8	4	70.71	-70.71	315.0
30				83.15	-55.56	326.3
31	16			92.39	-38.27	337.5
32				98.08	-19.51	348.8

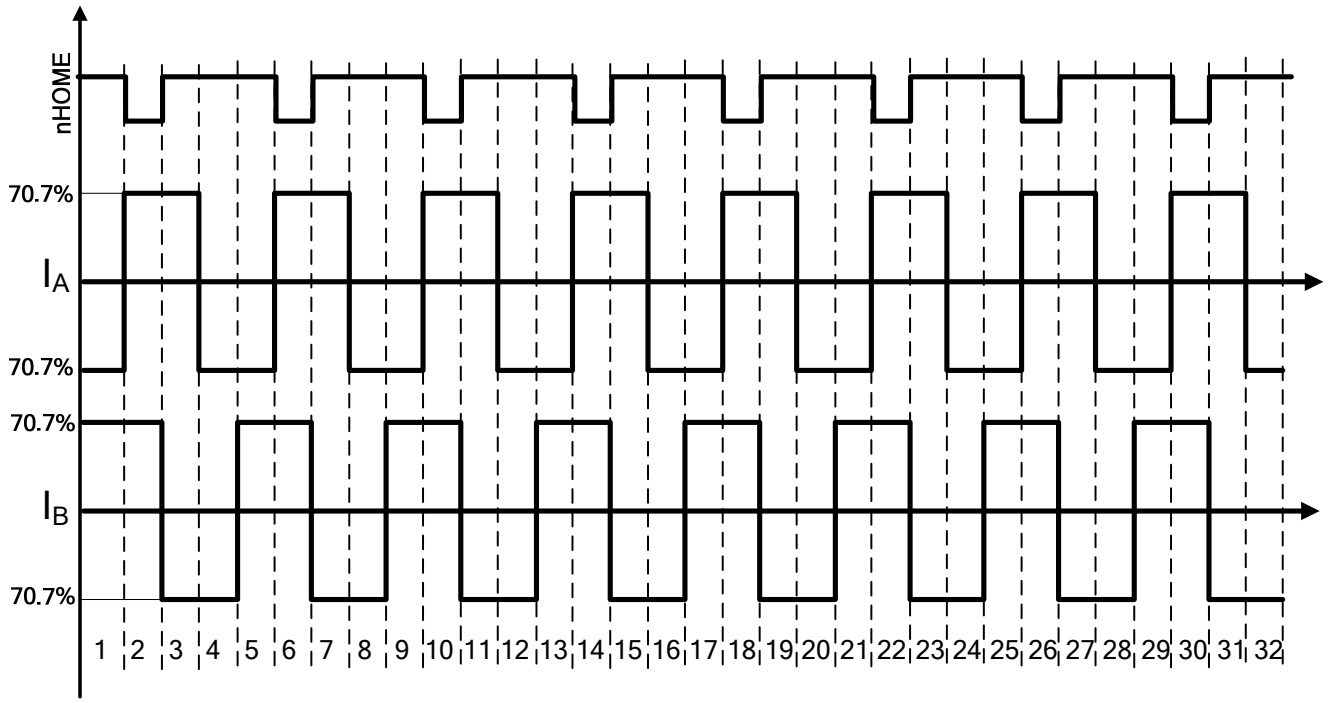


Figure 3a: Full Step (4 Step Sequences)

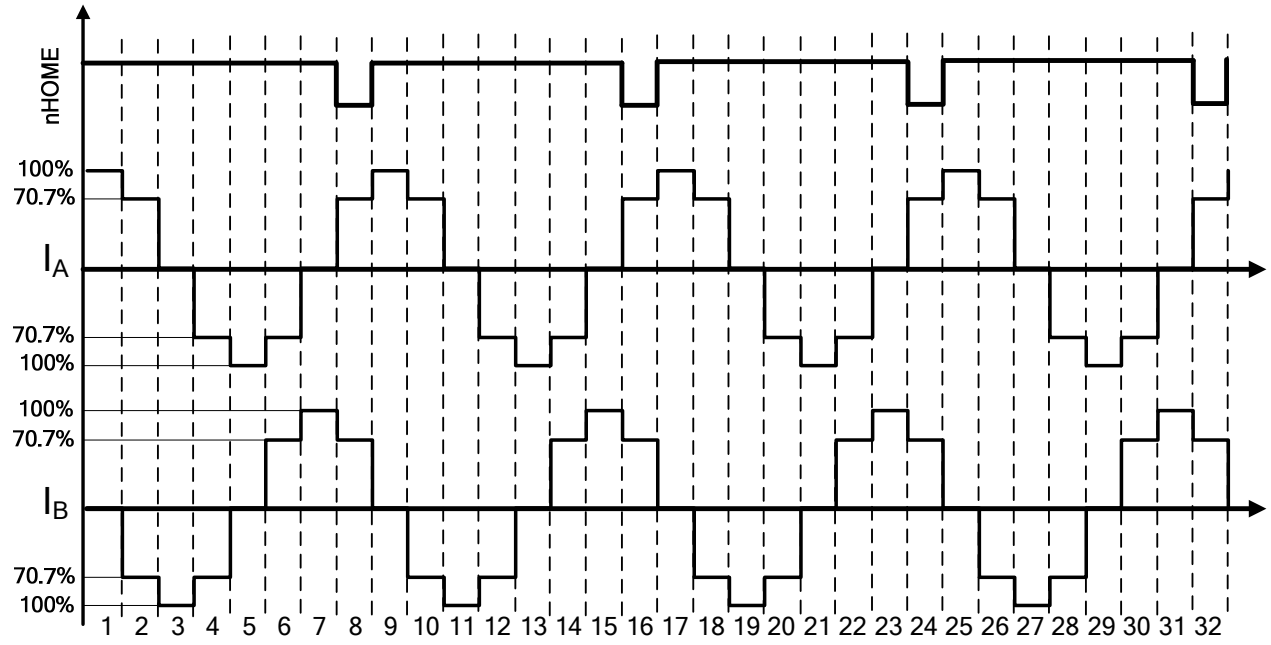


Figure 3b: Half Step (8 Step Sequences)

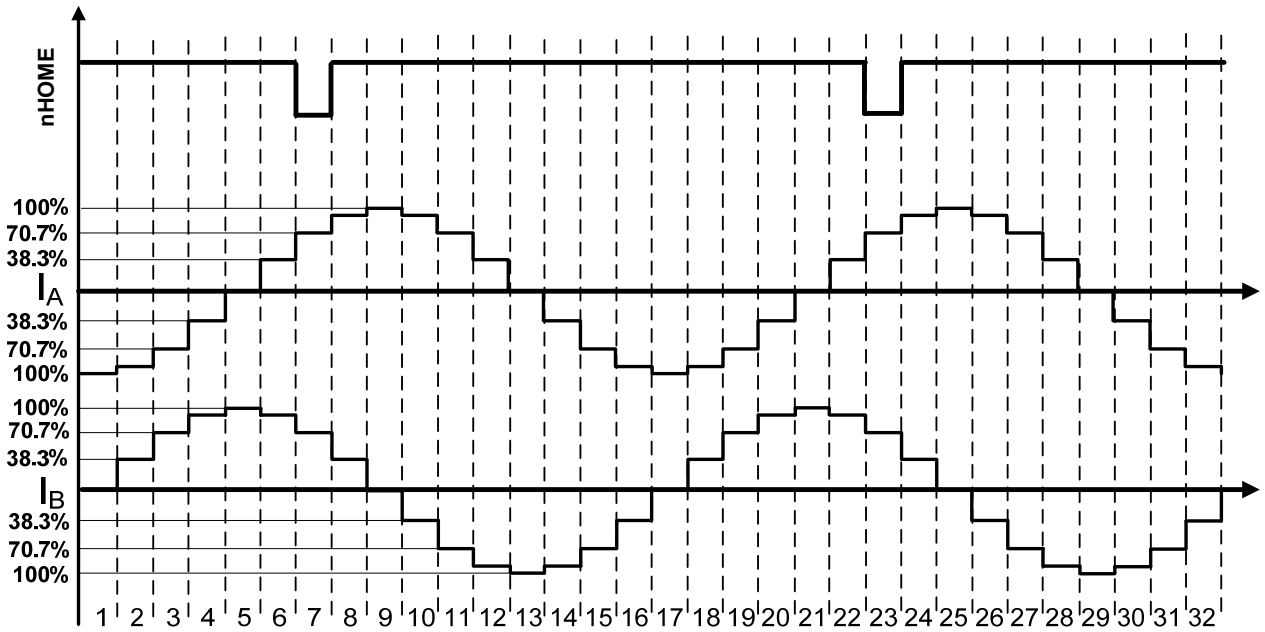


Figure 3c: Quarter Step (16 Step)

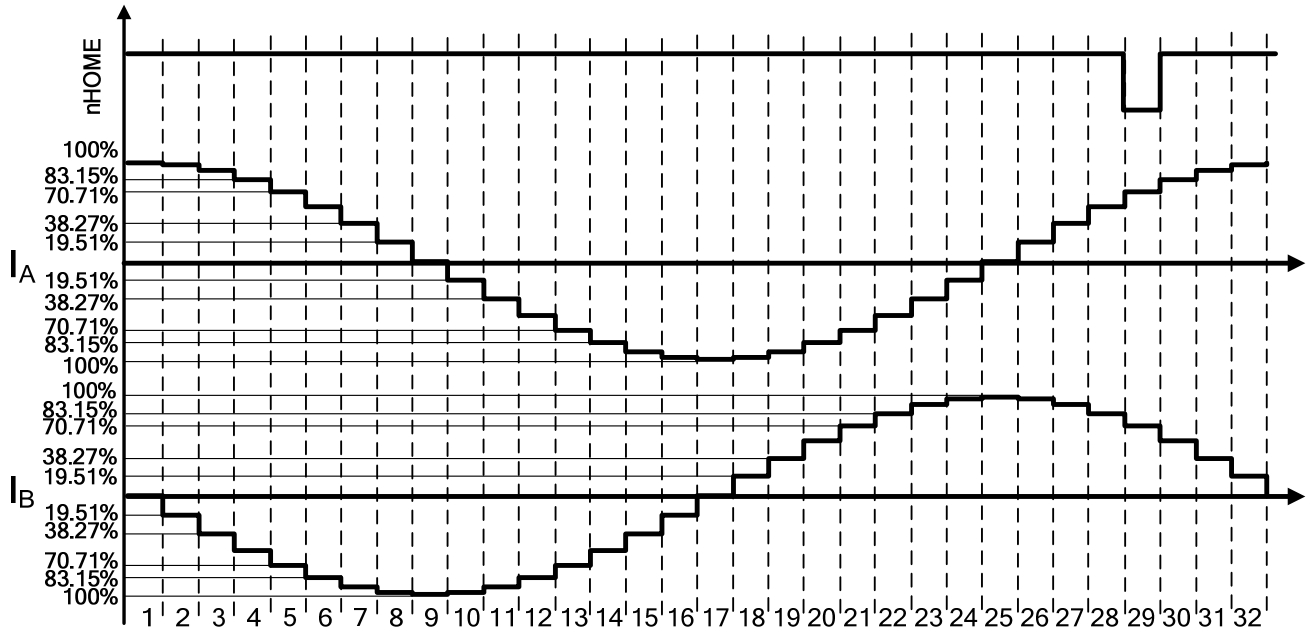
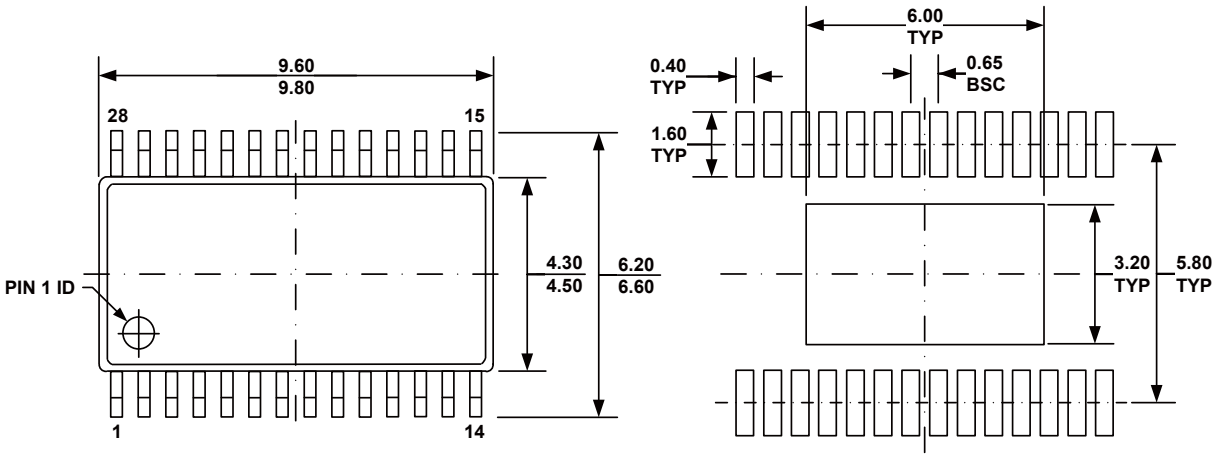


Figure 3d: Eighth Step (32 Step)

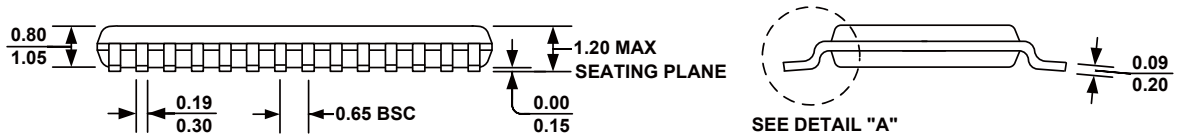
PACKAGE INFORMATION

TSSOP-28 EP (EXPOSED PAD)



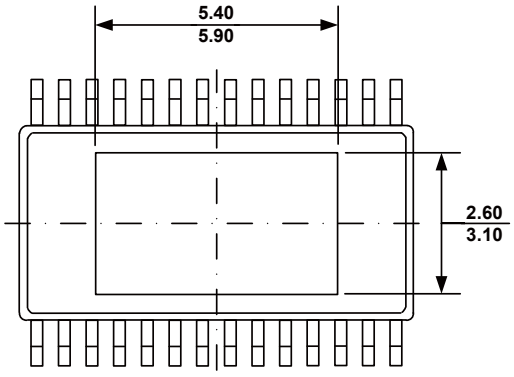
TOP VIEW

RECOMMENDED LAND PATTERN

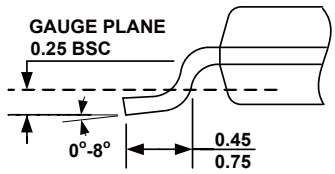


FRONT VIEW

SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.