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MP8869W

3V - 18V, 12A, High-Efficiency, Wide-Input, Synchronous Step-Down Converter with Integrated Telemetry via I²C Interface

The Future of Analog IC Technology

DESCRIPTION

The MP8869W is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I²C control interface. It offers a fully integrated solution that achieves 12A of continuous and 15A of peak output current with excellent load and line regulation over a wide input supply range.

In the I²C control loop, the output voltage level can be controlled on-the-fly through an I²C serial interface. The voltage range can be adjusted from 0.6V to 1.55V in 7.5mV steps. Voltage slew rate, frequency, current limit, hiccup/latch-off protection, enable, and power saving mode are also selectable through the I²C interface.

Constant-on-time (COT) control operation provides fast transient response. An open-drain power good (PG) pin indicates that the output voltage is in the nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MP8869W is available in a QFN-14 (3mmx4mm) package.

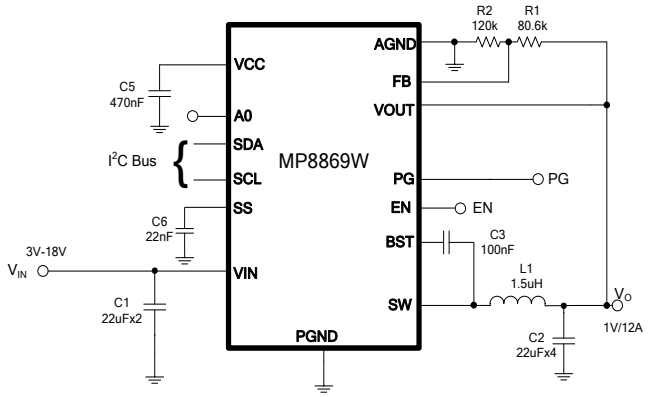
FEATURES

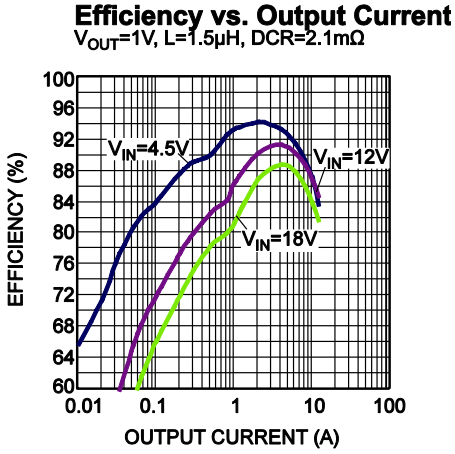
- Wide 3V to 18V Operating Input Range
- 12A Continuous/15A Peak Output Current
- 1% Internal Reference Accuracy
- I²C Programmable Output Range from 0.6V to 1.55V in 7.5mV Steps with Slew Rate Control
- 5% Accuracy Output Voltage and Output Current Monitoring via I²C
- Selectable PFM/PWM Mode, Adjustable Frequency and Current Limit through I²C
- 4 Different Selectable I²C Addresses
- External Soft Start
- Open-Drain Power Good Indication
- Output Over-Voltage Protection (OVP)
- Hiccup/Latch-Off OCP
- Available in a QFN-14 (3mmx4mm) Package

APPLICATIONS

- Solid-State Drive (SSD)
- Flat-Panel Television and Monitors
- Digital Set-Top Boxes
- Distributed Power Systems
- Networking/Server

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8869WGL	QFN-14 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP8869WGL–Z)

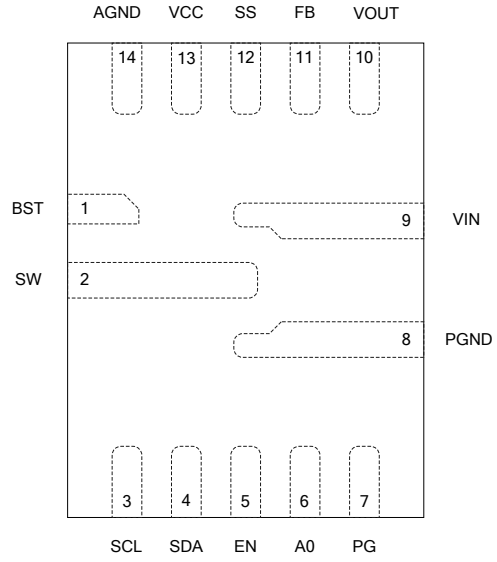
TOP MARKING

MPYW
8869
WLLL

MP: Product code of MP8869WGL
Y: Year code
W: Lot number
8869W: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-14 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 19V
V_{SW} ..... -0.6V (-7V for <10ns) to V_{IN} + 0.7V (25V for <25ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 18V
V_{OUT} 7V
All other pins ..... -0.3V to 4V
Continuous power dissipation (T_A = +25°C) **(2)**
QFN-14 (3mmx4mm) 2.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3V to 18V
Output voltage (V_{OUT}) ... 0.6V to 5.5V for FB loop and 0.6V to 1.55V for I^2C loop
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4) θJA θJC

	θJA	θJC	
QFN-14 (3mmx4mm)	48	11 ...	°C/W

NOTES:

1. Exceeding these ratings may damage the device.
2. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3. The device is not guaranteed to function outside of its operating conditions.
4. Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C(5), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		2.1	4	μA
Supply current (quiescent)	I_q	No switching, FB = 105% Vref, PFM mode		420	600	μA
HS switch on resistance	$HS_{RDS(ON)}$	$V_{BST - SW}$ =3.3V		15		mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 3.3V		4.5		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V, T_J = +25°C			1	μA
Low-side valley current limit	I_{LIMIT_L}	Adjustable by I²C		14		A
Low-side negative current limit	I_{LIMIT_LN}	In forced PWM mode or OVP state		-3		A
Low-side ZCD threshold	I_{ZCD}	T_J = +25°C		200		mA
Switching frequency	f_{SW1}	V_{IN} = 12V, V_{OUT} = 1V	400	500	600	kHz
	f_{SW2}	V_{IN} = 12V, V_{OUT} = 5V	400	500	600	kHz
Minimum off time(6)	T_{OFF_MIN}			185		ns
Minimum on time(6)	T_{ON_MIN}	V_{OUT} = 0.6V		50		ns
Reference voltage	V_{ref}	T_J = 25°C	594	600	606	mV
		-40°C < T_J < 125°C (5)	591	600	609	
FB current	I_{FB}	V_{OUT} = 620mV		10	50	nA
A0 voltage threshold 1	V_{ADD_1}	Set I²C address 60H			0.24	VCC
A0 voltage threshold 2	V_{ADD_2}	Set I²C address 62H	0.28		0.49	VCC
A0 voltage threshold 3	V_{ADD_3}	Set I²C address 64H	0.53		0.72	VCC
A0 voltage threshold 4	V_{ADD_4}	Set I²C address 66H	0.77			VCC
A0 to GND pull-down resistor	R_{A0_PD}			2		MΩ
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN threshold hysteresis	V_{EN_HYS}			110		mV
EN to GND pull-down resistor	R_{EN}			1.5		MΩ
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		2.7	2.8	2.92	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			300		mV
Power good UV threshold rising	PGVth-Hi	Good	0.86	0.9	0.94	VOUT
Power good UV threshold falling	PGVth-Lo	Fault	0.81	0.85	0.89	VOUT
Power good OV threshold rising	PGVth-Hi	Fault	1.11	1.15	1.19	VOUT

ELECTRICAL CHARACTERISTICS *(CONTINUED)*

V_{IN} = 12V, T_J = -40°C to +125°C(5), typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good OV threshold falling	PGVth-Lo	Good	1.01	1.05	1.09	VOUT
Power good deglitch time	PGTd	I²C programmable		30		µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
OVP rising threshold	V_{OVP_Rise}	VOUT and FB	121%	125%	129%	V_{REF}
OVP falling threshold	$V_{OVP\_Falling}$	VOUT and FB	106%	110%	114%	V_{REF}
OVP delay	T_{OVP}			3.7		µs
Output pin absolute OV	V_{OVP2}		6	6.5	7	V
UVP threshold	$V_{FB\_UV\_th}$	Hiccup entry	55%	60%	65%	V_{REF}
UVP delay (6)	T_{UVP}			10		µs
Soft-start current	I_{SS}		5	7	9	µA
VCC voltage	V_{CC}			3.5		V
VCC load regulation	V_{CC_reg}	I_{CC} = 20mA			3	%
Thermal shutdown (6)	T_{TSD}			160		°C
Thermal hysteresis (6)	T_{TSD_HYS}			20		°C

NOTES:

5) Not tested in production and guaranteed by over-temperature correlation.
6) Guaranteed by design and characterization test.

I/O LEVEL CHARACTERISTICS

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	$0.3V_{CC}$	-0.5	$0.3V_{CC}$	V
High-level input voltage	V_{IH}		$0.7V_{CC}$	V_{CC} + 0.5	$0.7V_{CC}$	V_{CC} + 0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{CC} > 2V	$0.05V_{CC}$	-	$0.05V_{CC}$	-	V
		V_{CC} < 2V	$0.1V_{CC}$	-	$0.1V_{CC}$	-	
Low-level output voltage (open drain) at 3mA sink current	V_{OL}	V_{CC} > 2V	0	0.4	0	0.4	V
		V_{CC} < 2V	0	$0.2V_{CC}$	0	$0.2V_{CC}$	
Low-level output current	I_{OL}		-	3	-	3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{onL}	VOL level, IOL = 3mA	-	50	-	50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{onH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{CC} level	50	-	50	-	kΩ
Pull-up current of the SCLH current source	I_{cs}	SCLH output levels between 0.3Vcc and $0.7V_{CC}$	2	6	2	6	mA
Rise time of the SCLH or SCL signal	T_{rCL}	Output rise time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Fall time of the SCLH or SCL signal	T_{fCL}	Output fall time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rise time of SDAH signal	T_{rDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Fall time of SDAH signal	T_{fDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns

I/O LEVEL CHARACTERISTICS *(continued)*

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current each I/O pin	I_i	Input voltage between $0.1V_{CC}$ and $0.9V_{CC}$	-	10	-10	+10	µA
Capacitance for each I/O pin	C_i		-	10	-	10	pF

I²C PORT SIGNAL CHARACTERISTICS

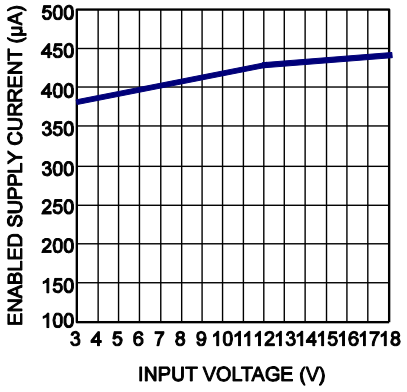
Parameter	Symbol	Condition	Cb = 100pF		Cb = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	$T_{SU;STA}$		160	-	600	-	ns
Hold time (repeated) start condition	$T_{HD;STA}$		160	-	600	-	ns
Low period of the SCL clock	T_{LOW}		160	-	1300	-	ns
High period of the SCL clock	T_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
Rise time of SCLH signal	T_{rCL}		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	T_{fCL1}		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Fall time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-up time for stop condition	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between a stop and start condition	T_{BUF}		160	-	1300	-	ns
Data valid time	$T_{VD;DAT}$		-	16	-	90	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Capacitive load for each bus line	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	-	400	-	400	pF
Noise margin at the low level	C_i	For each connected device	-	$0.1V_{CC}$	$0.1V_{CC}$	-	V
Noise margin at the high level	V_{nH}	For each connected device	-	$0.2V_{CC}$	$0.2V_{CC}$	-	V

NOTE:
V_{CC} is the I²C bus voltage, 1.8V to 3.6V range, and used for 1.8V, 2.5V, and 3.3V bus voltage.

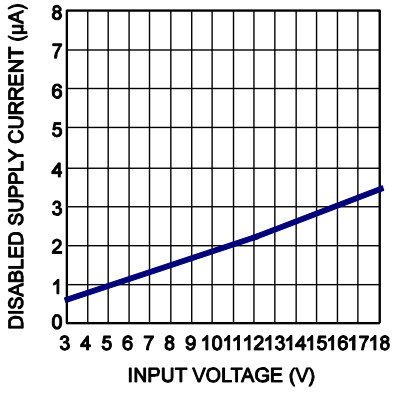
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

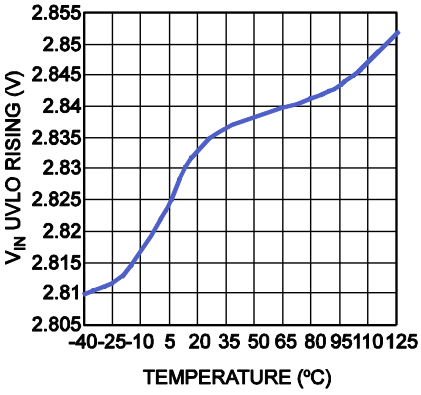
Enabled Supply Current vs. Input Voltage



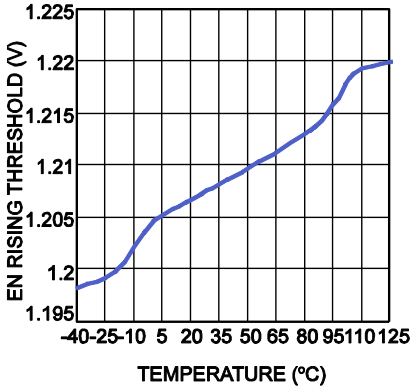
Disabled Supply Current vs. Input Voltage



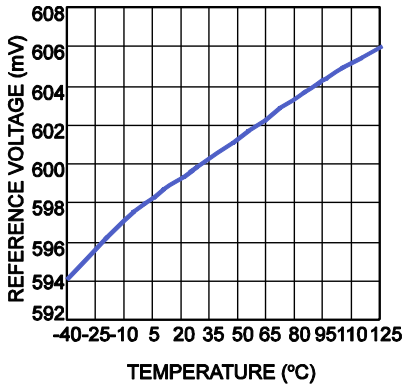
V_{IN} UVLO Rising vs. Temperature



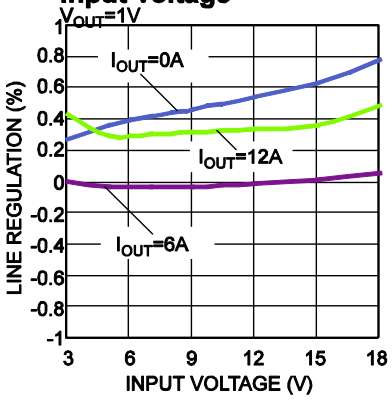
EN Rising Threshold vs. Temperature



Reference Voltage vs. Temperature

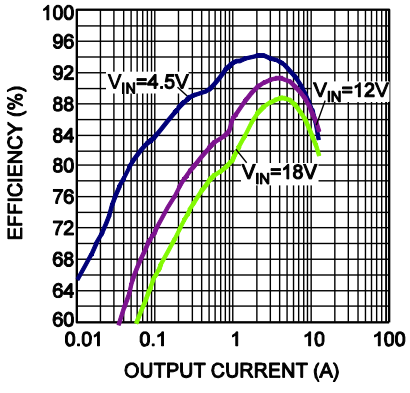


Line Regulation vs. Input Voltage



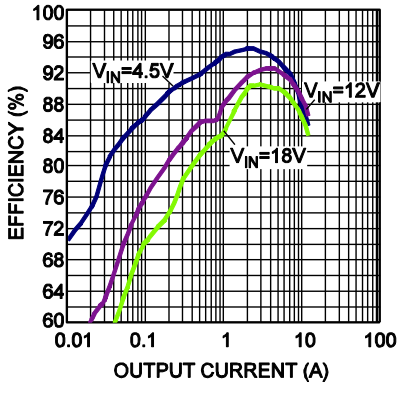
Efficiency vs. Output Current

V_{OUT}=1V, L=1.5µH, DCR=2.1mΩ



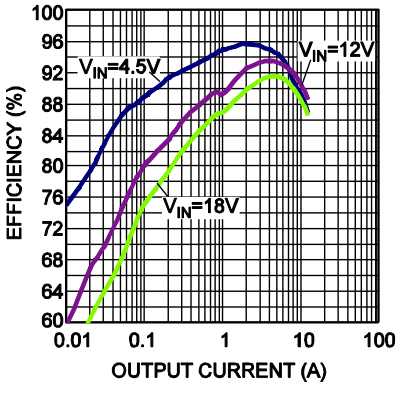
Efficiency vs. Output Current

V_{OUT}=1.2V, L=1.5µH, DCR=2.1mΩ



Efficiency vs. Output Current

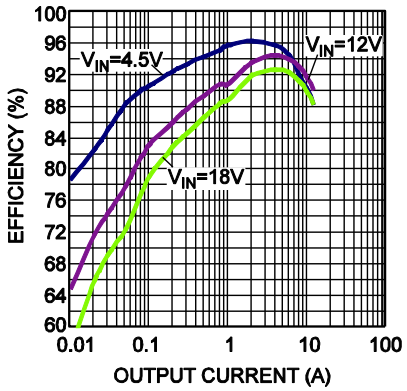
V_{OUT}=1.5V, L=1.5µH, DCR=2.1mΩ



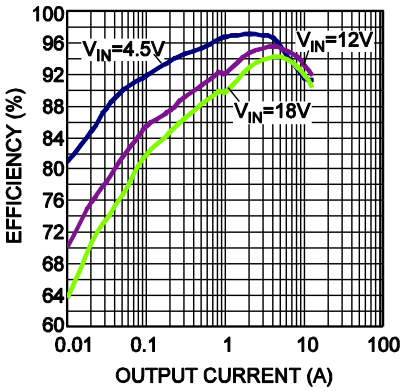
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

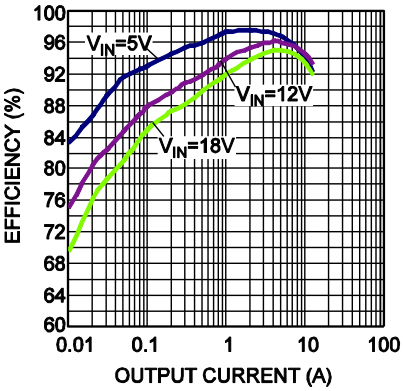
Efficiency vs. Output Current
V_{OUT}=1.8V, L=1.5µH, DCR=2.1mΩ



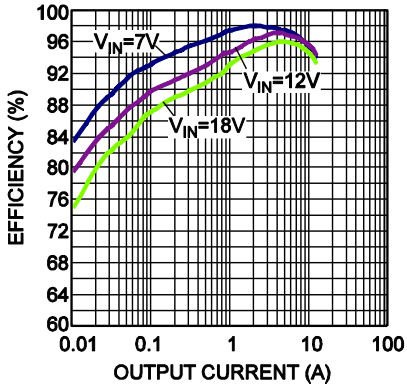
Efficiency vs. Output Current
V_{OUT}=2.5V, L=2.2µH, DCR=3mΩ



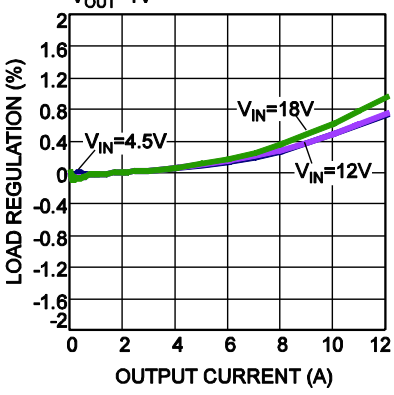
Efficiency vs. Output Current
V_{OUT}=3.3V, L=2.2µH, DCR=3mΩ



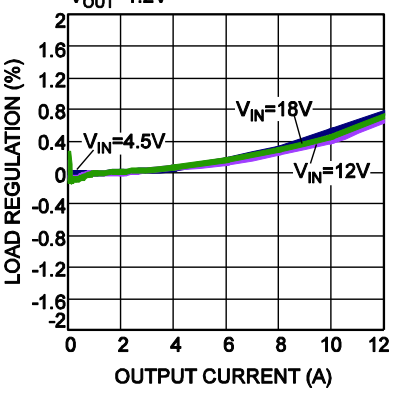
Efficiency vs. Output Current
V_{OUT}=5V, L=3.3µH, DCR=4.4mΩ



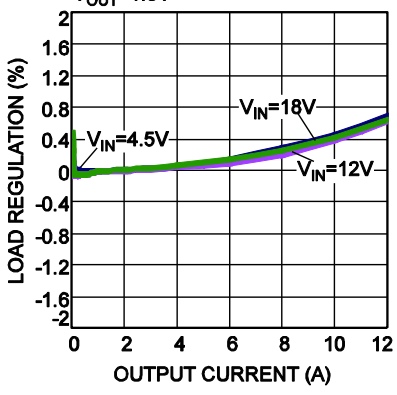
Load Regulation vs. Output Current
V_{OUT}=1V



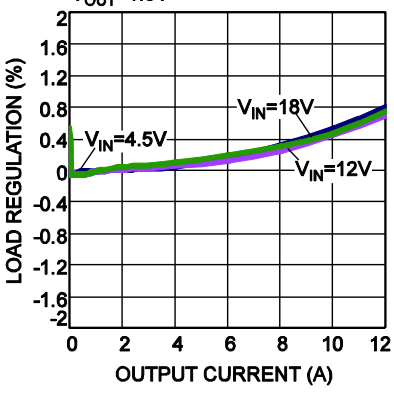
Load Regulation vs. Output Current
V_{OUT}=1.2V



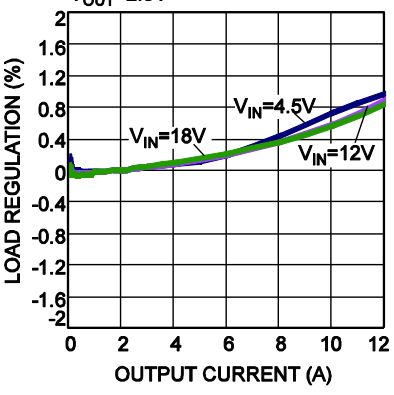
Load Regulation vs. Output Current
V_{OUT}=1.5V



Load Regulation vs. Output Current
V_{OUT}=1.8V



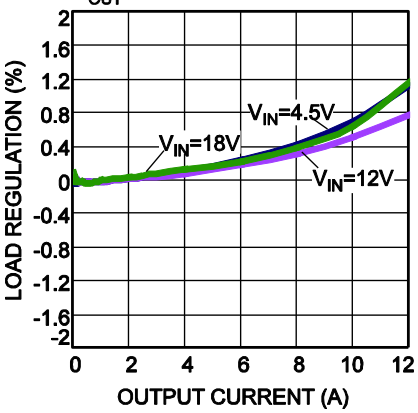
Load Regulation vs. Output Current
V_{OUT}=2.5V



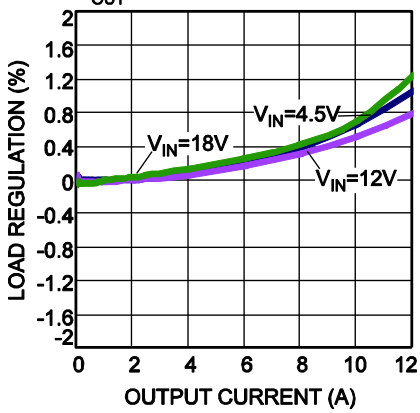
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

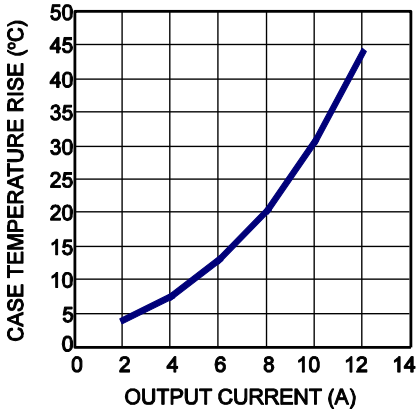
Load Regulation vs. Output Current
V_{OUT}=3.3V



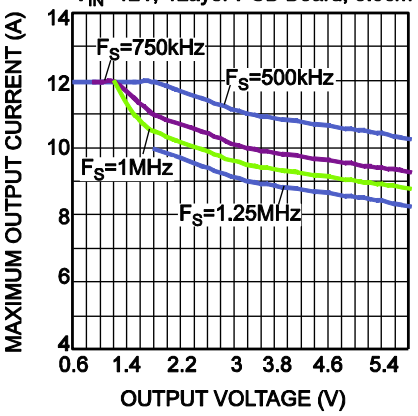
Load Regulation vs. Output Current
V_{OUT}=5V



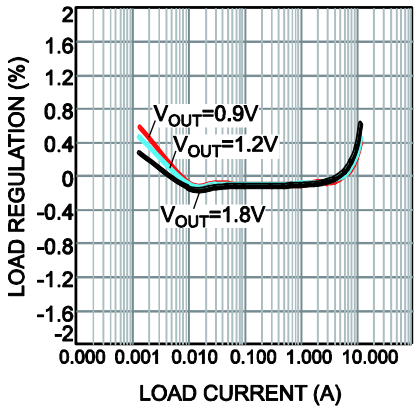
Case Temperature Rise vs. Output Current



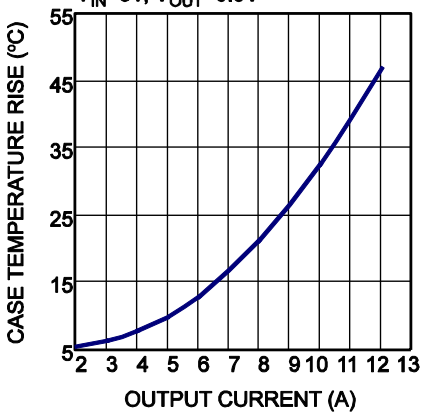
Output Current Derating vs. Frequency and Output Voltage
V_{IN}=12V, 4Layer PCB Board, 8.5cm x 8.5cm



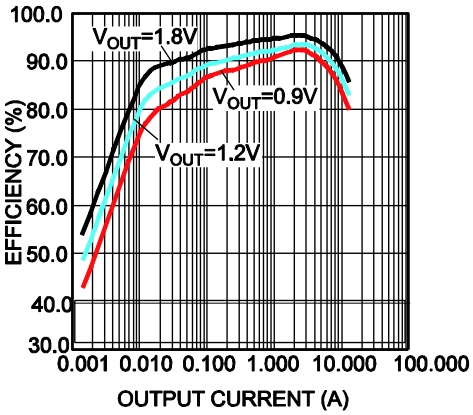
Load Regulation (%)
V_{IN}=3V, V_{OUT}=0.9V



Case Temperature Rise vs. Output Current
V_{IN}=3V, V_{OUT}=0.9V



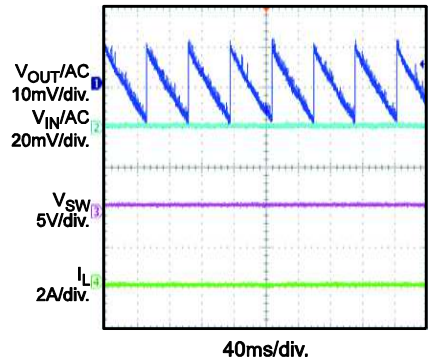
Efficiency Curve
V_{IN}=3V, V_{OUT}=0.9V



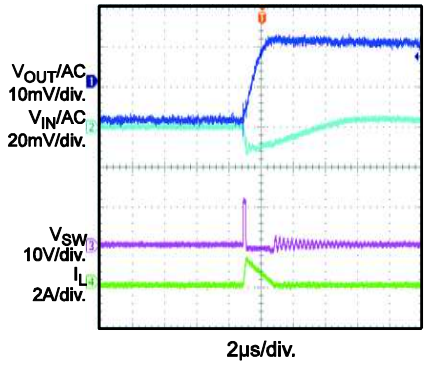
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

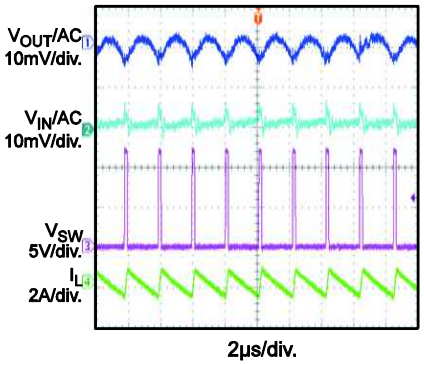
Input/Output Ripple
I_{OUT} = 0A



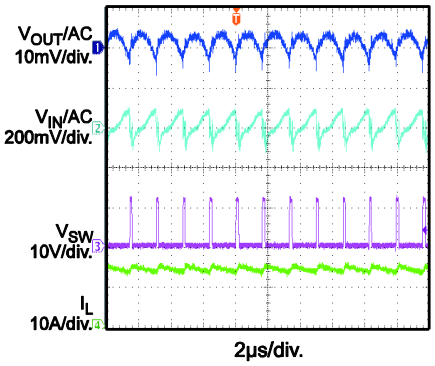
Input/Output Ripple
I_{OUT} = 0A



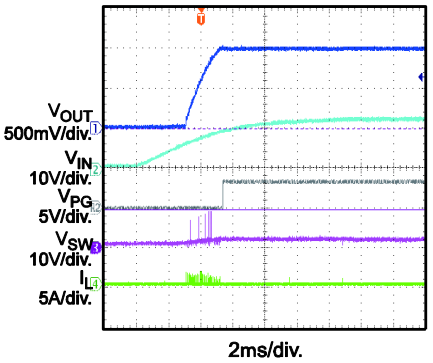
Input/Output Ripple
I_{OUT} = 0A, Forced PWM Mode



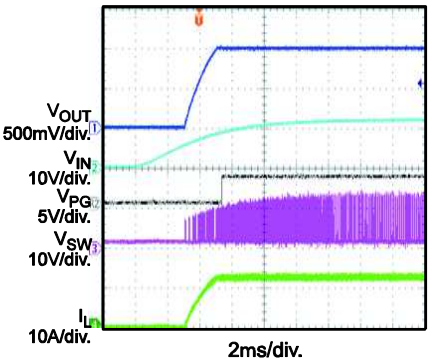
Input/Output Ripple
I_{OUT} = 12A



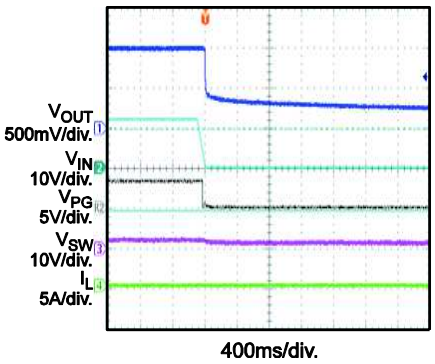
Start-Up through Input Voltage
I_{OUT} = 0A



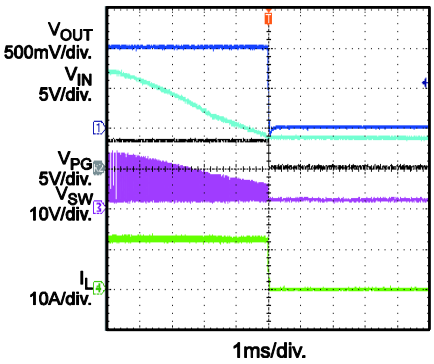
Start-Up through Input Voltage
I_{OUT} = 12A



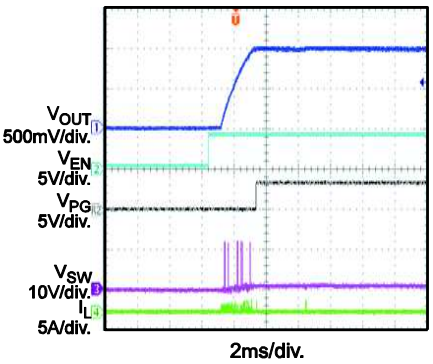
Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 12A



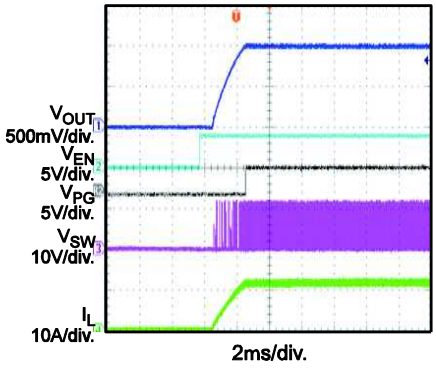
Start-Up through EN
I_{OUT} = 0A



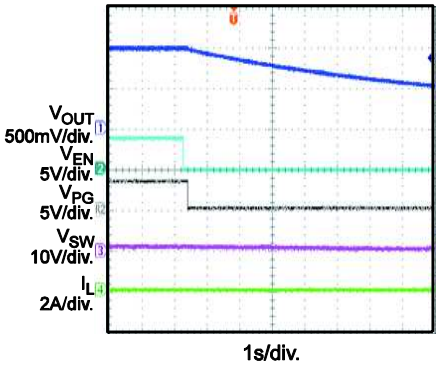
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

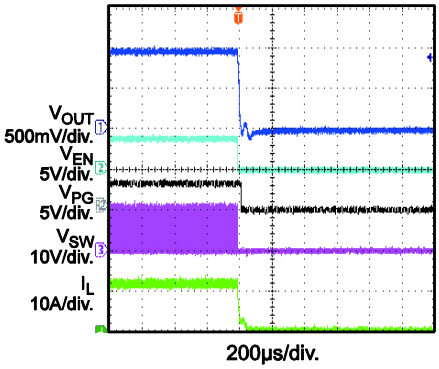
Start-Up through EN
I_{OUT} = 12A



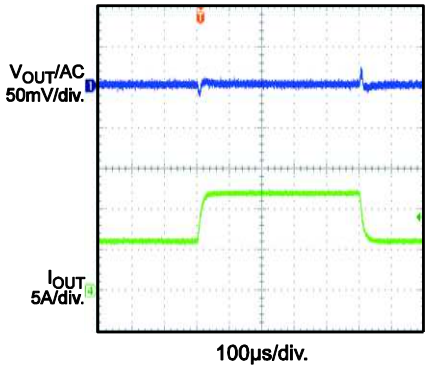
Shutdown through EN
I_{OUT} = 0A



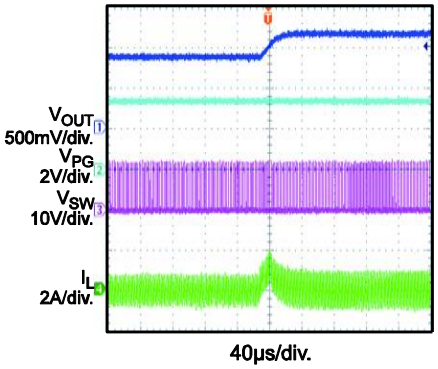
Shutdown through EN
I_{OUT} = 12A



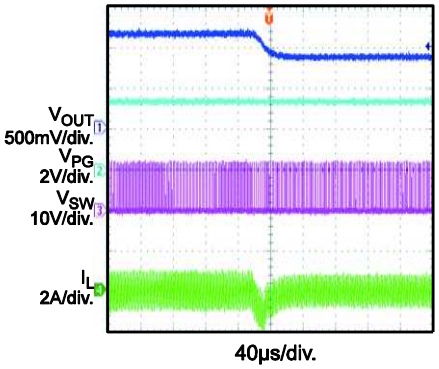
Load Transient
I_{OUT} = 6A-12A



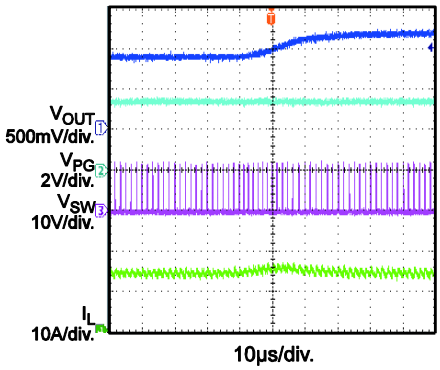
I^2C Control Slew Rate
I_{OUT}=0A, Slew Rate=20mV/µs,
PWM Mode, Output from 0.9V to 1.2V



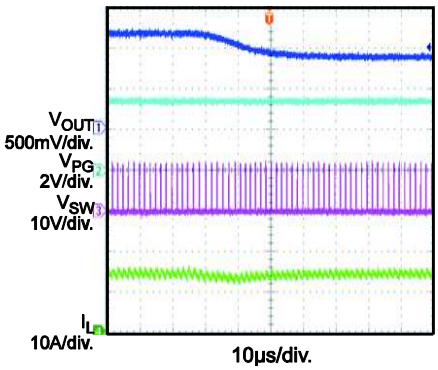
I^2C Control Slew Rate
I_{OUT}=0A, Slew Rate=20mV/µs,
PWM Mode, Output from 1.2V to 0.9V



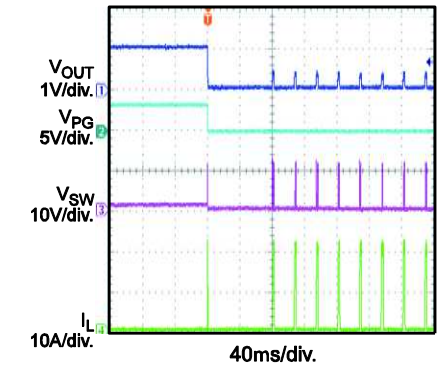
I^2C Control Slew Rate
I_{OUT}=12A, Slew Rate=20mV/µs,
PWM Mode, Output from 0.9V to 1.2V



I^2C Control Slew Rate
I_{OUT}=12A, Slew Rate=20mV/µs,
PWM Mode, Output from 1.2V to 0.9V



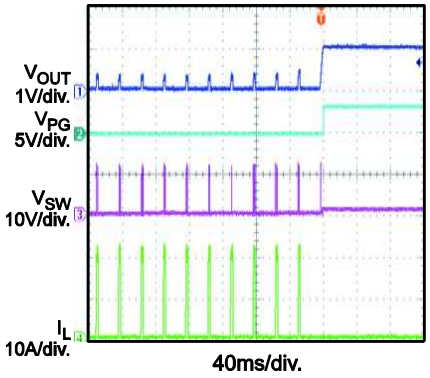
Short-Circuit Protection Entry
I_{OUT} = 0A



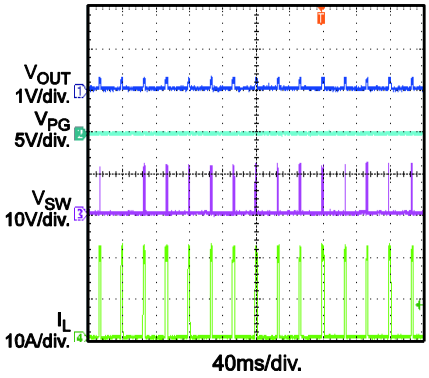
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

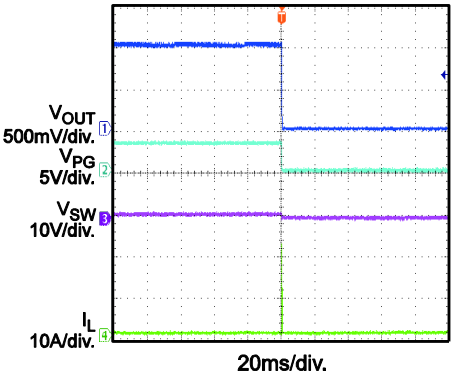
Short-Circuit Protection Recovery
I_{OUT} = 0A



Short-Circuit Protection Steady State
Short Output to GND



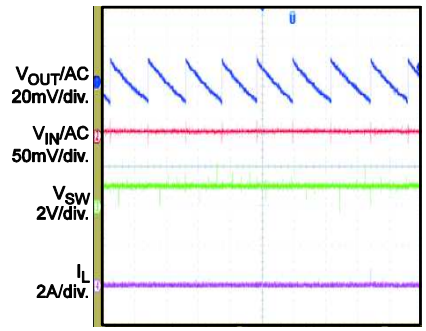
Short-Circuit Protection Entry, Latch Off Mode
I_{OUT}=0A



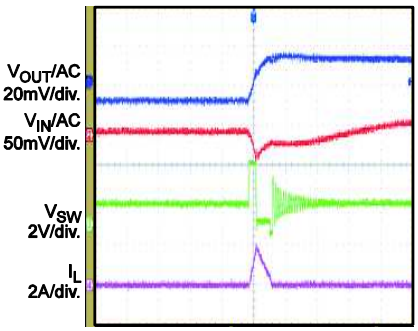
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are tested on the evaluation board.
V_{IN} = 3V, V_{OUT} = 0.9V, L = 0.47µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

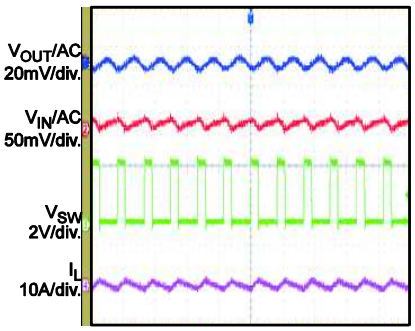
Input/Output Ripple
I_{OUT} = 0A



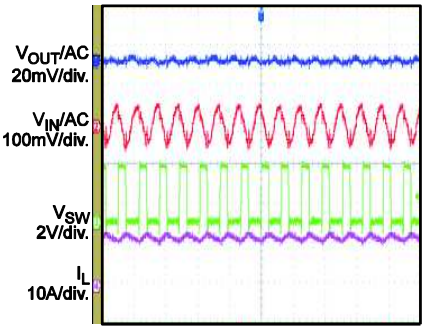
Input/Output Ripple
I_{OUT} = 0A



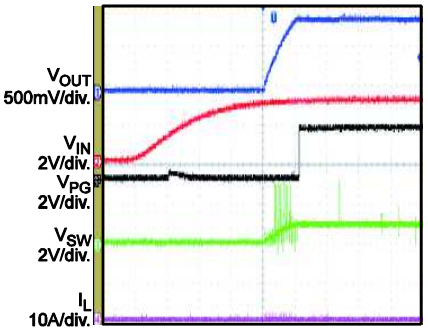
Input/Output Ripple
I_{OUT} = 0A, Forced PWM Mode



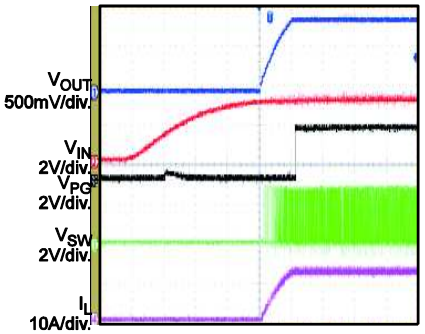
Input/Output Ripple
I_{OUT} = 12A



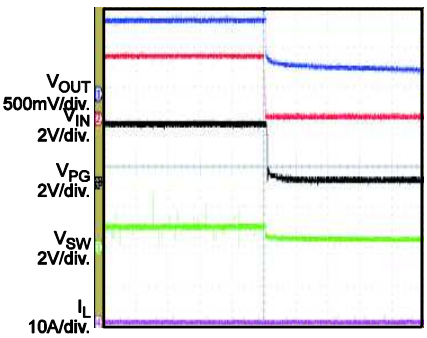
Start-Up through Input Voltage
I_{OUT} = 0A



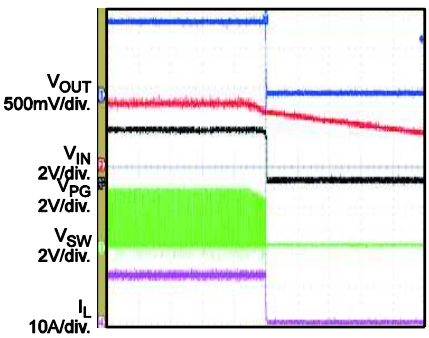
Start-Up through Input Voltage
I_{OUT} = 12A



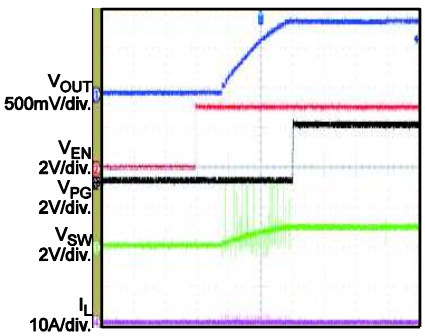
Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 12A



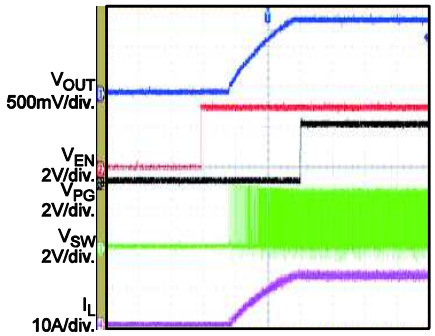
Start-Up through EN
I_{OUT} = 0A



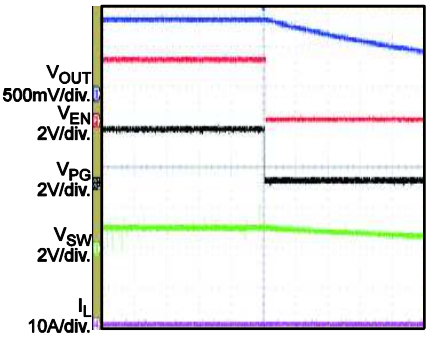
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are tested on the evaluation board.
V_{IN} = 3V, V_{OUT} = 0.9V, L = 0.47µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

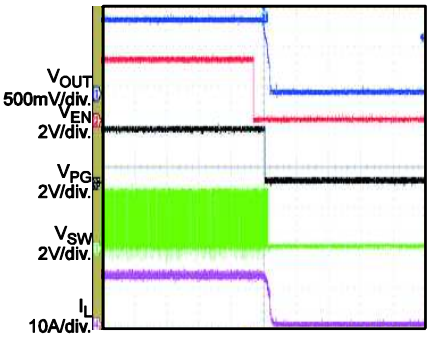
Start-Up through EN
I_{OUT} = 12A



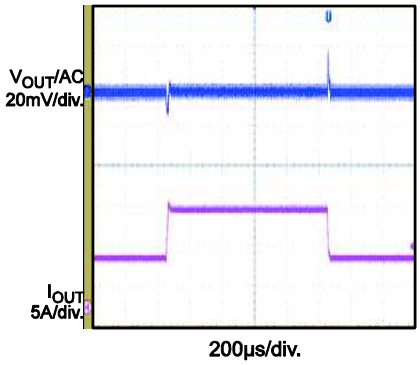
Shutdown through EN
I_{OUT} = 0A



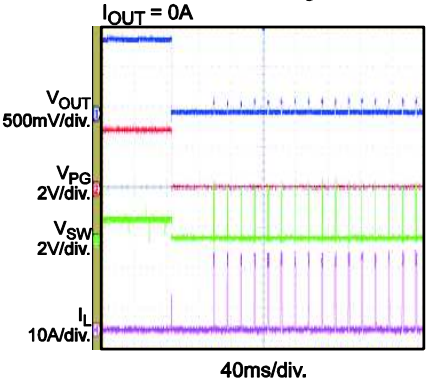
Shutdown through EN
I_{OUT} = 12A



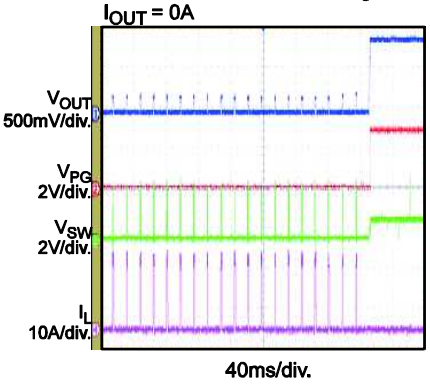
Load Transient
I_{OUT} = 6A-12A



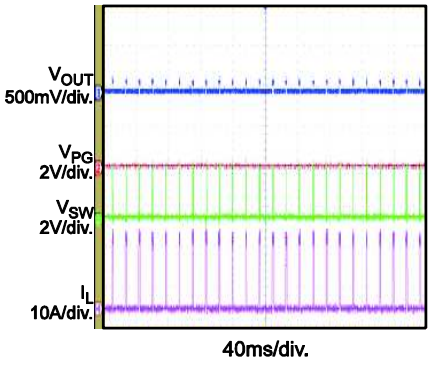
Short-Circuit Protection Entry
I_{OUT} = 0A



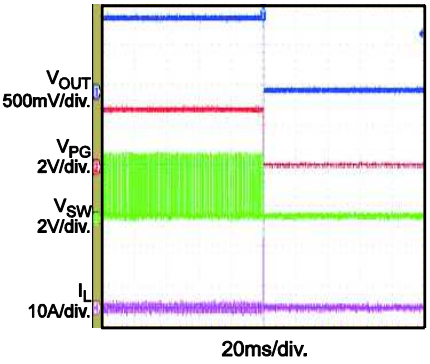
Short-Circuit Protection Recovery
I_{OUT} = 0A



Short-Circuit Protection Steady State
Short Output to GND



Short-Circuit Protection Entry, Latch Off Mode
I_{OUT}=0A



PIN FUNCTIONS

QFN-14 Pin#	Name	Description
1	BST	**Bootstrap**. A capacitor is required between SW and BST to form a floating supply across the high-side switch driver.
2	SW	**Switch output**. Connect SW using a wide PCB trace.
3	SCL	**I²C serial clock**.
4	SDA	**I²C serial data**.
5	EN	**Enable.** Set EN high to enable the MP8869W. EN has a 1.5MΩ internal pull-down resistor to GND. EN is a high-voltage pin, so it can be connected to VIN directly for auto start-up.
6	A0	**I²C address set-up**. Connect a resistor divider from VCC to A0 to set different I²C addresses.
7	PG	**Power good indication.** PG is an open-drain structure. PG is de-asserted if the output voltage is out of the regulation window.
8	PGND	**System power ground.** PGND is the reference ground of the regulated output voltage and requires special consideration during PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MP8869W operates from a 3V-to-18V input rail. Decouple the input rail with a ceramic capacitor. Connect VIN using a wide PCB trace.
10	VOUT	**Output voltage sense.** Connect VOUT to the positive terminal of the load.
11	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage before the I²C takes control.
12	SS	**Soft-start set-up.** Connect a capacitor from SS to ground to set the soft-start time.
13	VCC	**Internal LDO regulator output.** Decouple VCC with a 0.47µF capacitor.
14	AGND	**Signal ground.** If AGND is not connected to PGND internally, ensure that AGND is connected to PGND during the PCB layout.

BLOCK DIAGRAM

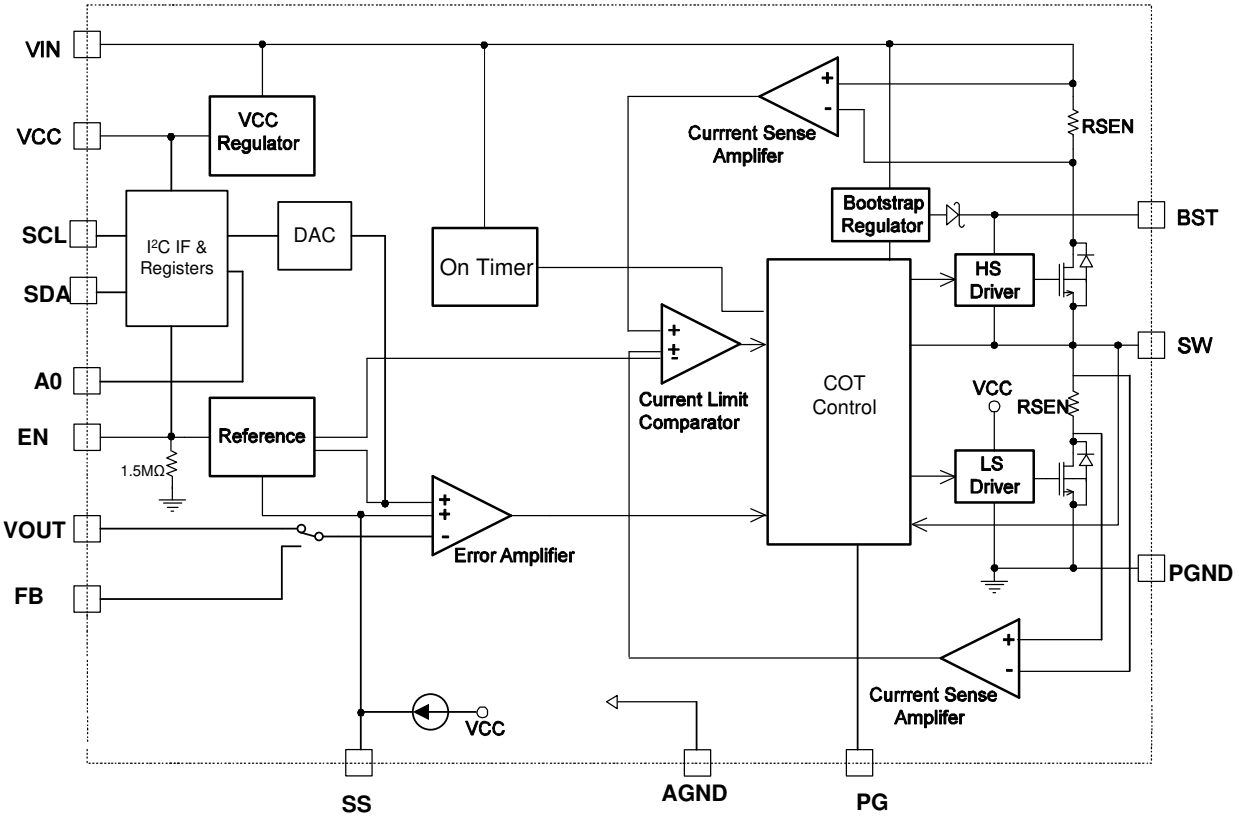


Figure 1: Functional Block Diagram

OPERATION

PWM Operation

The MP8869W is a fully-integrated, synchronous, rectified, step-down, switch-mode converter. The MP8869W uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. Figure 2 shows the simplified ramp compensation block. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{Ramp}) is lower than the error amplifier output voltage (V_{EAO}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET enters the off state. By cycling the HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are turned on at the same time, causing a dead short between input and GND and reducing efficiency dramatically. The MP8869W prevents this by generating a dead-time (DT) internally between when the HS-FET is off and the LS-FET is on, and when the LS-FET is off and the HS-FET is on. The device enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

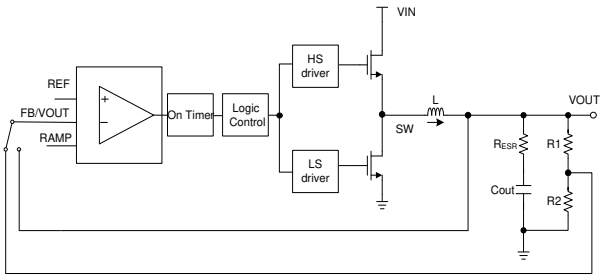


Figure 2: Simplified Compensation Block

Switching Frequency

The MP8869W uses constant-on-time (COT) control, so there is no dedicated oscillator in the IC. The input voltage is fed into the on-time one-shot timer through the internal frequency resistor. The duty ratio is VOUT/VIN, and the switching frequency is fairly constant over the input voltage range.

The MP8869W's switching frequency can be adjusted by setting the two bits D[5:4] in register 02 through I^2C communication. When the output voltage setting is low, and the input voltage is high, the switching on-time may be limited by the internal minimum on-time limit, and switching frequency decreases. Table 1 shows the maximum switching frequency vs. the output voltage when VIN = 12V and VIN = 5V.

Table 1: Maximum Frequency Selecting vs. Output Voltage

	Maximum Frequency Selecting	
Vo (V)	VIN = 12V	VIN = 5V
5	1.25MHz	/
3.3	1.25MHz	1.25MHz
2.5	1.25MHz	1.25MHz
1.8	1.25MHz	1.25MHz
1.5	1.25MHz	1.25MHz
1.2	1MHz	1.25MHz
1	750kHz	1.25MHz
0.9	750kHz	1.25MHz
0.6	500kHz	1.25MHz

Forced PWM Operation

When the MP8869W works in forced PWM mode, the MP8869W enters continuous conduction mode (CCM) where the HS-FET and LS-FET repeat the on/off operation, even if the inductor current is zero or a negative value. The switching frequency (F_{SW}) is fairly constant. Figure 3 shows the timing diagram during this operation.

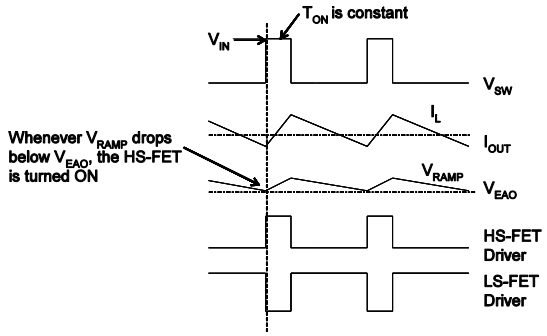


Figure 3: Forced PWM Operation

Light-Load Operation

When the MP8869W works in auto PFM/PWM mode or light-load operation, the MP8869W reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high-Z) (see Figure 4). The output capacitors discharge slowly to GND through R1 and R2. This operation improves device efficiency greatly when the output current is low.

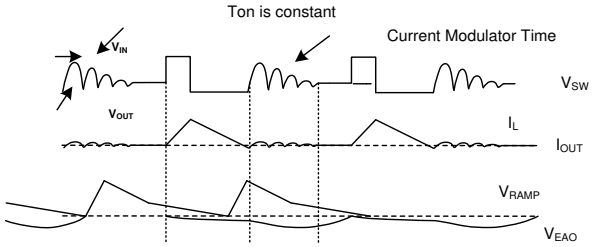


Figure 4: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently during heavy-load condition. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, the HS-FET turns on more frequently, and the switching frequency increases. The output current reaches critical levels when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MP8869W can operate in pulse frequency modulation (PFM) mode under light load to improve efficiency (low-power mode). The MP8869W can also operate in forced PWM mode at any load condition. This mode is selectable through the I²C control. To enable low-power mode, set the Mode bit to 0. To disable low-power mode, set the mode bit to 1, and the converter will work in forced PWM mode. The Mode bit is set to 0 (PFM) by default.

Operating without an External Ramp

The traditional constant-on-time control scheme is unstable intrinsically if the output capacitor's ESR is not large enough to be an effective current-sense resistor. Ceramic capacitors cannot be used as output capacitors, usually. The MP8869W has built-in, internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. The pure ceramic capacitor solution can reduce the output ripple, total BOM cost, and board area significantly.

VCC Regulator

A 3.5V internal regulator powers most of the internal circuitries. A 470nF decoupling capacitor is needed to stabilize the regulator and reduce ripple. This regulator takes the VIN input and operates in the full VIN range. After EN is pulled high, and VIN is greater than 3.5V, the output of the regulator is in full regulation. When VIN is lower than 3.5V, the output voltage decreases and follows the input voltage. A 0.47µF ceramic capacitor is required for decoupling.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage against the internal 0.6V reference (REF) for non-I²C mode and outputs a PWM modulation signal. In I²C mode, FB is opened, and VOUT is connected to the EA non-inverter input. The reference voltage can be programmed from 0.6V to 1.55V in the I²C control loop. The optimized internal ramp compensation minimizes the external component count and simplifies the control loop design.

Enable (EN)

EN is a digital control pin that turns the

regulator, including the I²C block, on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1.5MΩ resistor is connected from EN to ground. EN can operate with an 18V input voltage, which allows EN to be directly connected to VIN for automatic start-up. When the external EN is high, set the EN bit to 0 in register 01 to stop the HS-FET and LS-FET from switching. The MP8869W resumes switching by setting the EN bit to 1.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8869W UVLO comparator monitors the input voltage, VIN, and output voltage of the VCC regulator. The MP8869W is active when the voltages exceed the UVLO rising threshold.

Soft-Start (SS) and Pre-Bias Start-Up

The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V to VCC. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

The approximate typical soft-start time can be calculated with Equation (2):

$$t_{ss}(ms) = \frac{V_{ref}(V) \times C_{ss}(nF)}{7\mu A} \quad (2)$$

Where V_{ref} is reference voltage of the FB loop or I²C loop.

If the output of the MP8869W is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the sensed output voltage at FB or VOUT(7).

NOTE:

V_BOOT = 1, sense FB voltage. V_BOOT = 0, sense VOUT voltage.

The MP8869W also provides a selectable soft-stop function which defines the output discharge behavior after EN shutdown. By default, the output is not controlled after EN shutdown. If setting the soft-stop control bit D[3] to 1 in register 02 via the I²C, the output is discharged linearly to zero in a quarter of the soft-start time.

Over-Current-Protection (OCP)

The MP8869W has a default, hiccup, cycle-by-cycle, over-current limiting control. The current-limit circuit employs both high-side current limit and a low-side "valley" current-sensing algorithm. The part uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element for the valley current limit. If the magnitude of the high-side current-sense signal is above the current-limit threshold, the PWM on pulse is terminated, and the LS-FET is turned on. Afterward, the inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET. PWM is not allowed to initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle over-current limit occurs, the output voltage drops until VOUT is below the under-voltage (UV) threshold, typically 60% below the reference. Once UV is triggered, the MP8869W enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The MP8869W exits hiccup mode once the over-current condition is removed.

Short the output to ground first, and then power on the part. The MP8869W's I²C is disabled in this condition. The I²C resumes operation after the short circuit is removed. When hiccup OCP bit D[1] in register 01 is set to 0 by the I²C, a latch-off occurs if OCP is triggered, and FB UVP is triggered.

POWER GOOD (PG)

The power good (PG) indicates whether the output voltage is in the normal range compared to the internal reference voltage. PG is an open-drain structure. An external pull-up supply is required. During power-up, the PG output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce in-rush current at start-up.

When the output voltage is higher than 90% and lower than 115% of the internal reference voltage, and the soft start is finished, then the PG signal is pulled high. When the output voltage is lower than 85% after the soft start finishes, the PG signal remains low. When the output voltage is higher than 115% of the internal reference, PG is switched low; The PG signal rises back to high after the output voltage drops below 105% of the internal reference voltage.

PG implements an adjustable deglitch time via the I^2C whenever VOUT crosses the UV/OV rising and falling threshold. This guarantees the correct indication when the output voltage is scaled through the I^2C.

The PG output is pulled low immediately when EN UVLO, input UVLO, OCP, or OTP are triggered.

Input Over-Voltage Protection (VIN OVP)

The MP8869W monitors VIN to detect an input over-voltage event. This function is active only when the output is in OV or soft-stop condition. When the output is in OVP state, or soft stop is enabled, output discharge is enabled to charge the input voltage high. When the input voltage exceeds the input OVP threshold, both the HS-FET and LS-FET stop switching.

Output Over-Voltage Protection (OVP)

The MP8869W monitors both FB and VOUT to detect an over-voltage event. When setting the V_BOOT bit to 1, an internal comparator monitors FB. When setting the V_BOOT bit to 0, the internal comparator monitors VOUT. When the FB or VOUT voltage becomes higher than 125% of the internal reference voltage, the controller enters dynamic regulation mode, and the input voltage may be charged up during this time. When input OVP is triggered, the IC stops switching. If OVP mode is set to “Auto Retry” in the I^2C, the IC begins switching once the input voltage drops below the VIN OVP recover threshold. Otherwise, the MP8869W latches off. OVP auto-retry mode or latch-off mode occurs only if the soft start has finished.

Dynamic regulation mode can be operated by turning on the low side until the low-side negative current limit is triggered. Then the body diode of the HS-FET free-wheels the current.

The output power charges the input, which may trigger the VIN OVP function. In VIN OVP, neither the HS-FET or LS-FET turn on and stop charging VIN. If the output is still over-voltage and the input voltage drops below the VIN OVP threshold, repeat the operation. If the output voltage is below 110% of the internal reference voltage, then output OVP is exited.

Output Absolute Over-Voltage Protection (OVP_ABS)

The MP8869W monitors the VOUT voltage to detect absolute over-voltage protection. When VOUT is larger than 6.5V, the controller enters dynamic regulation mode if the OVP retry bit is set to 1 in the I^2C register 01. Otherwise, the MP8869W latches off when output OVP and input OVP are both triggered. Absolute over-voltage protection works once both the input voltage and EN are higher than their rising thresholds. This means that this function can work even during a soft start.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 160°C, the entire chip shuts down. When the temperature is less than its lower threshold (typically 140°C), the chip is enabled again.

The D[1] and D[2] bits can be monitored in register 06 for more information about IC silicon temperature.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO’s rising threshold is 2.4V with a 150mV hysteresis. The bootstrap capacitor voltage is regulated by VIN internally through D1, M1, C4, L1, and C2 (see Figure 5). If V_{BST} - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C4.

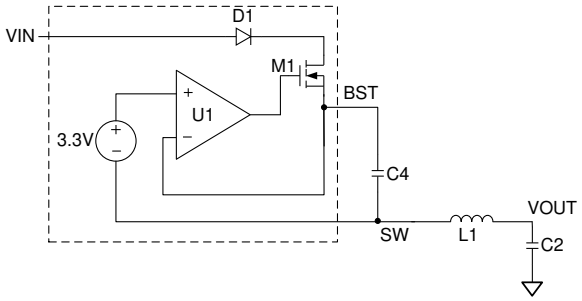


Figure 5: Internal Bootstrap Charging Circuit

START-UP AND SHUTDOWN

If VIN, VCC, and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, VIN low, VCC low, thermal shutdown, OVP latch, and OCP latch. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. V_{EAO} and the internal supply rail are then pulled down.

I²C Control and Default Output Voltage

When the MP8869W is enabled, the output voltage is determined by the FB resistors with a programmed soft-start time. After that, the I²C bus can communicate with the master. If the chip does not receive I²C communication signal continuously, it can works well through FB and performs behavior similar to a traditional non-I²C part. The output voltage is determined by the resistor dividers R1, R2, and FB reference voltage. V_{OUT} can be calculated using Equation (3):

$$Vout(V) = 0.6 \times (1 + \frac{R1}{R2}) \quad (3)$$

The FB loop V_{REF} is 0.6V. The FB loop reference voltage is a fixed value that cannot be adjusted by the I²C.

Loop Switch

There is no output slew rate control during the FB loop to the I2C loop. When the output voltage setting is much larger or smaller than the present voltage, it is recommended to take two steps to finish the loop switch and output voltage setting.

During the FB loop to the I²C loop, first set the output voltage in the I²C loop to the present output voltage, and then set V_BOOT = 0 to switch the FB loop to the I²C loop. Second, change the output voltage to the target with slew rate control in the I²C loop. Please refer to the Output Voltage Dynamic Scaling section on page 30 for details.

In the I²C control loop, the output voltage is determined by the I²C control, and the FB feedback loop is disabled. After the MP8869W receives a valid data byte of the output voltage setting, the MP8869W adjusts the DAC output as the reference voltage with a controlled slew rate. The slew rate is determined by three bits D[5:3] in register 01.

I²C Slave Address

To support multiple devices used on the same I²C bus, A0 can be used to select four different addresses. A resistor divider from VCC to GND can achieve an accurate reference voltage. Connect A0 to this reference voltage to set a different I²C slave address (see Figure 6). The internal circuit changes the I²C address accordingly. When the master sends an 8-bit address value, the 7-bit I²C address should be followed by 0/1 to indicate a write/read operation. Table 2 shows the recommended I²C address selection by the A0 voltage.

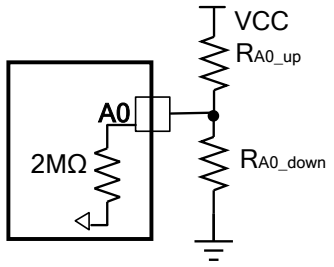


Figure 6: I²C Slave Address Selection Set-Up

Table 2: Recommended I²C Slave Address Selection by A0 Resistor Divider

A0 Upper Resistor R_{A0_up}(kΩ)	A0 Lower Resistor R_{A0_down}(kΩ)	I²C Slave Address	
		Binary	Hex
No connect	No connect	110 0000	60H
500	300	110 0010	62H
300	500	110 0100	64H
100	No connect	110 0110	66H

I²C INTERFACE

I²C Serial Interface Description

The I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP8869W interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 7).

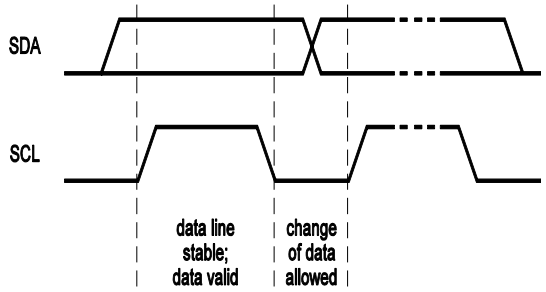


Figure 7: Bit Transfer on the I²C Bus

Start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is HIGH. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 8).

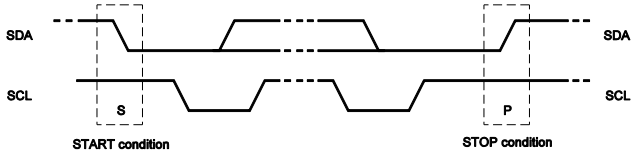


Figure 8: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition, and is considered to be free again after a minimum of 4.7μs after the stop condition. The bus remains busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be eight bits long. Each byte has to be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

Data transfers follow the format shown in Figure 9. After the start condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit data direction bit (R/W). A zero indicates a transmission (write), and a one indicates a request for data (read). A data transfer is always terminated by a stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

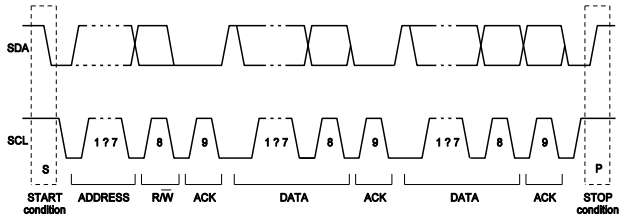
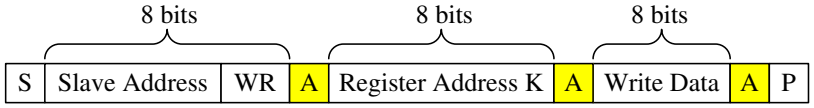


Figure 9: Complete Data Transfer

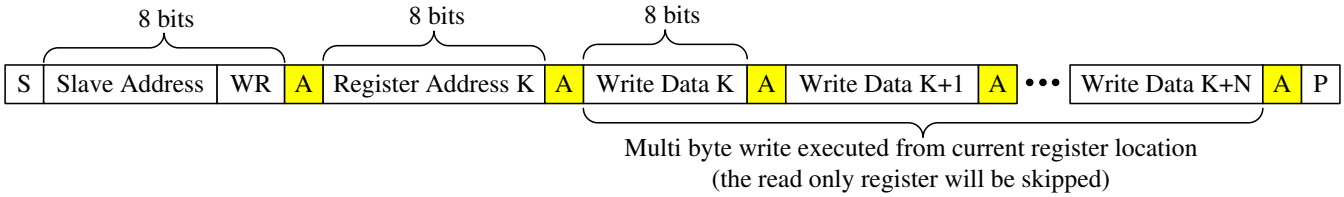
The MP8869W requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP8869W acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8869W. The MP8869W performs an update on the falling edge of the LSB byte.

I²C Write and Read Sequence Example



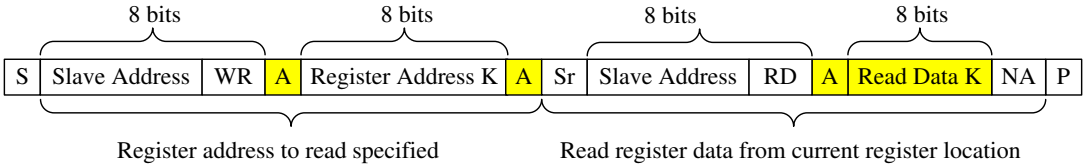
Master to Slave
Slave to Master
A = Acknowledge (SDA = LOW)
NA = NOT Acknowledge (SDA = HIGH)
S = Start Condition
P = Stop Condition
WR Write = 0
RD Read = 1

I²C Write Example --- Write Single Register



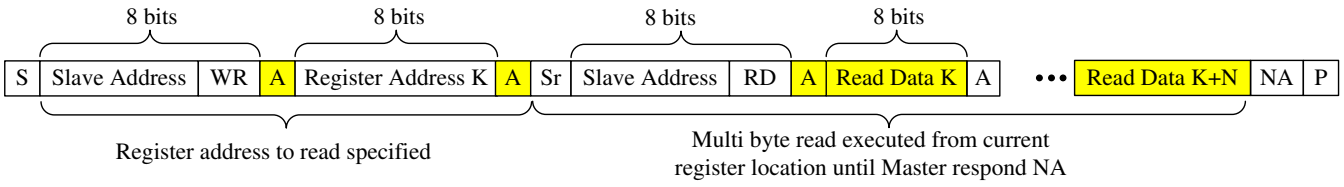
Master to Slave
Slave to Master
A = Acknowledge (SDA = LOW)
NA = NOT Acknowledge (SDA = HIGH)
S = Start Condition
P = Stop Condition
WR Write = 0
RD Read = 1

I²C Write Example --- Write Multi Register



Master to Slave
Slave to Master
A = Acknowledge (SDA = LOW)
NA = NOT Acknowledge (SDA = HIGH)
S = Start Condition
P = Stop Condition
Sr = Repeat Start Condition
WR Write = 0
RD Read = 1

I²C Read Example --- Read Single Register



Master to Slave
Slave to Master
A = Acknowledge (SDA = LOW)
NA = NOT Acknowledge (SDA = HIGH)
S = Start Condition
P = Stop Condition
Sr = Repeat Start Condition
WR Write = 0
RD Read = 1

I²C Read Example --- Read Multi Register