



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: [info@chipsmall.com](mailto:info@chipsmall.com) Web: [www.chipsmall.com](http://www.chipsmall.com)

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# 1.0 A 6.8 V H-Bridge Motor Driver IC

The 17511A is a monolithic H-Bridge designed to be used in portable electronic applications to control small DC motors or bipolar step motors. End applications include head positioners (CDROM or disk drive), camera focus motors, and camera shutter solenoids.

The 17511A can operate efficiently with supply voltages as low as 2.0V to as high as 6.8V. Its low  $R_{DS(ON)}$  H-Bridge output MOSFETs (0.46  $\Omega$  typical) can provide continuous motor drive currents of 1.0A and handle peak currents up to 3.0A. It is easily interfaced to low-cost MCUs via parallel 3.0V- or 5.0V- compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz.

This device contains an integrated charge pump and level shifter (for gate drive voltages), integrated shoot-through current protection (cross-conduction suppression logic and timing), and undervoltage detection and shutdown circuitry.

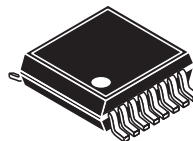
The 17511A has four operating modes: Forward, Reverse, Brake, and Tri-States (High Impedance).

## Features

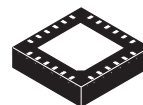
- 2.0V to 6.8V Continuous Operation
- Output Current 1.0 A(DC), 3.0A (Peak)
- MOSFETs < 600 m $\Omega$   $R_{DS(ON)}$  @ 25°C Guaranteed
- 3.0V/5.0V TTL-/CMOS-Compatible Inputs
- PWM Frequencies up to 200 kHz
- Undervoltage Shutdown
- Cross-Conduction Suppression
- Low Power Consumption
- Pb-Free Packaging Designated by Suffix Codes EV and EP

**17511A**

**H-BRIDGE MOTOR DRIVER IC**



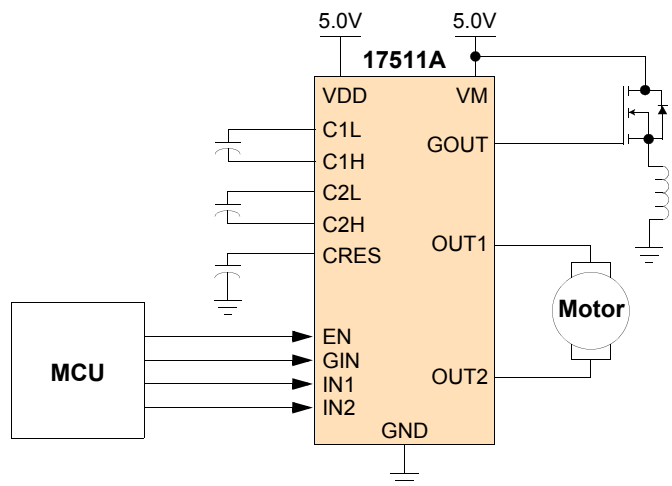
**EV SUFFIX (PB-FREE)**  
**98ASA10614D**  
**16-PIN VMFP**



**EP SUFFIX (PB-FREE)**  
**98ARL10577D**  
**24-PIN QFN**

## ORDERING INFORMATION

Device	Temperature Range (T <sub>A</sub> )	Package
MPC17511AEV	-20°C to 65°C	16 VMFP
MPC17511AEV/EL		
MPC17511AEP		24 QFN
MPC17511AEP/R2		



**Figure 1. 17511A Simplified Application Diagram**

## INTERNAL BLOCK DIAGRAM

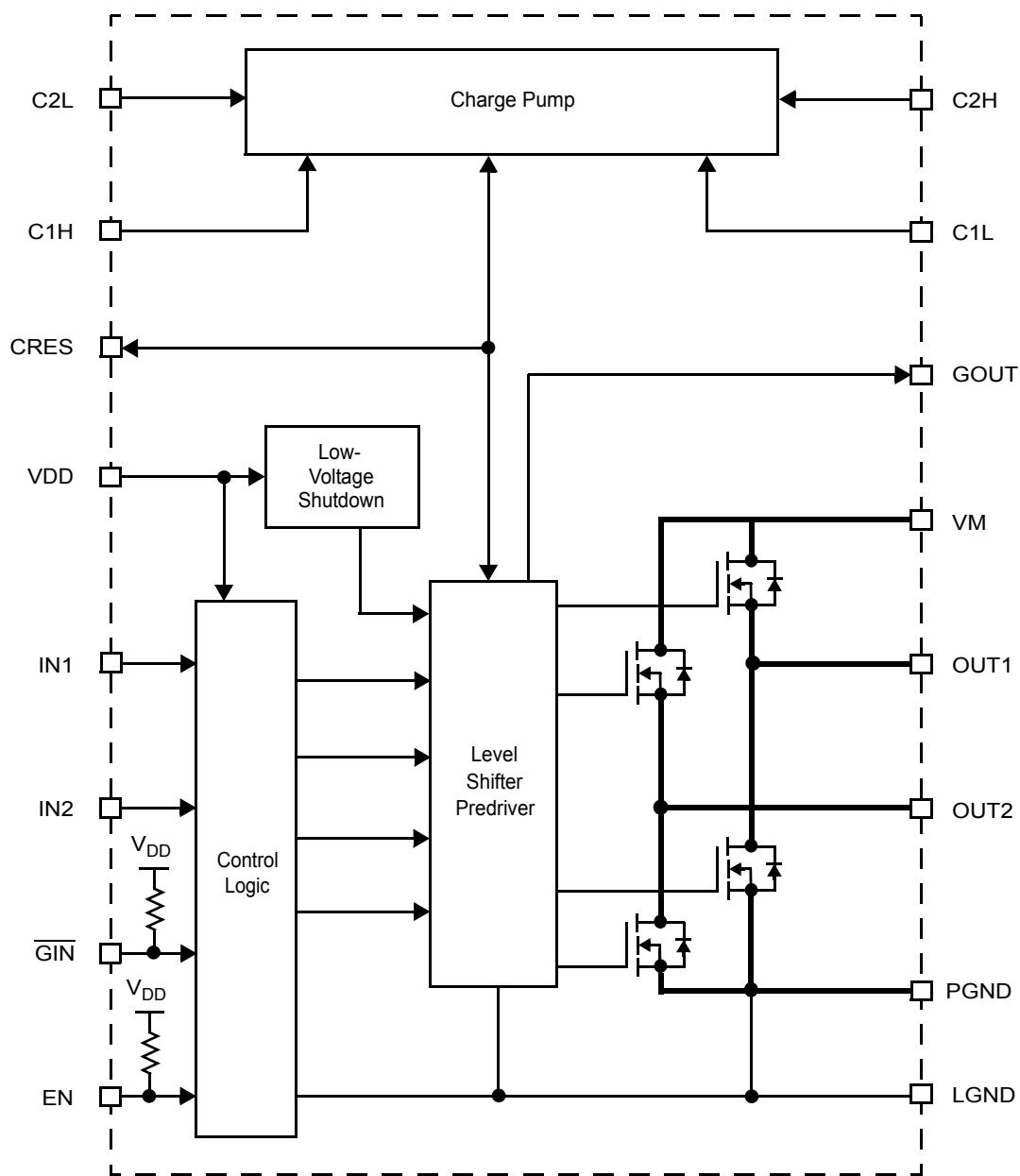


Figure 2. 17511A Simplified Internal Block Diagram

# PIN CONNECTIONS

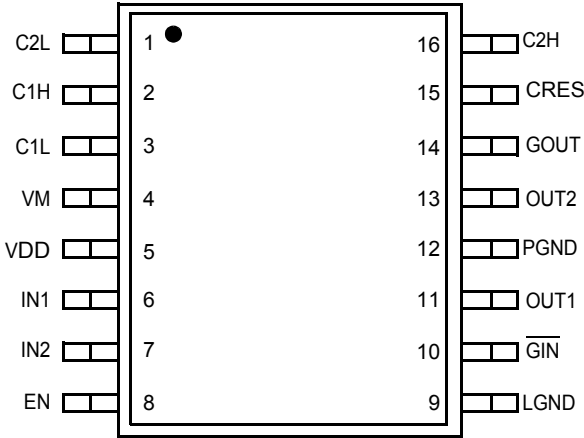


Figure 3. VMFP Pin Connections

Table 1. VMFP Pin Function Description

Pin Number	Pin Name	Formal Name	Definition
1	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
2	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
3	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
4	VM	Motor Drive Power Supply	Driver power supply voltage input pin.
5	VDD	Logic Supply	Control circuit power supply pin.
6	IN1	Input Control 1	Control signal input 1
7	IN2	Input Control 2	Control signal input 2.
8	EN	Enable Control	Enable control signal input pin.
9	LGND	Logic Ground	Logic ground pin.
10	GIN	Gate Driver Input	LOW = True control signal for GOUT pin.
11	OUT1	H-Bridge Output 1	Driver output 1 (right half of H-Bridge).
12	PGND	Power Ground	Driver ground pin.
13	OUT2	H-Bridge Output 2	Driver output 2 (left half of H-Bridge).
14	GOUT	Gate Driver Output	Output gate driver signal to external MOSFET switch.
15	CRES	Charge Pump Output Capacitor Connection	Charge pump reservoir capacitor pin.
16	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).



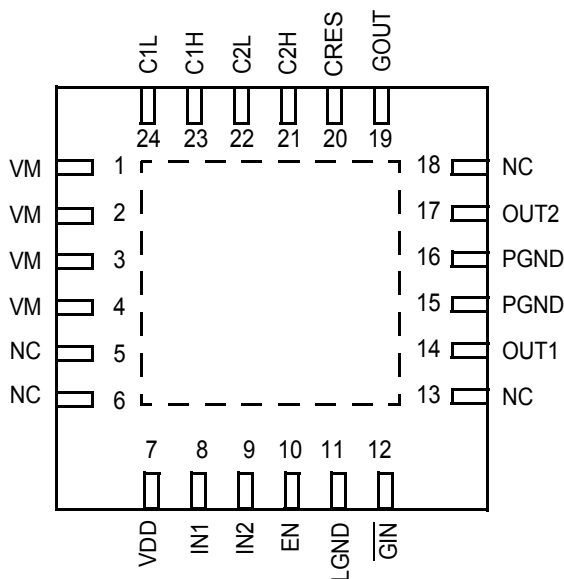


Figure 4. QFN Pin Connections

Table 2. QFN Pin Function Description

Pin Number	Pin Name	Formal Name	Definition
1, 2, 3, 4	VM	Motor Drive Power Supply	Driver power supply voltage input pin.
5, 6, 13, 18	NC	No Connect	This pin is not used.
7	VDD	Logic Supply	Control circuit power supply pin.
8	IN1	Logic Input Control 1	Control signal input 1.
9	IN2	Logic Input Control 2	Control signal input 2.
10	EN	Enable Control	Enable control signal input pin.
11	LGND	Logic Ground	Logic ground pin.
12	GIN	Gate Driver Input	LOW = True control signal for GOUT pin.
14	OUT1	Output 1	Driver output 1 (right half of H-Bridge).
15, 16	PGND	Power Ground	Driver ground pin.
17	OUT2	Output 2	Driver output 2 (left half of H-Bridge).
19	GOUT	Gate Driver Output	Output gate driver signal to external MOSFET switch.
20	CRES	Pre-Driver Power Supply	Pre-driver circuit power supply pin.
21	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
22	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
23	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
24	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).

# ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

**Table 3. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Motor Supply Voltage	$V_M$	-0.5 to 8.0	V
Charge Pump Output Voltage	$V_{CRES}$	-0.5 to 14.0	V
Logic Supply Voltage	$V_{DD}$	-0.5 to 7.0	V
Signal Input Voltage (EN, IN1, IN2, $\overline{GIN}$ )	$V_{IN}$	-0.5 to $V_{DD}+0.5$	V
Driver Output Current			A
Continuous	$I_O$	1.0	
Peak <sup>(1)</sup>	$I_{OPK}$	3.0	
ESD Voltage <sup>(2)</sup>			V
Human Body Model	$V_{ESD1}$	±1800	
Machine Model	$V_{ESD2}$	±100	
Storage Temperature Range	$T_{STG}$	-65 to 150	°C
Operating Ambient Temperature	$T_A$	-20 to 65	°C
Operating Junction Temperature	$T_J$	-20 to 150	°C
Thermal Resistance <sup>(3)</sup>	$R_{\theta JA}$		°C/W
24 Pin QFN		50	
16 Pin VMFP		150	
Power Dissipation <sup>(4)</sup>	$P_D$		mW
24 Pin QFN		2500	
16 Pin VMFP		830	
Soldering Temperature <sup>(5)</sup>	$T_{SOLDER}$	260	°C
Peak Package Reflow Temperature During Reflow <sup>(6), (7)</sup>	$T_{PPRT}$	Note 7	°C

**Notes**

- $T_A = 25^\circ\text{C}$ , 10 ms pulse width at 200 ms intervals.
- ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP} = 100\text{ pF}$ ,  $R_{ZAP} = 1500\ \Omega$ ), ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP} = 200\text{ pF}$ ,  $R_{ZAP} = 0\ \Omega$ ).
- QFN24: 45 x 30 x 1 [mm] glass EPOXY board mount. (See: recommended heat pattern) VMFP16: 37 x 50 x 1.6 [mm] glass EPOXY board mount. When the exposed pad is bonded,  $R_{sj}$  will not be performed.
- Maximum at  $T_A = 25^\circ\text{C}$ . When the exposed pad is bonded,  $R_{sj}$  will not be performed.
- Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescall's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescall.com](http://www.freescall.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

## STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions  $T_A = 25^\circ\text{C}$ ,  $V_M = V_{DD} = 5.0\text{V}$ ,  $\text{GND} = 0\text{V}$  unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^\circ\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>POWER</b>					
Driver Circuit Power Supply Voltage	$V_M$	2.0	5.0	6.8	V
Logic Supply Voltage	$V_{DD}$	2.7	5.0	5.7	V
Capacitor for Charge Pump	C1, C2, C3	0.01	0.1	1.0	$\mu\text{F}$
Standby Power Supply Current	$I_{V_{MSTBY}}$ $I_{V_{DDSTBY}}$	–	–	1.0	$\mu\text{A}$
Motor Supply Standby Current				1.0	$\text{mA}$
Logic Supply Standby Current (8)				1.0	$\text{mA}$
Operating Power Supply Current	$I_{V_{DD}}$ $I_{CRES}$	–	–	3.0	$\text{mA}$
Logic Supply Current (9)				0.7	$\text{mA}$
Charge Pump Circuit Supply Current				0.7	$\text{mA}$
Low $V_{DD}$ Detection Voltage (10)	$V_{DDDET}$	1.5	2.0	2.5	V
Driver Output ON Resistance (11)	$R_{DS(ON)}$	–	0.46	0.60	$\Omega$
<b>GATE DRIVE</b>					
Gate Drive Voltage (12) No Current Load	$V_{CRES}$	12	13	13.5	V
Gate Drive Ability (Internally Supplied) $I_{CRES} = -1.0\text{ mA}$	$V_{CRESLOAD}$	10	11.2	–	V
Gate Drive Output $I_{OUT} = -50\text{ }\mu\text{A}$ $I_{IN} = 50\text{ }\mu\text{A}$	$V_{GOUTHIGH}$ $V_{GOUTFLOW}$	$V_{CRES-0.5}$ LGND	$V_{CRES-0.1}$ LGND+0.1	$V_{CRES}$ LGND+0.5	V
<b>CONTROL LOGIC</b>					
Logic Input Voltage	$V_{IN}$	0	–	$V_{DD}$	V
Logic Input Function ( $2.7\text{V} < V_{DD} < 5.7\text{V}$ )	$V_{IH}$ $V_{IL}$ $I_{IH}$ $I_{IL}$	$V_{DD} \times 0.7$	–	–	V
High-Level Input Voltage		–	–	$V_{DD} \times 0.3$	V
Low-Level Input Voltage		–	–	1.0	$\mu\text{A}$
High-Level Input Current		–	–	–	$\mu\text{A}$
Low-Level Input Current		–1.0	–	–	$\mu\text{A}$
Pull-Up Resistance ( $\overline{\text{EN}}$ , $\overline{\text{GIN}}$ )	$R_{PU}$	50	100	200	$\text{k}\Omega$

**Notes**

- $I_{V_{DDSTBY}}$  includes current to the predriver circuit.
- $I_{V_{DD}}$  includes current to the predriver circuit.
- Detection voltage is defined as when the output becomes high-impedance after  $V_{DD}$  drops below the detection threshold. When the gate voltage  $V_{CRES}$  is applied from an external source,  $V_{CRES} = 7.5\text{V}$ .
- $I_O = 1.0\text{A}$  source + sink.
- Input logic signal not present.

### DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 5. Dynamic Electrical Characteristics**

Characteristics noted under conditions  $T_A = 25^\circ\text{C}$ ,  $V_M = V_{DD} = 5.0\text{V}$ ,  $\text{GND} = 0\text{V}$  unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^\circ\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>INPUT (EN, IN1, IN2, GIN)</b>					
Pulse Input Frequency	$f_{IN}$	—	—	200	kHz
Input Pulse Rise Time <sup>(13)</sup>	$t_R$	—	—	1.0 <sup>(14)</sup>	$\mu\text{s}$
Input Pulse Fall Time <sup>(15)</sup>	$t_F$	—	—	1.0 <sup>(14)</sup>	$\mu\text{s}$
<b>OUTPUT</b>					
Propagation Delay Time	$t_{PLH}$ $t_{PHL}$	—	0.55	1.0	$\mu\text{s}$
Turn-ON Time					
Turn-OFF Time					
GOUT Propagation Delay Time	$t_{SON}$ $t_{SOFF}$	—	0.15	0.5	$\mu\text{s}$
Turn-ON Time					
Turn-OFF Time					
Charge Pump Circuit <sup>(16)</sup>	$t_{VCRESON}$	—	0.1	3.0	ms
Rise Time <sup>(17)</sup>					
Low-Voltage Detection Time	$t_{VDDDET}$	—	—	10	ms

**Notes**

13. Time is defined between 10% and 90%.
14. That is, the input waveform slope must be steeper than this.
15. Time is defined between 90% and 10%.
16. When  $C1 = C2 = C3 = 0.1 \mu\text{F}$ .
17. Time to charge  $C_{RES}$  to 11V after application of  $V_{DD}$ .



### TIMING DIAGRAMS

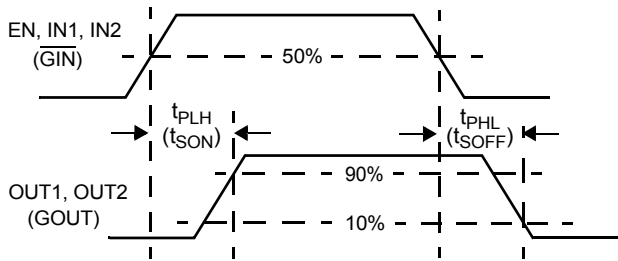


Figure 5.  $t_{PLH}$ ,  $t_{PHL}$ , and  $t_{PZH}$  Timing

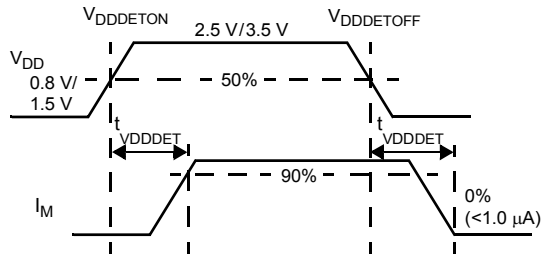


Figure 6. Low-Voltage Detection

Table 6. Truth Table

INPUT				OUTPUT		
EN	IN1	IN2	GIN	OUT1	OUT2	GOUT
H	H	H	X	L	L	X
H	H	L	X	H	L	X
H	L	H	X	L	H	X
H	L	L	X	Z	Z	X
L	X	X	X	L	L	L
H	X	X	H	X	X	L
H	X	X	L	X	X	H

H = High.  
L = Low.  
Z = High impedance.  
X = Don't care.

## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The 17511A is a monolithic H-Bridge power IC applicable to small DC motors used in portable electronics. The 17511A can operate efficiently with supply voltages as low as 2.0V to as high as 6.8V, and it can provide continuous motor drive currents of 1.0A while handling peak currents up to 3.0A. It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz. The 17511A has four operating modes: Forward, Reverse, Brake, and Tri-State (High Impedance).

Basic protection and operational features (direction, dynamic braking, PWM control of speed and torque, main power supply undervoltage detection and shutdown, logic power supply undervoltage detection and shutdown), in addition to the 1.0A rms output current capability, make the 17511A a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 17511A devices can be used to control bipolar step motors. The 17511A can also be used to excite transformer

primary windings with a switched square wave to produce secondary winding AC currents.

As shown in [Figure 2, 17511A Simplified Internal Block Diagram](#), page 2, the 17511A is a monolithic H-Bridge with built-in charge pump circuitry. For a DC motor to run, the input conditions need to be set as follows: ENable input logic HIGH, one INput logic LOW, and the other INput logic HIGH (to define output polarity). The 17511A can execute dynamic braking by setting both IN1 and IN2 logic HIGH, causing both low-side MOSFETs in the output H-Bridge to turn ON. Dynamic braking can also be implemented by taking the ENable logic LOW. The output of the H-Bridge can be set to an open-circuit high-impedance (Z) condition by taking both IN1 and IN2 logic LOW. (refer to [Table 6, Truth Table](#), page 8).

The 17511A outputs are capable of providing a continuous DC load current of up to 1.2A. An internal charge pump supports PWM frequencies to 200 kHz. The EN pin also controls the charge pump, turning it off when EN = LOW, thus allowing the 17511A to be placed in a power-conserving sleep mode.

### FUNCTIONAL PIN DESCRIPTION

#### OUT1 AND OUT2

The OUT1 and OUT2 pins provide the connection to the internal power MOSFET H-Bridge of the IC. A typical load connected between these pins would be a small DC motor. These outputs will connect to either VM or PGND, depending on the states of the control inputs (refer to [Table 6, Truth Table](#), page 8).

#### PGND AND LGND

The power and logic ground pins (PGND and LGND) should be connected together with a very low-impedance connection.

#### CRES

The CRES pin provides the connection for the external reservoir capacitor (output of the charge pump). Alternatively this pin can also be used as an input to supply gate-drive voltage from an external source via a series current-limiting resistor. The voltage at the CRES pin will be approximately three times the VDD voltage, as the internal charge pump utilizes a voltage tripler circuit. The VCRES voltage is used by the IC to supply gate drive for the internal power MOSFET H-Bridge.

#### VM

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power

to the load attached between OUT1 and OUT2. All VM pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

VM has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

#### IN1, IN2, AND EN

The IN1, IN2, and EN pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1, IN2, and EN work together to control OUT1 and OUT2 (refer to [Table 6, Truth Table](#)).

#### GIN

The  $\overline{\text{GIN}}$  input controls the GOUT pin. When  $\overline{\text{GIN}}$  is set logic LOW, GOUT supplies a level-shifted high-side gate drive signal to an external MOSFET. When  $\overline{\text{GIN}}$  is set logic HIGH, GOUT is set to GND potential.

#### C1L AND C1H, C2L AND C2H

These two pairs of pins, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1  $\mu\text{F}$ .

## GOUT

The GOUT output pin provides a level-shifted, high-side gate drive signal to an external MOSFET with  $C_{ISS}$  up to 500pF.

## VDD

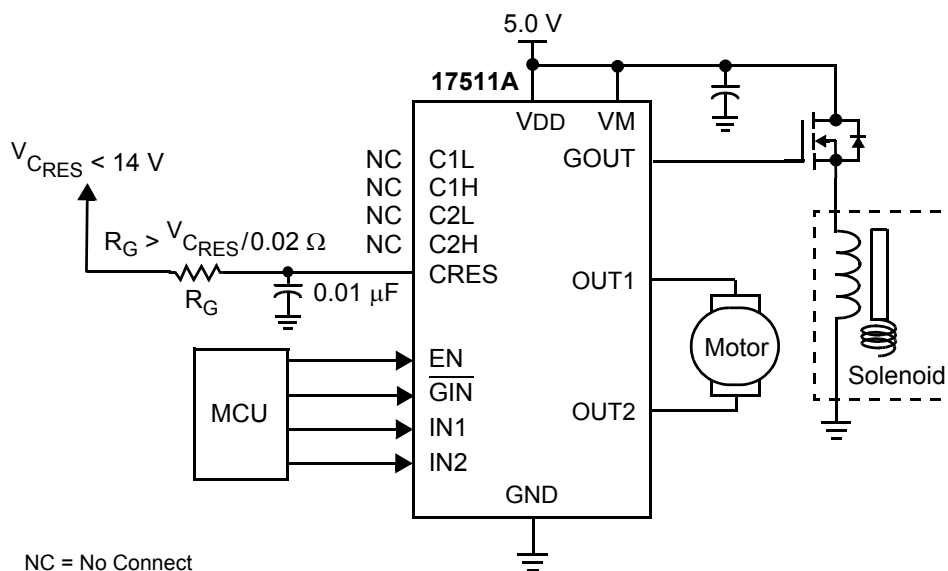
The VDD pin carries the 5.0V supply voltage and current into the logic sections of the IC. VDD has an undervoltage

threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

## TYPICAL APPLICATIONS

[Figure 7](#) shows a typical application for the 17511A. When applying the gate voltage to the CRES pin from an external

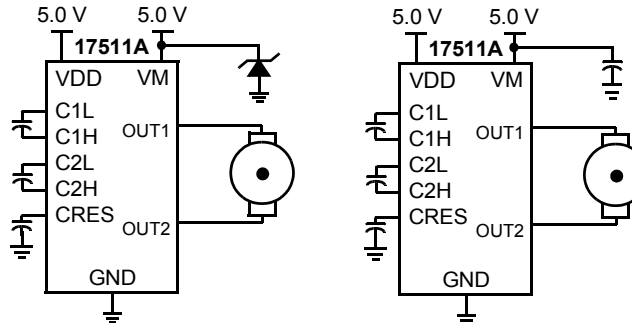
source, be sure to connect it via a resistor equal to, or greater than,  $R_G = V_{C_{RES}}/0.02\Omega$ .



### Figure 7. 17511A Typical Application Diagram

## CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients via placing a capacitor or zener at the supply pin (VM) (see [Figure 8](#)).



### Figure 8. CEMF Snubbing Techniques

## PACKAGING

### SOLDERING

#### THERMAL PERFORMANCE

Below are the recommended heat patterns for the QFN24 Exposed Pad thermal package.

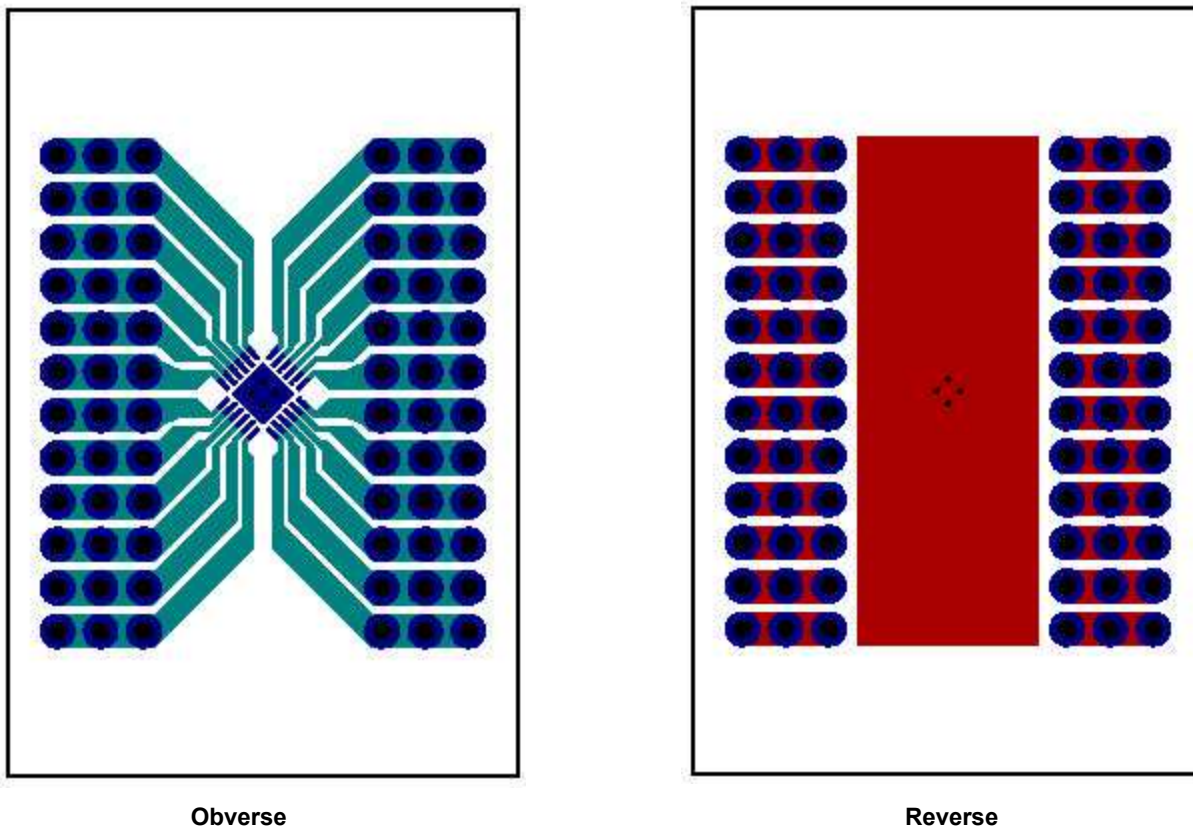
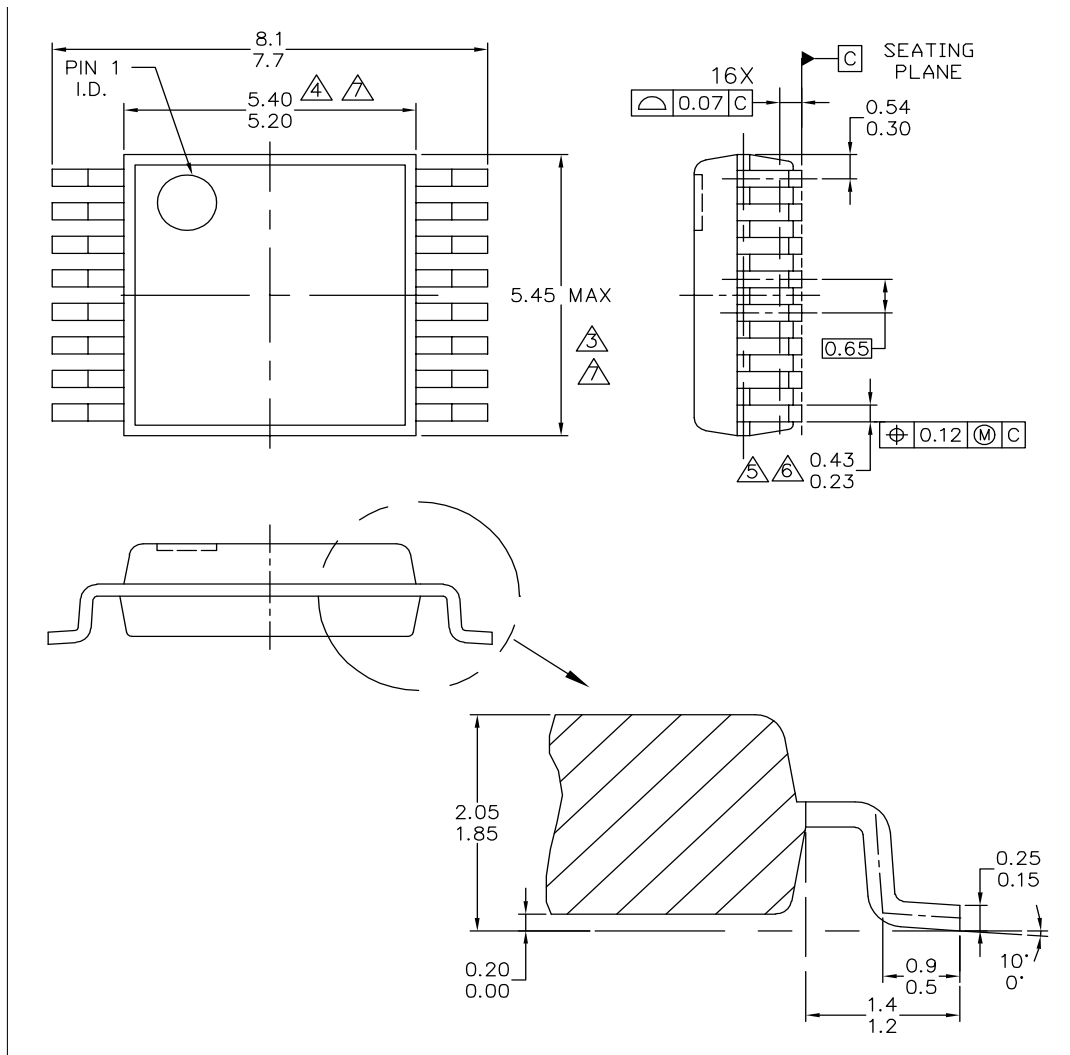


Figure 9. Recommended Heat Patterns for QFN24 EP



# PACKAGE DIMENSIONS

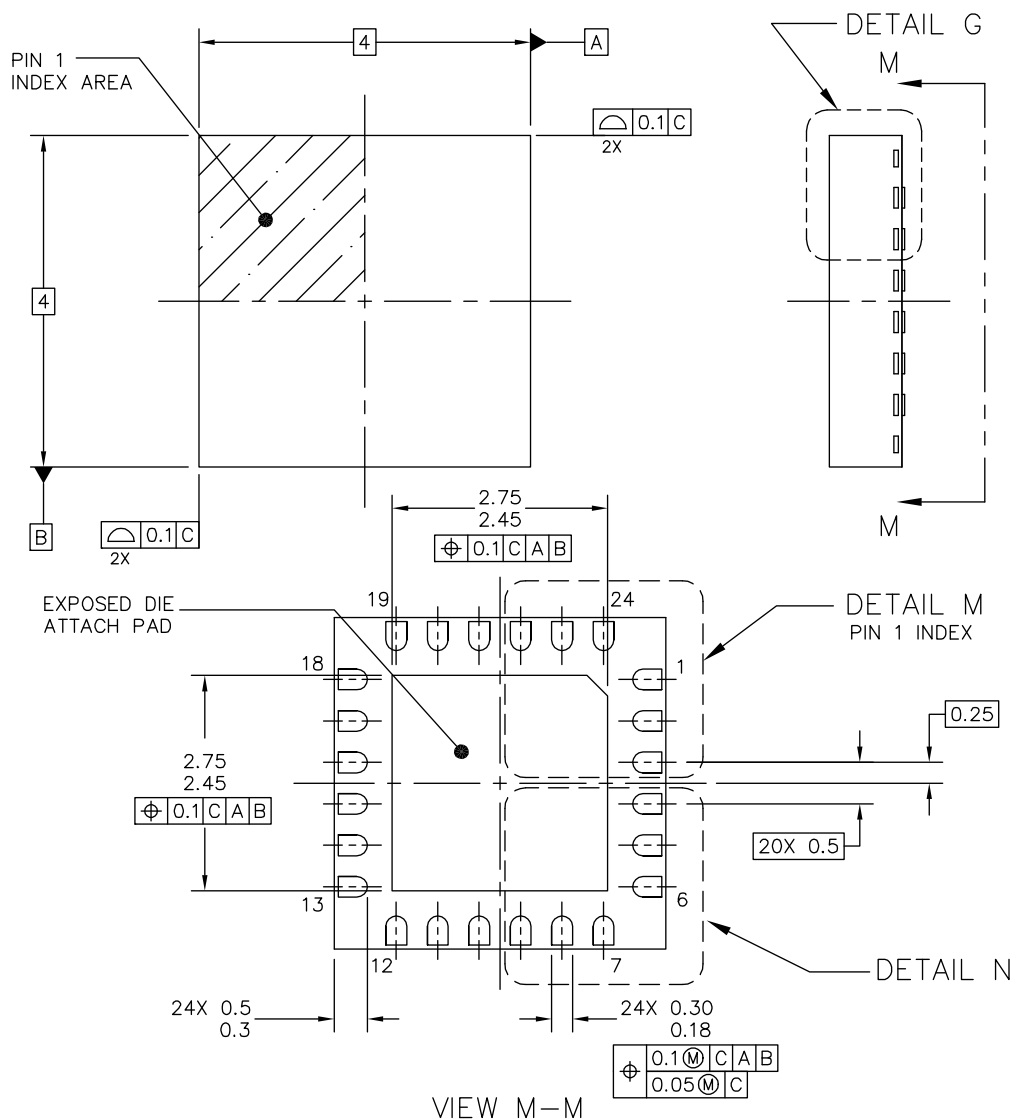
For the most current package revision, visit [www.freescale.com](http://www.freescale.com) and perform a keyword search using the "98A" listed below.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE
TITLE: 16LD VMFP, 5.30 X 5.45 PKG 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ASA10614D	REV: B
	CASE NUMBER: 1563-02	07 NOV 2007
	STANDARD: NON-JEDEC	

**EV (PB-FREE) SUFFIX**  
 16-PIN VMFP  
 PLASTIC PACKAGE  
 98ASA10614D  
 ISSUE B

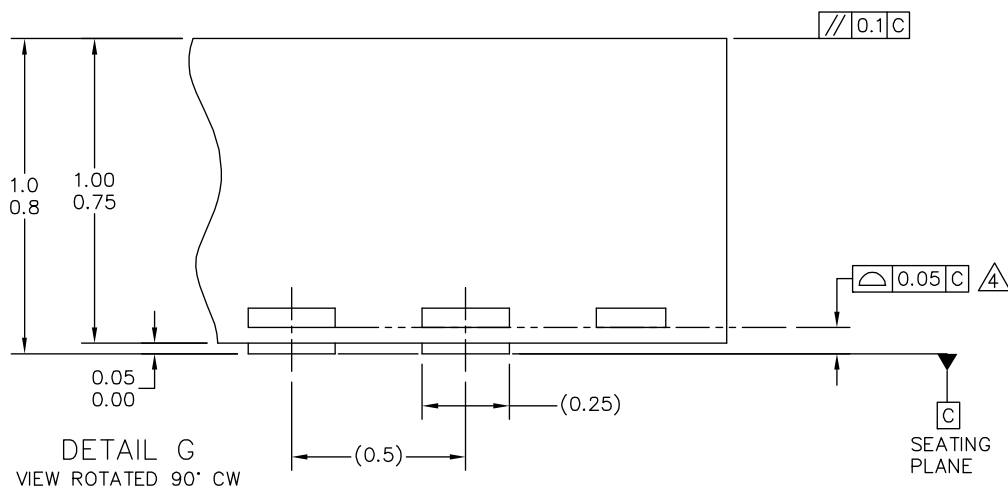
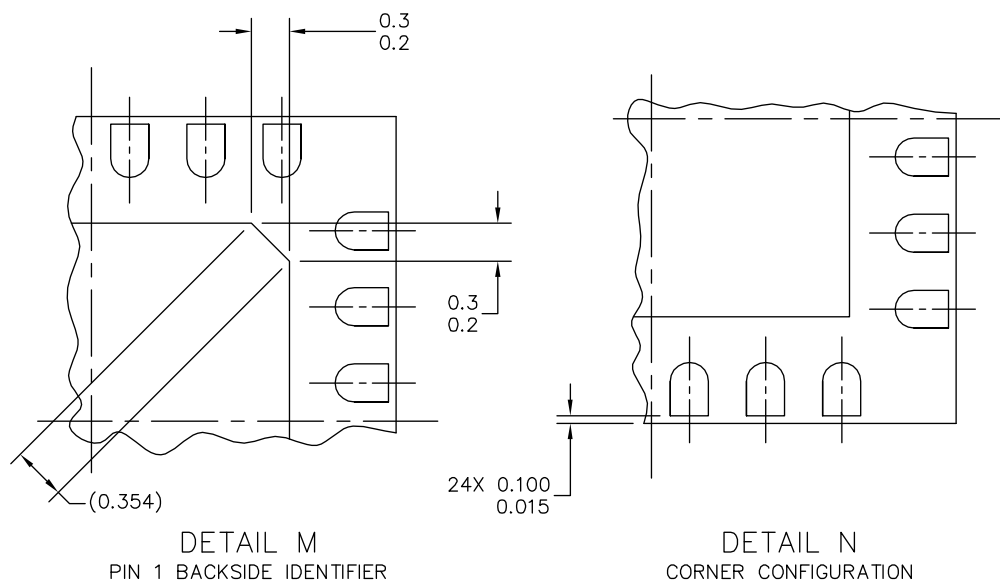
### PACKAGE DIMENSIONS (CONTINUED)



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		<b>MECHANICAL OUTLINE</b>		PRINT VERSION NOT TO SCALE	
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 24 TERMINAL, 0.5 PITCH (4 X 4 X 1)		DOCUMENT NO: 98ARL10577D		REV: B	
		CASE NUMBER: 1508-02		28 DEC 2005	
		STANDARD: NON-JEDEC			

**EP (PB-FREE) SUFFIX**  
24-PIN QFN  
**NON-LEADED PACKAGE**  
98ARL10577D  
ISSUE B

### PACKAGE DIMENSIONS (CONTINUED)



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		<b>MECHANICAL OUTLINE</b>		PRINT VERSION NOT TO SCALE	
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 24 TERMINAL, 0.5 PITCH (4 X 4 X 1)		DOCUMENT NO: 98ARL10577D		REV: B	
		CASE NUMBER: 1508-02		28 DEC 2005	
		STANDARD: NON-JEDEC			

### REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	4/2007	<ul style="list-style-type: none"><li>Implemented Revision History page</li><li>Converted to Freescale format</li><li>Added Peak Package Reflow Temperature During Reflow (solder reflow) parameter and Note with instructions from <a href="http://www.freescale.com">www.freescale.com</a> to Maximum Ratings Table 3</li></ul>
3.0	11/2007	<ul style="list-style-type: none"><li>Replaced 16 pin package drawing with 98ASA10614D, REV. B and replaced 24 pin package drawing with 98ARL10577D, REV. B.</li></ul>
4.0	2/2008	<ul style="list-style-type: none"><li>Revised Siplified Application Diagram on page 1; Corrected typo - VM voltage from 15V to 5V.</li></ul>
5.0	8/2008	<ul style="list-style-type: none"><li>Further Defined Thermal Resistance and Power Disapation in Table 2, Page 5 for both packages.</li></ul>

ARCHIVE INFORMATION

ARCHIVE INFORMATION

## How to Reach Us:

### Home Page:

[www.freescale.com](http://www.freescale.com)

### Web Support:

<http://www.freescale.com/support>

### USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
+1-800-521-6274 or +1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### Japan:

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2008. All rights reserved.