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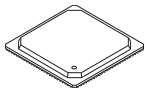
MPC5121E/MPC5123



516 TEPBGA
27 mm x 27 mm

MPC5121E/MPC5123 Data Sheet

The MPC5121e/MPC5123 integrates a high performance e300 CPU core based on the Power Architecture® Technology with a rich set of peripheral functions focused on communications and systems integration.

Major features of the MPC5121e/MPC5123 are:

- e300 Power Architecture processor core
- Power modes include doze, nap, sleep, deep sleep, and hibernate
- AXE – Auxiliary Execution Engine
- MBX Lite – 2D/3D graphics engine (not available in MPC5123)
- DIU – Display interface unit
- DDR1, DDR2, and LPDDR/mobile-DDR SDRAM memory controller
- MEM – 128 KB on-chip SRAM
- USB 2.0 OTG controller with integrated physical layer (PHY)
- DMA subsystem
- EMB – Flexible multi-function external memory bus interface
- NFC – NAND flash controller
- LPC – LocalPlus interface
- 10/100Base Ethernet
- PCI interface, version 2.3
- PATA – Parallel ATA integrated development environment (IDE) controller
- SATA – Serial ATA controller with integrated physical layer (PHY)
- SDHC – MMC/SD/SDIO card host controller
- PSC – Programmable serial controller
- I^2C – inter-integrated circuit communication interfaces
- S/PDIF – Serial audio interface
- CAN – Controller area network
- BDLC – J1850 interface
- VIU – Video Input, ITU-656 compliant
- RTC – On-Chip real-time clock
- On-chip temperature sensor
- IIM – IC Identification module

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Figure 1 shows a simplified MPC5121e/MPC5123 block diagram.

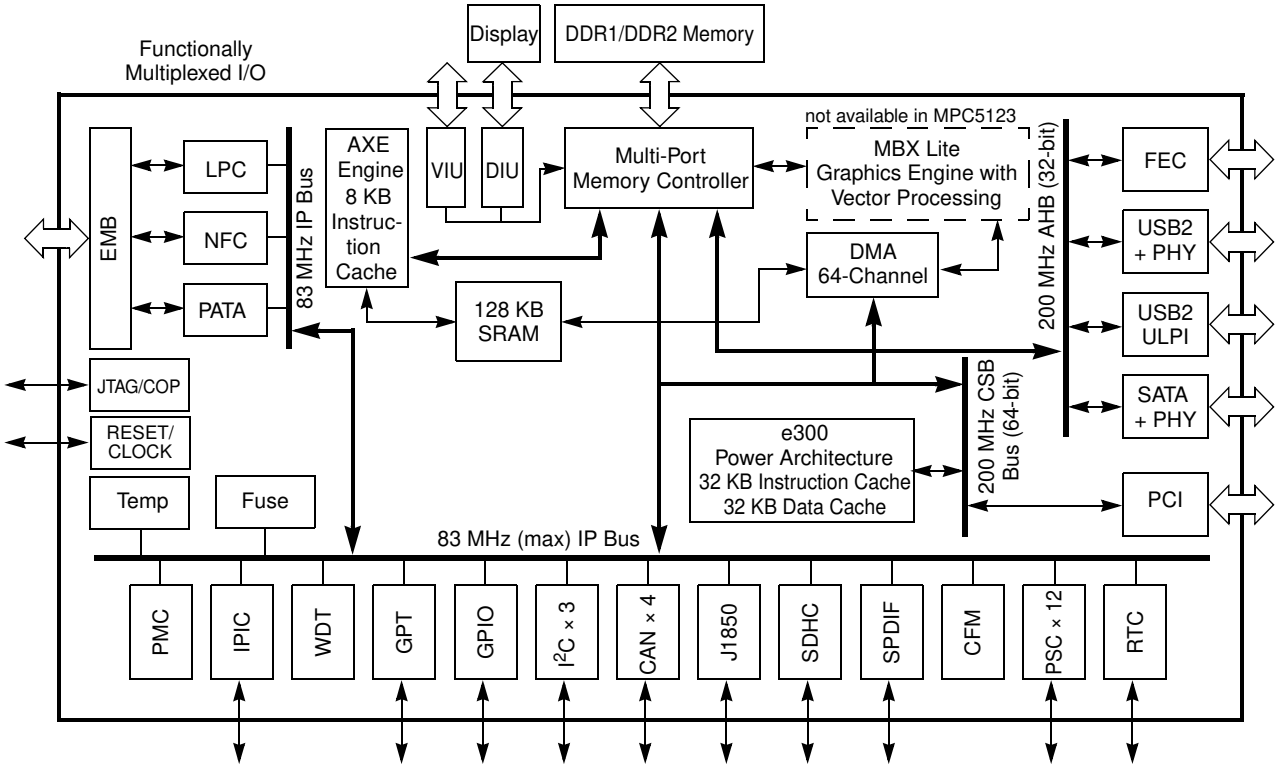

Figure 1. Simplified MPC5121e/MPC5123 Block Diagram

1 Ordering Information

Table 1. MPC5121e Orderable Part Numbers

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5121VY400B	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tray
MPC5121VY400BR	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tape and Reel
MPC5121YVY400B	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tray
MPC5121YVY400BR	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tape and Reel
SPC5121YVY400B	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tray
SPC5121YVY400BR	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tape and Reel

Table 2. MPC5123 Orderable Part Numbers

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5123VY400B	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tray
MPC5123VY400BR	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tape and Reel
MPC5123YVY400B	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tray

Table 2. MPC5123 Orderable Part Numbers (continued)

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5123YVY400BR	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tape and Reel
SPC5123YVY400B	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tray
SPC5123YVY400BR	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tape and Reel

2 Pin Assignments

This section details pin assignments.

2.1 516-TEPBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A		VSS	VSS	SATA_RXN	SATA_RXP	SATA_RX_VSSA	PSC7_4	PSC7_3	PSC6_4	PSC6_2	PSC6_0	PSC11_0	PSC10_2	PSC2_3	PSC1_3	PSC1_1	PSC0_1	CAN1_TX	GPIO28	RTC_XTALO	USB2_DRVVBUS	USB_DM	USB_DP	USB_TPA	VSS	
B	VSS	VSS	VSS	SATA_RX_VSSA	VSS	PSC8_3	VSS	PSC7_0	PSC6_3	VDD_IO	PSC11_1	VSS	PSC10_1	PSC2_1	VDD_IO	PSC0_4	VSS	GPIO31	CAN2_RX	VSS	USB2_VBUS_PWR_FAULT	VSS	USB_VSSA_BIAS	USB_XTALO	VDD_IO	VSS
C	VSS	SATA_XTALO	SATA_XTALI	VSS	SATA_VDDA_1P2	PSC9_0	PSC8_2	PSC7_2	AVDD_FUSEWR	PSC6_1	PSC11_2	PSC10_3	PSC10_0	PSC2_0	PSC1_0	PSC0_3	PSC_MCLK_IN	GPIO30	CAN1_RX	RTC_XTALI	USB_VDDA	USB_VSSA	VSS	USB_XTALI	VSS	PCI_CLK
D	SATA_VDDA_1P2	VSS	SATA_PLL_VSSA	SATA_VDDA_3P3	SATA_VDDA_VREG	PSC9_3	PSC9_1	PSC8_1	VDD_IO	VDD_IO	PSC11_4	VSS	PSC2_4	PSC1_4	VDD_IO	PSC0_0	VSS	HIB_MODE	VBAT_RTC	USB_VDDA	USB_VBUS	USB_VDDA_BIAS	USB_PLL_PWR3	VSS	VSS	PCI_REQ2
E	SATA_TXN	SATA_VDDA_1P2	SATA_PLL_VDDA1P2	SATA_RESREF	SATA_ANAVIZ	PSC9_4	PSC9_2	PSC8_4	PSC8_0	PSC7_1	PSC11_3	PSC10_4	PSC2_2	PSC1_2	PSC0_2	CAN2_TX	GPIO29	VSS	USB_UID	USB_VSSA	USB_VSSA	USB_RREF	USB_PLL_GND	PCI_GNT2	PCI_GNT0	PCI_REQ1
F	SATA_TXP	VSS	VSS	VSS	VSS	VSS		VSS		VSS	VDD_IO		VDD_IO	VDD_IO		VSS	VSS		VDD_IO		VSS	PCI_RST_OUT	VDD_IO	PCI_AD30	VDD_IO	PCI_AD28
G	SATA_TX_VSSA	NFC_RE	NFC_WE	NFC_WP	VSS																	PCI_GNT1	PCI_REQ0	PCI_AD29	PCI_AD26	PCI_C/BE3
H	NFC_R/B	PATA_DACK	NFC_CE0	NFC_ALE	NFC_CLE	VSS															VDD_IO	PCI_AD31	VSS	PCI_AD24	VSS	PCI_AD21
J	PATA_IOR	PATA_IOCHRDY	PATA_INTRQ	PATA_DRQ	VDD_IO																	PCI_AD27	PCI_AD25	PCI_AD23	PCI_AD20	PCI_AD18
K	PATA_CE1	VDD_IO	PATA_ISOLATE	VDD_IO	PATA_IOW	VSS				VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE				VSS	PCI_IDSEL	PCI_AD22	PCI_AD19	PCI_AD17	PCI_IRDY
L	EMB_AD03	EMB_AD02	EMB_AD01	EMB_AD00	PATA_CE2	VSS				VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE				VSS	PCI_AD16	VDD_IO	PCI_C/BE2	VDD_IO	PCI_DEVSEL
M	EMB_AD06	VSS	EMB_AD05	VSS	EMB_AD04					VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE					PCI_TRDY	PCI_FRAME	PCI_STOP	PCI_PERR	PCI_SERR
N	EMB_AD10	EMB_AD09	EMB_AD08	EMB_AD07	VSS	VDD_IO				VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE				VDD_IO	PCI_PAR	VSS	PCI_C/BE1	VSS	PCI_AD15
P	EMB_AD15	EMB_AD14	EMB_AD11	EMB_AD13	EMB_AD12	VDD_IO				VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE				VDD_IO	PCI_C/BE0	PCI_AD09	PCI_AD13	PCI_AD14	PCI_AD12
R	EMB_AD17	VDD_IO	EMB_AD16	VDD_IO	EMB_AD19					VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE					PCI_AD03	PCI_AD06	PCI_AD10	PCI_AD11	PCI_AD08
T	EMB_AD22	EMB_AD18	EMB_AD20	EMB_AD21	EMB_AD23	VSS				VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE				VSS	SYS_PLL_AVDD	VDD_IO	PCI_AD05	VDD_IO	PCI_AD07
U	EMB_AD25	VSS	EMB_AD24	VSS	EMB_AD29	VSS				VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE				VSS	SYS_PLL_AVSS	PCI_INTA	PCI_AD00	PCI_AD02	PCI_AD04
V	EMB_AD26	EMB_AD27	EMB_AD28	EMB_AD30	EMB_AX01																	SRESET	VSS	SYS_XTALI	VSS	PCI_AD01
W	EMB_AD31	EMB_AX00	EMB_AX02	LPC_AX03	LPC_CS0	VDD_IO															VDD_IO	TDO	PORESET	HRESET	TEST	SYS_XTALO
Y	LPC_CS2	VDD_IO	LPC_CS1	VDD_IO	LPC_OE																	J1850_TX	TDI	VSS	TMS	CKSTP_OUT
AA	LPC_RWB	LPC_ACK	PSC4_1	LPC_CLK	PSC4_3	VSS		VDD_MEM_IO		VSS	VSS		VDD_MEM_IO	VDD_MEM_IO		VSS	VSS		CORE_PLL_AVDD		VSS	I2C2_SDA	VDD_IO	J1850_RX	VDD_IO	TRST
AB	PSC4_0	VSS	PSC4_2	VSS	PSC3_1	MDQ1	MVTT0	MDQ5	MDQ10	VSS	MVREF	MDQ19	MDQ21	MDQ27	MDQ31	MA1	MA5	VDD_MEM_IO	MA14	MCKE	SPDIF_TXCLK	I2C1_SCL	I2C1_SDA	VSS	IRQ1	TCK
AC	PSC5_0	PSC4_4	PSC5_1	PSC3_2	VDD_MEM_IO	MDM0	MDQ8	VSS	MDQ14	VDD_MEM_IO	MDQS2	VSS	MDQ25	VDD_MEM_IO	MDQ30	MBA1	VSS	MA7	MA11	VDD_MEM_IO	MODT	VSS	I2C0_SCL	SPDIF_RX	I2C2_SCL	IRQ0
AD	PSC5_2	PSC5_3	VSS	PSC3_3	MDQS0	MDQ6	MDQ11	MDQS1	VDD_MEM_IO	MDQ16	MDQ18	MDQ20	MDQ23	MDQS3	MDQ29	MBA0	MA0	MA4	MA9	MA13	MWE	MCS	CORE_PLL_AVSS	SPDIF_TX	VSS	I2C0_SDA
AE	VDD_IO	VDD_IO	PSC5_4	MDQ2	VDD_MEM_IO	MDQ7	VSS	MDM1	MDQ12	VDD_MEM_IO	MVTT2	VSS	MDQ24	MVTT3	VDD_MEM_IO	MDQ28	VSS	MA2	MA6	VDD_MEM_IO	MA12	MA15	VSS	VDD_IO	VDD_IO	VSS
AF		VDD_IO	PSC3_0	PSC3_4	MDQ0	MDQ3	MDQ4	MDQ9	MVTT1	MDQ13	MDQ15	MDQ17	MDM2	MDQ22	MDQ26	MDM3	MCK	MCK	MBA2	MA3	MA8	MA10	MRAS	MCAS	VDD_IO	

Figure 2. Ball Map for the MPC5121e 516 TEPBGA Package

2.2 Pinout Listings

Table 3 provides the pin-out listing for the MPC5121e/MPC5123.

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 1 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
DDR Memory Interface (67 Total)				
MDQ0	AF5	DDR	$V_{DD\_MEM\_IO}$	—
MDQ1	AB6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ2	AE4	DDR	$V_{DD\_MEM\_IO}$	—
MDQ3	AF6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ4	AF7	DDR	$V_{DD\_MEM\_IO}$	—
MDQ5	AB8	DDR	$V_{DD\_MEM\_IO}$	—
MDQ6	AD6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ7	AE6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ8	AC7	DDR	$V_{DD\_MEM\_IO}$	—
MDQ9	AF8	DDR	$V_{DD\_MEM\_IO}$	—
MDQ10	AB9	DDR	$V_{DD\_MEM\_IO}$	—
MDQ11	AD7	DDR	$V_{DD\_MEM\_IO}$	—
MDQ12	AE9	DDR	$V_{DD\_MEM\_IO}$	—
MDQ13	AF10	DDR	$V_{DD\_MEM\_IO}$	—
MDQ14	AC9	DDR	$V_{DD\_MEM\_IO}$	—
MDQ15	AF11	DDR	$V_{DD\_MEM\_IO}$	—
MDQ16	AD10	DDR	$V_{DD\_MEM\_IO}$	—
MDQ17	AF12	DDR	$V_{DD\_MEM\_IO}$	—
MDQ18	AD11	DDR	$V_{DD\_MEM\_IO}$	—
MDQ19	AB12	DDR	$V_{DD\_MEM\_IO}$	—
MDQ20	AD12	DDR	$V_{DD\_MEM\_IO}$	—
MDQ21	AB13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ22	AF14	DDR	$V_{DD\_MEM\_IO}$	—
MDQ23	AD13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ24	AE13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ25	AC13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ26	AF15	DDR	$V_{DD\_MEM\_IO}$	—
MDQ27	AB14	DDR	$V_{DD\_MEM\_IO}$	—
MDQ28	AE16	DDR	$V_{DD\_MEM\_IO}$	—
MDQ29	AD15	DDR	$V_{DD\_MEM\_IO}$	—
MDQ30	AC15	DDR	$V_{DD\_MEM\_IO}$	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 2 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
MDQ31	AB15	DDR	$V_{DD\_MEM\_IO}$	—
MDM0	AC6	DDR	$V_{DD\_MEM\_IO}$	—
MDM1	AE8	DDR	$V_{DD\_MEM\_IO}$	—
MDM2	AF13	DDR	$V_{DD\_MEM\_IO}$	—
MDM3	AF16	DDR	$V_{DD\_MEM\_IO}$	—
MDQS0	AD5	DDR	$V_{DD\_MEM\_IO}$	—
MDQS1	AD8	DDR	$V_{DD\_MEM\_IO}$	—
MDQS2	AC11	DDR	$V_{DD\_MEM\_IO}$	—
MDQS3	AD14	DDR	$V_{DD\_MEM\_IO}$	—
MBA0	AD16	DDR	$V_{DD\_MEM\_IO}$	—
MBA1	AC16	DDR	$V_{DD\_MEM\_IO}$	—
MBA2	AF19	DDR	$V_{DD\_MEM\_IO}$	—
MA0	AD17	DDR	$V_{DD\_MEM\_IO}$	—
MA1	AB16	DDR	$V_{DD\_MEM\_IO}$	—
MA2	AE18	DDR	$V_{DD\_MEM\_IO}$	—
MA3	AF20	DDR	$V_{DD\_MEM\_IO}$	—
MA4	AD18	DDR	$V_{DD\_MEM\_IO}$	—
MA5	AB17	DDR	$V_{DD\_MEM\_IO}$	—
MA6	AE19	DDR	$V_{DD\_MEM\_IO}$	—
MA7	AC18	DDR	$V_{DD\_MEM\_IO}$	—
MA8	AF21	DDR	$V_{DD\_MEM\_IO}$	—
MA9	AD19	DDR	$V_{DD\_MEM\_IO}$	—
MA10	AF22	DDR	$V_{DD\_MEM\_IO}$	—
MA11	AC19	DDR	$V_{DD\_MEM\_IO}$	—
MA12	AE21	DDR	$V_{DD\_MEM\_IO}$	—
MA13	AD20	DDR	$V_{DD\_MEM\_IO}$	—
MA14	AB19	DDR	$V_{DD\_MEM\_IO}$	—
MA15	AE22	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MWE}}$	AD21	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MRAS}}$	AF23	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MCAS}}$	AF24	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MCS}}$	AD22	DDR	$V_{DD\_MEM\_IO}$	—
MCKE	AB20	DDR	$V_{DD\_MEM\_IO}$	—
MCK	AF17	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MCK}}$	AF18	DDR	$V_{DD\_MEM\_IO}$	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 3 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
MODT	AC21	DDR	$V_{DD\_MEM\_IO}$	—
LPC Interface (8 Total)				
LPC_CLK	AA4	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_OE}}$	Y5	General IO	V_{DD_IO}	—
LPC_$\overline{\text{RW}}$	AA1	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_CS0}}$	W5	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_CS1}}$	Y3	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_CS2}}$	Y1	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_ACK}}$	AA2	General IO	V_{DD_IO}	—
LPC_AX03	W4	General IO	V_{DD_IO}	—
EMB Interface (35 Total)				
EMB_AX02	W3	General IO	V_{DD_IO}	—
EMB_AX01	V5	General IO	V_{DD_IO}	—
EMB_AX00	W2	General IO	V_{DD_IO}	—
EMB_AD31	W1	General IO	V_{DD_IO}	—
EMB_AD30	V4	General IO	V_{DD_IO}	—
EMB_AD29	U5	General IO	V_{DD_IO}	—
EMB_AD28	V3	General IO	V_{DD_IO}	—
EMB_AD27	V2	General IO	V_{DD_IO}	—
EMB_AD26	V1	General IO	V_{DD_IO}	—
EMB_AD25	U1	General IO	V_{DD_IO}	—
EMB_AD24	U3	General IO	V_{DD_IO}	—
EMB_AD23	T5	General IO	V_{DD_IO}	—
EMB_AD22	T1	General IO	V_{DD_IO}	—
EMB_AD21	T4	General IO	V_{DD_IO}	—
EMB_AD20	T3	General IO	V_{DD_IO}	—
EMB_AD19	R5	General IO	V_{DD_IO}	—
EMB_AD18	T2	General IO	V_{DD_IO}	—
EMB_AD17	R1	General IO	V_{DD_IO}	—
EMB_AD16	R3	General IO	V_{DD_IO}	—
EMB_AD15	P1	General IO	V_{DD_IO}	—
EMB_AD14	P2	General IO	V_{DD_IO}	—
EMB_AD13	P4	General IO	V_{DD_IO}	—
EMB_AD12	P5	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 4 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
EMB_AD11	P3	General IO	V_{DD_IO}	—
EMB_AD10	N1	General IO	V_{DD_IO}	—
EMB_AD09	N2	General IO	V_{DD_IO}	—
EMB_AD08	N3	General IO	V_{DD_IO}	—
EMB_AD07	N4	General IO	V_{DD_IO}	—
EMB_AD06	M1	General IO	V_{DD_IO}	—
EMB_AD05	M3	General IO	V_{DD_IO}	—
EMB_AD04	M5	General IO	V_{DD_IO}	—
EMB_AD03	L1	General IO	V_{DD_IO}	—
EMB_AD02	L2	General IO	V_{DD_IO}	—
EMB_AD01	L3	General IO	V_{DD_IO}	—
EMB_AD00	L4	General IO	V_{DD_IO}	—
PATA Interface (9 Total)				
$\overline{\text{PATA\_CE1}}$	K1	General IO	V_{DD_IO}	ATA name: CS0
$\overline{\text{PATA\_CE2}}$	L5	General IO	V_{DD_IO}	ATA name: CS1
PATA_ISOLATE	K3	General IO	V_{DD_IO}	—
$\overline{\text{PATA\_IOR}}$	J1	General IO	V_{DD_IO}	ATA name: DIOR
$\overline{\text{PATA\_IOW}}$	K5	General IO	V_{DD_IO}	ATA name: DIOW
PATA_IOCHRDY	J2	General IO	V_{DD_IO}	ATA name: IORDY
PATA_INTRQ	J3	General IO	V_{DD_IO}	—
PATA_DRQ	J4	General IO	V_{DD_IO}	ATA name: DMARQ
$\overline{\text{PATA\_DACK}}$	H2	General IO	V_{DD_IO}	ATA name: DMACK
NFC Interface (7 Total)				
$\overline{\text{NFC\_WP}}$	G4	General IO	V_{DD_IO}	—
NFC_R/$\overline{\text{B}}$	H1	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_WE}}$	G3	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_RE}}$	G2	General IO	V_{DD_IO}	—
NFC_ALE	H4	General IO	V_{DD_IO}	—
NFC_CLE	H5	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_CE0}}$	H3	General IO	V_{DD_IO}	—
I2C Interface (6 Total)				
I2C0_SCL	AC23	General IO	V_{DD_IO}	—
I2C0_SDA	AD26	General IO	V_{DD_IO}	—
I2C1_SCL	AB22	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 5 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
I2C1_SDA	AB23	General IO	V_{DD_IO}	—
I2C2_SCL	AC25	General IO	V_{DD_IO}	—
I2C2_SDA	AA22	General IO	V_{DD_IO}	—
IRQ Interface (2 Total)				
$\overline{IRQ0}$	AC26	General IO	V_{DD_IO}	—
$\overline{IRQ1}$	AB25	General IO	V_{DD_IO}	—
CAN Interface (4 Total)				
CAN1_RX	C19	Analog Input	VBAT_RTC	—
CAN1_TX	A18	General IO	V_{DD_IO}	—
CAN2_RX	B19	Analog Input	VBAT_RTC	—
CAN2_TX	E16	General IO	V_{DD_IO}	—
J1850 Interface (2 Total)				
J1850_TX	Y22	General IO	V_{DD_IO}	—
J1850_RX	AA24	General IO	V_{DD_IO}	—
SPDIF Interface (3 Total)				
SPDIF_TXCLK	AB21	General IO	V_{DD_IO}	—
SPDIF_TX	AD24	General IO	V_{DD_IO}	—
SPDIF_RX	AC24	General IO	V_{DD_IO}	—
PCI (54 Total)				
$\overline{PCI\_INTA}$	U23	PCI	V_{DD_IO}	—
$\overline{PCI\_RST\_OUT}$	F22	PCI	V_{DD_IO}	—
PCI_AD00	U24	PCI	V_{DD_IO}	—
PCI_AD01	V26	PCI	V_{DD_IO}	—
PCI_AD02	U25	PCI	V_{DD_IO}	—
PCI_AD03	R22	PCI	V_{DD_IO}	—
PCI_AD04	U26	PCI	V_{DD_IO}	—
PCI_AD05	T24	PCI	V_{DD_IO}	—
PCI_AD06	R23	PCI	V_{DD_IO}	—
PCI_AD07	T26	PCI	V_{DD_IO}	—
PCI_AD08	R26	PCI	V_{DD_IO}	—
PCI_AD09	P23	PCI	V_{DD_IO}	—
PCI_AD10	R24	PCI	V_{DD_IO}	—
PCI_AD11	R25	PCI	V_{DD_IO}	—
PCI_AD12	P26	PCI	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 6 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
PCI_AD13	P24	PCI	V_{DD_IO}	—
PCI_AD14	P25	PCI	V_{DD_IO}	—
PCI_AD15	N26	PCI	V_{DD_IO}	—
PCI_AD16	L22	PCI	V_{DD_IO}	—
PCI_AD17	K25	PCI	V_{DD_IO}	—
PCI_AD18	J26	PCI	V_{DD_IO}	—
PCI_AD19	K24	PCI	V_{DD_IO}	—
PCI_AD20	J25	PCI	V_{DD_IO}	—
PCI_AD21	H26	PCI	V_{DD_IO}	—
PCI_AD22	K23	PCI	V_{DD_IO}	—
PCI_AD23	J24	PCI	V_{DD_IO}	—
PCI_AD24	H24	PCI	V_{DD_IO}	—
PCI_AD25	J23	PCI	V_{DD_IO}	—
PCI_AD26	G25	PCI	V_{DD_IO}	—
PCI_AD27	J22	PCI	V_{DD_IO}	—
PCI_AD28	F26	PCI	V_{DD_IO}	—
PCI_AD29	G24	PCI	V_{DD_IO}	—
PCI_AD30	F24	PCI	V_{DD_IO}	—
PCI_AD31	H22	PCI	V_{DD_IO}	—
PCI_C/$\overline{BE}$0	P22	PCI	V_{DD_IO}	—
PCI_C/$\overline{BE}$1	N24	PCI	V_{DD_IO}	—
PCI_C/$\overline{BE}$2	L24	PCI	V_{DD_IO}	—
PCI_C/$\overline{BE}$3	G26	PCI	V_{DD_IO}	—
PCI_PAR	N22	PCI	V_{DD_IO}	—
$\overline{PCI\_FRAME}$	M23	PCI	V_{DD_IO}	1
$\overline{PCI\_TRDY}$	M22	PCI	V_{DD_IO}	1
$\overline{PCI\_IRDY}$	K26	PCI	V_{DD_IO}	1
$\overline{PCI\_STOP}$	M24	PCI	V_{DD_IO}	1
$\overline{PCI\_DEVSEL}$	L26	PCI	V_{DD_IO}	1
PCI_IDSEL	K22	PCI	V_{DD_IO}	—
$\overline{PCI\_SERR}$	M26	PCI	V_{DD_IO}	1
$\overline{PCI\_PERR}$	M25	PCI	V_{DD_IO}	1
$\overline{PCI\_REQ0}$	G23	PCI	V_{DD_IO}	1
$\overline{PCI\_REQ1}$	E26	PCI	V_{DD_IO}	1
$\overline{PCI\_REQ2}$	D26	PCI	V_{DD_IO}	1

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 7 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
$\overline{\text{PCI\_GNT0}}$	E25	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT1}}$	G22	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT2}}$	E24	PCI	V_{DD_IO}	—
PCI_CLK	C26	PCI	V_{DD_IO}	—
PSC Interface (61 Total)				
PSC_MCLK_IN	C17	General IO	V_{DD_IO}	—
PSC0_0	D16	General IO	V_{DD_IO}	—
PSC0_1	A17	General IO	V_{DD_IO}	—
PSC0_2	E15	General IO	V_{DD_IO}	—
PSC0_3	C16	General IO	V_{DD_IO}	—
PSC0_4	B16	General IO	V_{DD_IO}	—
PSC1_0	C15	General IO	V_{DD_IO}	—
PSC1_1	A16	General IO	V_{DD_IO}	—
PSC1_2	E14	General IO	V_{DD_IO}	—
PSC1_3	A15	General IO	V_{DD_IO}	—
PSC1_4	D14	General IO	V_{DD_IO}	—
PSC2_0	C14	General IO	V_{DD_IO}	—
PSC2_1	B14	General IO	V_{DD_IO}	—
PSC2_2	E13	General IO	V_{DD_IO}	—
PSC2_3	A14	General IO	V_{DD_IO}	—
PSC2_4	D13	General IO	V_{DD_IO}	—
PSC3_0	AF3	General IO	V_{DD_IO}	—
PSC3_1	AB5	General IO	V_{DD_IO}	—
PSC3_2	AC4	General IO	V_{DD_IO}	—
PSC3_3	AD4	General IO	V_{DD_IO}	—
PSC3_4	AF4	General IO	V_{DD_IO}	—
PSC4_0	AB1	General IO	V_{DD_IO}	—
PSC4_1	AA3	General IO	V_{DD_IO}	—
PSC4_2	AB3	General IO	V_{DD_IO}	—
PSC4_3	AA5	General IO	V_{DD_IO}	—
PSC4_4	AC2	General IO	V_{DD_IO}	—
PSC5_0	AC1	General IO	V_{DD_IO}	—
PSC5_1	AC3	General IO	V_{DD_IO}	—
PSC5_2	AD1	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 8 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
PSC5_3	AD2	General IO	V_{DD_IO}	—
PSC5_4	AE3	General IO	V_{DD_IO}	—
PSC6_0	A11	General IO	V_{DD_IO}	—
PSC6_1	C10	General IO	V_{DD_IO}	—
PSC6_2	A10	General IO	V_{DD_IO}	—
PSC6_3	B9	General IO	V_{DD_IO}	—
PSC6_4	A9	General IO	V_{DD_IO}	—
PSC7_0	B8	General IO	V_{DD_IO}	—
PSC7_1	E10	General IO	V_{DD_IO}	—
PSC7_2	C8	General IO	V_{DD_IO}	—
PSC7_3	A8	General IO	V_{DD_IO}	—
PSC7_4	A7	General IO	V_{DD_IO}	—
PSC8_0	E9	General IO	V_{DD_IO}	—
PSC8_1	D8	General IO	V_{DD_IO}	—
PSC8_2	C7	General IO	V_{DD_IO}	—
PSC8_3	B6	General IO	V_{DD_IO}	—
PSC8_4	E8	General IO	V_{DD_IO}	—
PSC9_0	C6	General IO	V_{DD_IO}	—
PSC9_1	D7	General IO	V_{DD_IO}	—
PSC9_2	E7	General IO	V_{DD_IO}	—
PSC9_3	D6	General IO	V_{DD_IO}	—
PSC9_4	E6	General IO	V_{DD_IO}	—
PSC10_0	C13	General IO	V_{DD_IO}	—
PSC10_1	B13	General IO	V_{DD_IO}	—
PSC10_2	A13	General IO	V_{DD_IO}	—
PSC10_3	C12	General IO	V_{DD_IO}	—
PSC10_4	E12	General IO	V_{DD_IO}	—
PSC11_0	A12	General IO	V_{DD_IO}	—
PSC11_1	B11	General IO	V_{DD_IO}	—
PSC11_2	C11	General IO	V_{DD_IO}	—
PSC11_3	E11	General IO	V_{DD_IO}	—
PSC11_4	D11	General IO	V_{DD_IO}	—
JTAG (5 Total)				
TCK	AB26	General IO	V_{DD_IO}	[2]

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 9 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
TDI	Y23	General IO	V_{DD_IO}	3
TDO	W22	General IO	V_{DD_IO}	—
TMS	Y25	General IO	V_{DD_IO}	3
$\overline{\text{TRST}}$	AA26	General IO	V_{DD_IO}	3
Test / Debug (2 Total)				
TEST	W25	General IO	V_{DD_IO}	4, 5
$\overline{\text{CKSTP\_OUT}}$	Y26	General IO	V_{DD_IO}	—
System Control (3 Total)				
$\overline{\text{HRESET}}$	W24	General IO	V_{DD_IO}	6, 2
$\overline{\text{PORESET}}$	W23	General IO	V_{DD_IO}	4, 2
$\overline{\text{SRESET}}$	V22	General IO	V_{DD_IO}	6, 2
System Clock (2 Total)				
SYS_XTALI	V24	Analog Input	SYS_PLL_AVDD	Oscillator Input
SYS_XTALO	W26	Analog Output	SYS_PLL_AVDD	Oscillator Output
RTC (3 Total)				
RTC_XTALI	C20	Analog Input	VBAT_RTC	Oscillator Input
RTC_XTALO	A20	Analog Output	VBAT_RTC	Oscillator Output
$\overline{\text{HIB\_MODE}}$	D18	Analog Output	VBAT_RTC	—
GP Input Only (4 Total)				
GPIO28	A19	Analog Input	VBAT_RTC	—
GPIO29	E17	Analog Input	VBAT_RTC	—
GPIO30	C18	Analog Input	VBAT_RTC	—
GPIO31	B18	Analog Input	VBAT_RTC	—
DDR Reference Voltage				
MVREF	AB11	Analog Input	Voltage Reference for SSTL input pads	
USB – PHY without Power and Ground Supplies (7 Total)				
USB_XTALI	C24	Analog Input	USB_PLL_PWR3	Oscillator Input
USB_XTALO	B24	Analog Output	USB_PLL_PWR3	Oscillator Output
USB_DP	A23	Analog IO	USB_VDDA	—
USB_DM	A22	Analog IO	USB_VDDA	—
USB_TPA	A24	Analog Output	—	USB PHY debug output
USB_VBUS	D21	Analog IO	—	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 10 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
USB_UID	E19	Analog Input	—	—
USB digital IOs (2 Total)				
USB2_VBUS_PWR_FAULT	B21	General IO	V_{DD_IO}	—
USB2_DRVVBUS	A21	General IO	V_{DD_IO}	—
SATA PHY without Power and Ground Supplies (7 Total)				
SATA_XTALI	C3	Analog Input	SATA_VDDA_3P3	Oscillator Input
SATA_XTALO	C2	Analog Output	SATA_VDDA_3P3	Oscillator Output
SATA_ANAVIZ	E5	Analog Output	—	SATA PHY debug output
SATA_TXN	E1	Analog Output	SATA_VDDA_1P2	—
SATA_TXP	F1	Analog Output	SATA_VDDA_1P2	—
SATA_RXP	A5	Analog Input	SATA_VDDA_1P2	—
SATA_RXN	A4	Analog Input	SATA_VDDA_1P2	—
Power and Ground Supplies (without SATA PHY and USB PHY)				
V_{DD_CORE}	K10, K11, K12, K13, K14, K15, K16, K17, L10, L17, M10, M17, N10, N17, P10, P17, R10, R17, T10, T17, U10, U11, U12, U13, U14, U15, U16, U17	Power	—	—
V_{DD_IO}	B10, B15, B25, D9, D10, D15, F11, F13, F14, F19, F23, F25, H21, J5, K2, K4, L23, L25, N6, N21, P6, P21, R2, R4, T23, T25, W6, W21, Y2, Y4, AA23, AA25, AE1, AE2, AE24, AE25, AF2, AF25	Power	—	—
$V_{DD\_MEM\_IO}$	AA8, AA13, AA14, AB18, AC5, AC10, AC14, AC20, AD9, AE5, AE10, AE15, AE20	Power	—	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 11 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
V_{SS}	A2, A3, A25, B1,B2, B3, B5, B7, B12, B17, B20, B22, B26, C1, C4, C23, C25, D2, D12, D17, D24, D25, E18, F2, F3, F4, F5, F6, F8, F10, F16, F17, F21, G5, H6, H23, H25, K6, K21, L6, L11, L12, L13, L14, L15, L16, L21, M2, M4, M11, M12, M13, M14, M15, M16, N5, N11, N12, N13, N14, N15, N16,	Ground	—	—
V_{SS}	N23, N25, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T6, T11, T12, T13, T14, T15, T16, T21, U2, U4, U6, U21, V23, V25, Y24, AA6, AA10, AA11, AA16, AA17, AA21, AB2, AB4, AB10, AB24, AC8, AC12, AC17, AC22, AD3, AD25, AE7, AE12, AE17, AE23, AE26	Ground	—	—
SYS_PLL_AVDD	T22	Analog Power	—	—
SYS_PLL_AVSS	U22	Analog Ground	—	—
CORE_PLL_AVDD	AA19	Analog Power	—	—
CORE_PLL_AVSS	AD23	Analog Ground	—	—
VBAT_RTC	D19	Power	—	—
AVDD_FUSEWR	C9	Power	—	—
MVTT0	AB7	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT1	AF9	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT2	AE11	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT3	AE14	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
Power and Ground Supplies (USB PHY)				
USB_PLL_GND	E23	Analog Ground	—	—
USB_PLL_PWR3	D23	Analog Power	—	—
USB_RREF	E22	Analog Power	—	—
USB_VSSA_BIAS	B23	Analog Ground	—	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 12 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
USB_VDDA_BIAS	D22	Analog Power	—	—
USB_VSSA	C22, E20, E21	Analog Ground	—	—
USB_VDDA	C21, D20	Analog Power	—	—
Power and Ground Supplies (SATA PHY)				
SATA_RESREF	E4	Analog Power	—	—
SATA_VDDA_3P3	D4	Analog Power	—	—
SATA_VDDA_1P2	C5, D1, E2	Analog Power	—	—
SATA_VDDA_VREG	D5	Analog Power	—	—
SATA_PLL_VDDA1P2	E3	Analog Power	—	—
SATA_PLL_VSSA	D3	Analog Ground	—	—
SATA_RX_VSSA	A6, B4	Analog Ground	—	—
SATA_TX_VSSA	G1	Analog Ground	—	—

1 This pins should have an external pull-up resistor. Follow PCI specification and see System Design Information.

2 This pin contains an enabled internal Schmitt trigger.

3 These JTAG pins have internal pull-up P-FETs. This pin can not be configured.

4 This pin is an input only. This pin can not be configured.

5 This test pin must be tied to V_{SS}.

6 This pin is an input or open-drain output. This pin can not be configured. There is an internal pull-up resistor implemented.

NOTE

This table indicates only the pins with permananently enabled internal pull-up, pull-down, or Schmitt trigger. Most of the digital I/O pins can be configured to enable internal pull-up, pull-down, or Schmitt trigger. See the *MPC5121e Microcontroller Reference Manual*, IO Control chapter.

3 Electrical and Thermal Characteristics

3.1 DC Electrical Characteristics

3.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5121e/MPC5123 DC Electrical characteristics. Table 4 gives the absolute maximum ratings.

Table 4. Absolute Maximum Ratings[1]

Characteristic	Symbol	Min	Max	Unit	SpecID
Supply voltage – e300 core and peripheral logic	V_{DD_CORE}	–0.3	1.47	V	D1.1
Supply voltage – I/O buffers	V_{DD_IO}, $V_{DD\_MEM\_IO}$	–0.3	3.6	V	D1.2
Input reference voltage (DDR/DDR2)	MVREF	–0.3	3.6	V	
Termination Voltage (DDR2)	MVTT	–0.3	3.6	V	
Supply voltage – System APLL, System Oscillator	SYS_PLL_AVDD	–0.3	3.6	V	D1.3
Supply voltage – e300 APLL	CORE_PLL_AVDD	–0.3	3.6	V	D1.4
Supply voltage – RTC (Hibernation)	VBAT_RTC	–0.3	3.6	V	D1.5
Supply voltage – FUSE Programming	AVDD_FUSEWR	–0.3	3.6	V	D1.6
Supply voltage – SATA PHY analog	SATA_VDDA_3P3	–0.3	3.6	V	D1.8
Supply voltage – SATA PHY voltage regulator	SATA_VDDA_VREG	–0.3	2.6	V	D1.9
Supply voltage – SATA PHY Tx/Rx	SATA_VDDA_1P2	–0.3	1.47	V	D1.10
Supply voltage – SATA PHY PLL	SATA_PLL_VDDA1P2	–0.3	1.47	V	D1.11
Supply voltage – USB PHY PLL and OSC	USB_PLL_PWR3	–0.3	3.6	V	D1.12
Supply voltage – USB PHY transceiver	USB_VDDA	–0.3	3.6	V	D1.13
Supply voltage – USB PHY bandgap bias	USB_VDDA_BIAS	–0.3	3.6	V	D1.14
Input voltage – USB PHY cable	USB_VBUS	–0.3	3.6	V	D1.15
Input voltage (V_{DD_IO})	Vin	–0.3	V_{DD_IO} + 0.3	V	D1.16
Input voltage ($V_{DD\_MEM\_IO}$)	Vin	–0.3	$V_{DD\_MEM\_IO}$ + 0.3	V	D1.17
Input voltage (VBAT_RTC)	Vin	–0.3	VBAT_RTC + 0.3	V	D1.18
Input voltage overshoot	Vinos	—	1	V	D1.19
Input voltage undershoot	Vinus	—	1	V	D1.20
Storage temperature range	Tstg	–55	150	°C	D1.21

1 Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

3.1.2 Recommended Operating Conditions

Table 5 gives the recommended operating conditions.

Table 5. Recommended Operating Conditions

Characteristic	Symbol	Min[1]	Typ	Max[1]	Unit	SpecID
Supply voltage – e300 core and peripheral logic	V_{DD_CORE}	1.33	1.4	1.47	V	D2.1
State Retention voltage – e300 core and peripheral logic [2]		1.08	—	—	V	D2.2
Supply voltage – standard I/O buffers	V_{DD_IO}	3.0	3.3	3.6	V	D2.3
Supply voltage – memory I/O buffers (DDR)	$V_{DD\_MEM\_IO\_DDR}$	2.3	2.5	2.7	V	D2.4
Supply voltage – memory I/O buffers (DDR2, LPDDR)	$V_{DD\_MEM\_IO\_DDR2}$ $V_{DD\_MEM\_IO\_LPDDR}$	1.7	1.8	1.9	V	D2.5
Input Reference Voltage (DDR/DDR2)	MVREF	0.49 × $V_{DD\_MEM\_IO}$	0.50 × $V_{DD\_MEM\_IO}$	0.51 × $V_{DD\_MEM\_IO}$	V	D2.6
Termination Voltage (DDR2)	MVTT	MVREF – 0.04	MVREF	MVREF + 0.04	V	D2.7
Supply voltage – System APLL, System Oscillator	SYS_PLL_AVDD	3.0	3.3	3.6	V	D2.8
Supply voltage – e300 APLL	CORE_PLL_AVDD	3.0	3.3	3.6	V	D2.9
Supply voltage – RTC (Hibernation)[3]	VBAT_RTC	3.0	3.3	3.6	V	D2.10
Supply voltage – FUSE Programming	AVDD_FUSEWR	3.3		3.6	V	D2.11
Supply voltage – SATA PHY analog and OSC	SATA_VDDA_3P3	3.0	3.3	3.6	V	D2.13
Supply voltage – SATA PHY voltage regulator	SATA_VDDA_VREG	1.7		2.6	V	D2.14
Supply voltage – SATA PHY Tx/Rx	SATA_VDDA_1P2	1.14	1.2	1.47	V	D2.15
Supply voltage – SATA PHY PLL	SATA_PLL_VDDA1P2	1.33	1.4	1.47	V	D2.16
Supply voltage – USB PHY PLL and OSC	USB_PLL_PWR3	3.0	3.3	3.6	V	D2.17
Supply voltage – USB PHY transceiver	USB_VDDA	3.0	3.3	3.6	V	D2.18
Supply voltage – USB PHY bandgap bias	USB_VDDA_BIAS	3.0	3.3	3.6	V	D2.19
Input voltage – USB PHY cable	USB_VBUS	1.4	—	3.6	V	D2.20
Input voltage – standard I/O buffers	Vin	0	—	V_{DD_IO}	V	D2.21
Input voltage – memory I/O buffers (DDR)	Vin_{DDR}	0	—	$V_{DD\_MEM\_IO\_DDR}$	V	D2.22
Input voltage – memory I/O buffers (DDR2)	Vin_{DDR2}	0	—	$V_{DD\_MEM\_IO\_DDR2}$	V	D2.23
Input voltage – memory I/O buffers (LPDDR)	Vin_{LPDDR}	0	—	$V_{DD\_MEM\_IO\_LPDR}$	V	D2.24
Ambient operating temperature range	TA	–40	—	+85	°C	D2.25
Junction operating temperature range	TJ	–40	—	+125	°C	D2.26

1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

2 The State Retention voltage can be applied to V_{DD_CORE} after the device is placed in Deep-Sleep mode.

3 VBAT_RTC should not be supplied by a battery of voltage less than 3.0 V.

3.1.3 DC Electrical Specifications

Table 6 gives the DC Electrical characteristics for the MPC5121e/MPC5123 at recommended operating conditions.

Table 6. DC Electrical Specifications

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL V_{DD_IO}	V_{IH}	0.51 × V_{DD_IO}	—	V	D3.1
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR}$	V_{IH}	MVREF + 0.15	—	V	D3.2
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR2}$	V_{IH}	MVREF + 0.125	—	V	D3.3
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_LPDDR}$	V_{IH}	0.7 × $V_{DD\_MEM\_IO\_LPDDR}$	—	V	D3.4
Input high voltage	Input type = PCI V_{DD_IO}	V_{IH}	0.5 × V_{DD_IO}	—	V	D3.5
Input high voltage	Input type = Schmitt V_{DD_IO}	V_{IH}	0.65 × V_{DD_IO}	—	V	D3.6
Input high voltage	SYS_XTALI crystal mode[1] Bypass mode[2]	CV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.7
Input high voltage	SATA_XTALI crystal mode Bypass mode	SV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.8
Input high voltage	USB_XTALI crystal mode Bypass mode	UV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.9
Input high voltage	RTC_XTALI crystal mode[3] Bypass mode[4]	RV_{IH}	(VBAT_RTC/5) + 0.5V (VBAT_RTC/2) + 0.4V	—	V	D3.10
Input low voltage	Input type = TTL V_{DD_IO}	V_{IL}	—	0.42 × V_{DD_IO}	V	D3.11
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR}$	V_{IL}	—	MVREF – 0.15	V	D3.12
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR2}$	V_{IL}	—	MVREF – 0.125	V	D3.13
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_LPDDR}$	V_{IL}	—	0.3 × $V_{DD\_MEM\_IO\_LPDDR}$	V	D3.14
Input low voltage	Input type = PCI V_{DD_IO}	V_{IL}	—	0.3 × V_{DD_IO}	V	D3.15
Input low voltage	Input type = Schmitt V_{DD_IO}	V_{IL}	—	0.35 × V_{DD_IO}	V	D3.16
Input low voltage	SYS_XTALI crystal mode Bypass mode	CV_{IL}	—	Vxtal – 0.4 (V_{DD_IO}/2) – 0.4	V	D3.17
Input low voltage	SATA_XTALI crystal mode Bypass mode	SV_{IL}	—	Vxtal – 0.4 V (V_{DD_IO}/2) – 0.4	V	D3.18
Input low voltage	USB_XTALI crystal mode Bypass mode	UV_{IL}	—	Vxtal – 0.4 (V_{DD_IO}/2) – 0.4	V	D3.19
Input low voltage	RTC_XTALI crystal mode Bypass mode	RV_{IL}	—	(VBAT_RTC/5) – 0.5 (VBAT_RTC/2) – 0.4	V	D3.20
Input leakage current	Vin = 0 or V_{DD_IO}/$V_{DD\_MEM\_IO\_DDR/2}$ (depending on input type)[5]	I_{IN}	–2.5	2.5	µA	D3.21
Input leakage current	SYS_XTALI Vin = 0 or V_{DD_IO}	I_{IN}	—	20	µA	D3.22

Table 6. DC Electrical Specifications (continued)

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input leakage current	RTC_XTALI Vin = 0 or V_{DD_IO}	I_{IN}	—	1.0	µA	D3.23
Input current, pullup resistor[6]	Pullup V_{DD_IO} Vin = VIL	I_{INpu}	25	150	µA	D3.24
Input current, pulldown resistor [8]	Pulldown V_{DD_IO} Vin = VIH	I_{INpd}	25	150	µA	D3.25
Output high voltage	IOH is driver dependent[7] V_{DD_IO}	V_{OH}	0.8 × V_{DD_IO}	—	V	D3.26
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OHDDR}	1.90	—	V	D3.27
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OHDDR2}	1.396	—	V	D3.28
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OHLPDDR}$	$V_{DD\_MEM\_IO}$ – 0.28	—	V	D3.28
Output low voltage	IOL is driver dependent[7] V_{DD_IO}	V_{OL}	—	0.2 × V_{DD_IO}	V	D3.30
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OLDDR}	—	0.36	V	D3.31
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OLDDR2}	—	0.28	V	D3.32
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OLLPDDR}$	—	0.28	V	D3.33
Differential cross point voltage (DDR MCK/$\overline{\text{MCK}}$)	—	V_{OXMCK}	0.5 × $V_{DD\_MEM\_IO}$ – 0.125	0.5 × $V_{DD\_MEM\_IO}$ + 0.125	V	D3.34
DC Injection Current Per Pin[8]	—	I_{CS}	–1.0	1.0	mA	D3.35
Input Capacitance (digital pins)	—	C_{in}	—	7	pF	D3.36
Input Capacitance (analog pins)	—	C_{in}	—	10	pF	D3.37
On Die Termination (DDR2)	—	R_{ODT}	120	180	Ω	D3.38

1 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, Vextal – Vxtal - 400mV criteria has to be met for oscillator's comparator to produce output clock.

2 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the EXTAL pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

3 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, drive one of the XTAL_IN or XTAL_OUT pins not connecting anything to other pin for the oscillator's comparator to produce output clock.

4 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the xtal_in pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

5 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.

6 Pullup current is measured at VIL and pulldown current is measured at VIH.

7 See Table 7 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 3.

8 All injection current is transferred to $V_{DD\_IO}/V_{DD\_MEM\_IO}$. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 7. I/O Pads—Drive Current, Slew Rate

Pad Type	Supply Voltage	Drive Select/Slew Rate Control	Rise time max (ns)	Fall time max (ns)	Current Ioh (mA)	Current Iol (mA)	SpecID
General IO	V_{DD_IO} = 3.3V	configuration 3 (11)	1.4	1.6	35	35	D3.41
		configuration 2 (10)	9.8	12			D3.42
		configuration 1 (01)	19	24			D3.43
		configuration 0 (00)	140	183			D3.44
DDR	$V_{DD\_MEM\_IO}$ = 2.5V (DDR)	configuration 3 (011)	2	2	16.2	16.2	D3.45
	$V_{DD\_MEM\_IO}$ = 1.8V (LPDDR)	configuration 0 (000)	1	1	4.6	4.6	D3.46
		configuration 1 (001)			8.1	8.1	D3.47
	$V_{DD\_MEM\_IO}$ = 1.8V (DDR2)	configuration 2 (010)	1	1	5.3	5.3	D3.48
		configuration 6 (110)			13.4	13.4	D3.49
PCI	V_{DD_IO} = 3.3V	configuration 1 (1)	1.4	1.4	11	17	D3.50
		configuration 0 (0)	2	2			D3.51

Notes:
1. General IO – Rise and Fall Times at Drive load 50pF.
2. PCI – Rise and Fall Times at Drive load 10pF.
3. DDR – for LPDDR/Mobile-DDR, slew rate is measured between 20% of $V_{DD\_MEM\_IO}$ and 80% of $V_{DD\_MEM\_IO}$.
4. DDR – for DDR, DDR2, rising signals, slew rate is measured between $V_{DD\_MEM\_IO} \times 0.5$ and ViH_{AC}. For falling signals, slew rate is measured between $V_{DD\_MEM\_IO} \times 0.5$ and ViL_{AC}.
5. DDR – Rise and Fall Times terminated at the destination with 50 ohm to MVTT ($0.5 \times V_{DD\_MEM\_IO}$), with 4 pF representing the DDR input capacitance.

3.1.4 Electrostatic Discharge

CAUTION

This device contains circuitry that protects against damage due to high-static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (GND or VDD). Table 10 gives package thermal characteristics for this device.

Table 8. ESD and Latch-Up Protection Characteristics

Symbol	Rating	Min	Max	Unit	SpecID
V_{HBM}	Human Body Model (HBM) – JEDEC JESD22-A114-B	2000	—	V	D4.1
V_{MM}	Machine Model (MM) – JEDEC JESD22-A115	200	—	V	D4.2
V_{CDM}	Charge Device Model (CDM) – JEDEC JESD22-C101	500	—	V	D4.3

3.1.5 Power Dissipation

Power dissipation of the MPC5121e/MPC5123 is caused by 4 different components: the dissipation of the internal or core digital logic (supplied by V_{DD_CORE}), the dissipation of the analog circuitry (supplied by SYS_PLL_AVDD and CORE_PLL_AVDD), the dissipation of the IO logic (supplied by $V_{DD\_MEM\_IO}$ and V_{DD_IO}) and the dissipation of the PHYs (supplied by own supplies). Table 9 details typical measured core and analog power dissipation figures for a range of operating modes. However, the dissipation due to the switching of the IO pins can not be given in general, but must be calculated for each application case using the following formula:

$$P_{IO} = P_{IOint} + \sum_{M} N \times C \times VDD\_IO^2 \times f \qquad \textit{Eqn. 1}$$

where N is the number of output pins switching in a group M, C is the capacitance per pin, V_{DD_IO} is the IO voltage swing, f is the switching frequency and P_{IOint} is the power consumed by the unloaded IO stage. The total power consumption of the device must not exceed the value that would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{analog} + P_{IO} + PPHYs \qquad \textit{Eqn. 2}$$

Table 9. Power Dissipation

Core Power Supply (V_{DD_CORE})			SpecID
Mode	High-Performance	Unit	
	e300 = 300 MHz, CSB = 200 MHz		
Operational[1]	800	mW	D5.1
Deep-Sleep[1]	1	mW	D5.2
Hibernation	20	uW	D5.3
PLL/OSC Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD)			
Typical	25	mW	D5.4
Unloaded I/O Power Supplies (V_{DD_IO}, $V_{DD\_MEM\_IO}$)			

Table 9. Power Dissipation (continued)

Core Power Supply (V_{DD_CORE})			SpecID
Mode	High-Performance	Unit	
	e300 = 300 MHz, CSB = 200 MHz		
Typical	300	mW	D5.5
PHY Power Supplies (USB_VDDA, SATA_VDDA)			
Typical	200	mW	D5.6

1 Typical core power is measured at V_{DD_CORE} = 1.4 V, T_j = 25 °C.

NOTE

The maximum power depends on the supply voltage, process corner, junction temperature, and the concrete application and clock configurations.
The worst case power consumption could reach a maximum of 2000 mW.

3.1.6 Thermal Characteristics

Table 10. Thermal Resistance Data

Rating	Board Layers	Symbol	TEPBGA	TEPBGA 2	Value	Unit	SpecID
Junction to Ambient Natural Convection[1,2]	Single layer board (1s)	$R_{\theta JA}$	31	24	30	°C/W	D6.1
Junction to Ambient Natural Convection[1,3]	Four layer board (2s2p)	$R_{\theta JMA}$	22	17	22	°C/W	D6.2
Junction to Ambient (@200 ft/min)[1,3]	Single layer board (1s)	$R_{\theta JMA}$	25	19	24	°C/W	D6.3
Junction to Ambient (@200 ft/min)[1,3]	Four layer board (2s2p)	$R_{\theta JMA}$	19	14	19	°C/W	D6.4
Junction to Board[4]	—	$R_{\theta JB}$	14	9	14	°C/W	D6.5
Junction to Case[5]	—	$R_{\theta JC}$	9	7	8	°C/W	D6.6
Junction to Package Top[6]	Natural Convection	Ψ_{JT}	2	7	2	°C/W	D6.7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending