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# MPC5200 Data Sheet

**NOTE**

The information in this document is subject to change. For the latest data on the MPC5200, visit www.freescale.com and proceed to the MPC5200 Product Summary Page.

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# 1 Overview

The MPC5200 integrates a high performance MPC603e series G2_LE core with a rich set of peripheral functions focused on communications and systems integration. The G2_LE core design is based on the PowerPC™ core architecture. MPC5200 incorporates an innovative BestComm I/O subsystem, which isolates routine maintenance of peripheral functions from the embedded G2_LE core. The MPC5200 contains a SDRAM/DDR Memory Controller, a flexible External Bus Interface, PCI Controller, USB, ATA, Ethernet, six Programmable Serial Controllers (PSC), $I^2C$, SPI, CAN, J1850, Timers, and GPIOs.

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# 2 Features

Key features are shown below.

- MPC603e series G2_LE core
  - Superscalar architecture
  - 760 MIPS at 400 MHz (-40 to +85 $^{o}$C)
  - 16 k Instruction cache, 16 k Data cache
  - Double precision FPU
  - Instruction and Data MMU
  - Standard and Critical interrupt capability
- SDRAM / DDR Memory Interface
  - up to 132-MHz operation
  - SDRAM and DDR SDRAM support
  - 256-MByte addressing range per CS, two CS available
  - 32-bit data bus
  - Built-in initialization and refresh
- Flexible multi-function External Bus Interface
  - Supports interfacing to ROM/Flash/SRAM memories or other memory mapped devices
  - 8 programmable Chip Selects
  - Non multiplexed data access using 8/16/32 bit databus with up to 26-bit address
  - Short or Long Burst capable
  - Multiplexed data access using 8/16/32 bit databus with up to 25-bit address
- Peripheral Component Interconnect (PCI) Controller
  - Version 2.2 PCI compatibility
  - PCI initiator and target operation
  - 32-bit PCI Address/Data bus
  - 33- and 66-MHz operation
  - PCI arbitration function
- ATA Controller
  - Version 4 ATA compatible external interface—IDE Disk Drive connectivity
- BestComm DMA subsystem
  - Intelligent virtual DMA Controller
  - Dedicated DMA channels to control peripheral reception and transmission
  - Local memory (SRAM 16 kBytes)
- 6 Programmable Serial Controllers (PSC), configurable for the following:
  - UART or RS232 interface

  - CODEC interface for Soft Modem, Master/Slave CODEC Mode, $I^2S$ and AC97
  - Full duplex SPI mode
  - IrDA mode from 2400 bps to 4 Mbps
- Fast Ethernet Controller (FEC)
  - Supports 100Mbps IEEE 802.3 MII, 10 Mbps IEEE 802.3 MII, 10 Mbps 7-wire interface
- Universal Serial Bus Controller (USB)
  - USB Revision 1.1 Host
  - Open Host Controller Interface (OHCI)
  - Integrated USB Hub, with two ports.
- Two Inter-Integrated Circuit Interfaces ($I^2C$)
- Serial Peripheral Interface (SPI)
- Dual CAN 2.0 A/B Controller (MSCAN)
  - Freescale Scalable Controller Area Network (FSCAN) architecture
  - Implementation of version 2.0A/B CAN protocol
  - Standard and extended data frames
- J1850 Byte Data Link Controller (BDLC)
  - J1850 Class B data communication network interface compatible and ISO compatible for low speed (<125 kbps) serial data communications in automotive applications.
  - Supports 4X mode, 41.6 kbps
  - In-frame response (IFR) types 0, 1, 2, and 3 supported
- Systems level features
  - Interrupt Controller supports four external interrupt request lines and 47 internal interrupt sources
  - GPIO/Timer functions
    - Up to 56 total GPIO pins (depending on functional multiplexing selections) that support a variety of interrupt/WakeUp capabilities.
    - Eight GPIO pins with timer capability supporting input capture, output compare, and pulse width modulation (PWM) functions
  - Real-time Clock with one-second resolution
  - Systems Protection (watch dog timer, bus monitor)
  - Individual control of functional block clock sources
  - Power management: Nap, Doze, Sleep, Deep Sleep modes
  - Support of WakeUp from low power modes by different sources (GPIO, RTC, CAN)

- Test/Debug features
  - — JTAG (IEEE 1149.1 test access port)
  - — Common On-chip Processor (COP) debug port
- On-board PLL and clock generation

Figure 1 shows a simplified MPC5200 block diagram.

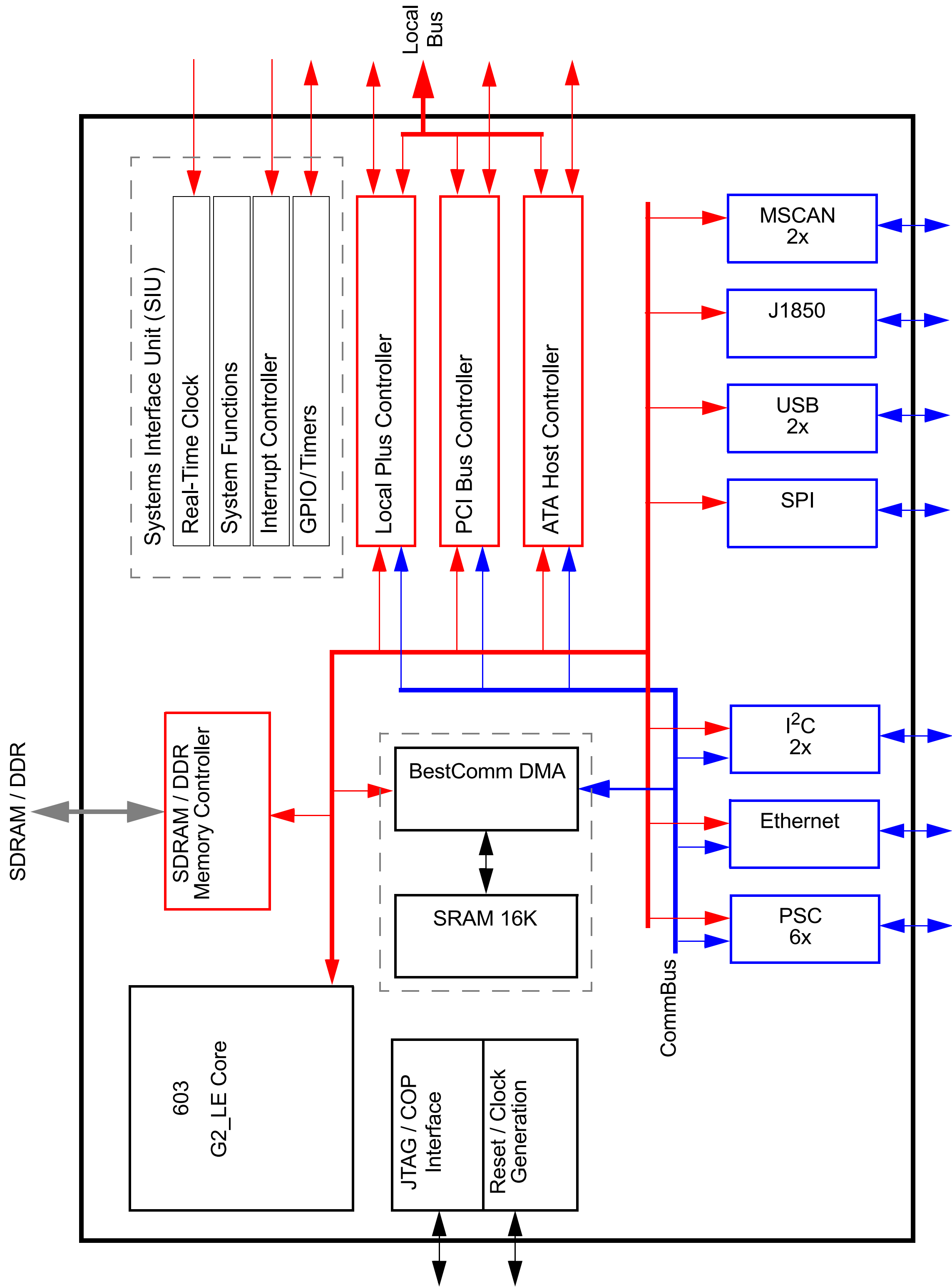



**Figure 1. Simplified Block Diagram—MPC5200**

# 3 Electrical and Thermal Characteristics

## 3.1 DC Electrical Characteristics

### 3.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5200 DC Electrical characteristics. Table 1 gives the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | Symbol | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|
| Supply voltage - G2_LE core and peripheral logic | VDD_CORE | –0.3 | 1.8 | V | D1.1 |
| Supply voltage - I/O buffers | VDD_IO, VDD_MEM_IO | –0.3 | 3.6 | V | D1.2 |
| Supply voltage - System APLL | SYS_PLL_AVDD | –0.3 | 2.1 | V | D1.3 |
| Supply voltage - G2_LE APLL | CORE_PLL_AVDD | –0.3 | 2.1 | V | D1.4 |
| Input voltage (VDD_IO) | Vin | –0.3 | VDD_IO + 0.3 | V | D1.5 |
| Input voltage (VDD_MEM_IO) | Vin | –0.3 | VDD_MEM_IO + 0.3 | V | D1.6 |
| Input voltage overshoot | Vinos | – | 1.0 | V | D1.7 |
| Input voltage undershoot | Vinus | – | 1.0 | V | D1.8 |
| Storage temperature range | Tstg | –55 | 150 | °C | D1.9 |

NOTES:
1 Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

### 3.1.2 Recommended Operating Conditions

Table 2 gives the recommended operating conditions.

**Table 2. Recommended Operating Conditions**

| Characteristic | Symbol | Min[1] | Max(1) | Unit | SpecID |
|---|---|---|---|---|---|
| Supply voltage - G2_LE core and peripheral logic | VDD_CORE | 1.42 | 1.58 | V | D2.1 |
| Supply voltage - standard I/O buffers | VDD_IO | 3.0 | 3.6 | V | D2.2 |
| Supply voltage - memory I/O buffers (SDR) | $VDD_MEM_IO_{SDR}$ | 3.0 | 3.6 | V | D2.3 |
| Supply voltage - memory I/O buffers (DDR) | $VDD_MEM_IO_{DDR}$ | 2.42 | 2.63 | V | D2.4 |
| Supply voltage - System APLL | SYS_PLL_AVDD | 1.42 | 1.58 | V | D2.5 |
| Supply voltage - G2_LE APLL | CORE_PLL_AVDD | 1.42 | 1.58 | V | D2.6 |
| Input voltage - standard I/O buffers | Vin | 0 | VDD_IO | V | D2.7 |
| Input voltage - memory I/O buffers (SDR) | $Vin_{SDR}$ | 0 | $VDD_MEM_IO_{SDR}$ | V | D2.8 |

**Table 2. Recommended Operating Conditions (continued)**

| Characteristic | Symbol | Min[1] | Max[(1)] | Unit | SpecID |
|---|---|---|---|---|---|
| Input voltage - memory I/O buffers (DDR) | $Vin_{DDR}$ | 0 | $VDD_MEM_IO_{DDR}$ | V | D2.9 |
| Ambient operating temperature range[2] | $T_A$ | -40 | +85 | °C | D2.10 |
| Extended ambient operating temperature range[3] | $T_{Aext}$ | -40 | +105 | °C | D2.11 |
| Die junction operating temperature range | Tj | -40 | +115 | °C | D2.12 |
| Extended die junction operating temperature range | Tjext | -40 | +125 | °C | D2.13 |

NOTES:
1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.
2 Maximum G2_LE core operating frequency is 400 MHz
3 Maximum G2_LE core operating frequency is 264 MHz

## 3.1.3 DC Electrical Specifications

Table 3 gives the DC Electrical characteristics for the MPC5200 at recommended operating conditions (see Table 2).

**Table 3. DC Electrical Specifications**

| Characteristic | Condition | Symbol | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|---|
| Input high voltage | Input type = TTL<br>$VDD_IO/VDD_MEM_IO_{SDR}$ | $V_{IH}$ | 2.0 | — | V | D3.1 |
| Input high voltage | Input type = TTL<br>$VDD_MEM_IO_{DDR}$ | $V_{IH}$ | 1.7 | — | V | D3.2 |
| Input high voltage | Input type = PCI<br>VDD_IO | $V_{IH}$ | 2.0 | — | V | D3.3 |
| Input high voltage | Input type = SCHMITT<br>VDD_IO | $V_{IH}$ | 2.0 | — | V | D3.4 |
| Input high voltage | SYS_XTAL_IN | $CV_{IH}$ | 2.0 | — | V | D3.5 |
| Input high voltage | RTC_XTAL_IN | $CV_{IH}$ | 2.0 | — | V | D3.6 |
| Input low voltage | Input type = TTL<br>$VDD_IO/VDD_MEM_IO_{SDR}$ | $V_{IL}$ | — | 0.8 | V | D3.7 |
| Input low voltage | Input type = TTL<br>$VDD_MEM_IO_{DDR}$ | $V_{IL}$ | — | 0.7 | V | D3.8 |
| Input low voltage | Input type = PCI<br>VDD_IO | $V_{IL}$ | — | 0.8 | V | D3.9 |
| Input low voltage | Input type = SCHMITT<br>VDD_IO | $V_{IL}$ | — | 0.8 | V | D3.10 |
| Input low voltage | SYS_XTAL_IN | $CV_{IL}$ | — | 0.8 | V | D3.11 |
| Input low voltage | RTC_XTAL_IN | $CV_{IL}$ | — | 0.8 | V | D3.12 |

**Table 3. DC Electrical Specifications (continued)**

| Characteristic | Condition | Symbol | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|---|
| Input leakage current | Vin = 0 or VDD_IO/VDD_IO_MEM$_{SDR}$ (depending on input type[1]) | $I_{IN}$ | — | ±10 | μA | D3.13 |
| Input leakage current | SYS_XTAL_IN Vin = 0 or VDD_IO | $I_{IN}$ | — | ±10 | μA | D3.14 |
| Input leakage current | RTC_XTAL_IN Vin = 0 or VDD_IO | $I_{IN}$ | — | ±10 | μA | D3.15 |
| Input current, pullup resistor | PULLUP VDD_IO Vin = 0 | $I_{INpu}$ | 40 | 109 | μA | D3.16 |
| Input current, pullup resistor - memory I/O buffers | PULLUP_MEM VDD_IO_MEM$_{SDR}$ Vin = 0 | $I_{INpu}$ | 41 | 111 | μA | D3.17 |
| Input current, pulldown resistor | PULLDOWN VDD_IO Vin = VDD_IO | $I_{INpd}$ | 36 | 106 | μA | D3.18 |
| Output high voltage | IOH is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$ | $V_{OH}$ | 2.4 | — | V | D3.19 |
| Output high voltage | IOH is driver dependent[2] VDD_IO_MEM$_{DDR}$ | $V_{OHDDR}$ | 1.7 | — | V | D3.20 |
| Output low voltage | IOL is driver dependent[2] VDD_IO, VDD_IO_MEM$_{SDR}$ | $V_{OL}$ | — | 0.4 | V | D3.21 |
| Output low voltage | IOL is driver dependent[2] VDD_IO_MEM$_{DDR}$ | $V_{OLDDR}$ | — | 0.4 | V | D3.22 |
| DC Injection Current Per Pin[3] | | $I_{CS}$ | -1.0 | 1.0 | mA | D3.23 |
| Capacitance | Vin = 0V, f = 1 MHz | $C_{in}$ | — | 15 | pF | D3.24 |

NOTES:
1 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.
2 See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 52.
3 All injection current is transferred to VDD_IO/VDD_IO_MEM. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

**Table 4. Drive Capability of MPC5200 Output Pins**

| Driver Type | Supply Voltage | $I_{OH}$ | $I_{OL}$ | Unit | SpecID |
|---|---|---|---|---|---|
| DRV4 | VDD_IO = 3.3V | 4 | 4 | mA | D3.25 |
| DRV8 | VDD_IO = 3.3V | 8 | 8 | mA | D3.26 |

**Table 4. Drive Capability of MPC5200 Output Pins (continued)**

| Driver Type | Supply Voltage | $I_{OH}$ | $I_{OL}$ | Unit | SpecID |
|---|---|---|---|---|---|
| DRV8_OD | VDD_IO = 3.3V | - | 8 | mA | D3.27 |
| DRV16_MEM | VDD_IO_MEM = 3.3V | 16 | 16 | mA | D3.28 |
| DRV16_MEM | VDD_IO_MEM = 2.5V | 16 | 16 | mA | D3.29 |
| PCI | VDD_IO = 3.3V | 16 | 16 | mA | D3.30 |

### 3.1.4 Electrostatic Discharge

**CAUTION**

This device contains circuitry that protects against damage due to high-static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (i.e., either GND or $V_{CC}$). Table 7 gives package thermal characteristics for this device.

**Table 5. ESD and Latch-Up Protection Characteristics**

| Sym | Rating | Min | Max | Unit | SpecID |
|---|---|---|---|---|---|
| $V_{HBM}$ | Human Body Model (HBM)—JEDEC JESD22-A114-B | 2000 | — | V | D4.1 |
| $V_{MM}$ | Machine Model (MM)—JEDEC JESD22-A115 | 200 | — | V | D4.2 |
| $V_{CDM}$ | Charge Device Model (CDM)—JEDEC JESD22-C101 | 500 | — | V | D4.3 |
| $I_{LAT}$ | Latch-up Current at $T_A$=85°C<br>positive<br>negative | <br>+100<br>-100 | — | mA | D4.4 |
| $I_{LAT}$ | Latch-up Current at $T_A$=27°C<br>positive<br>negative | <br>+200<br>-200 | — | mA | D4.5 |

### 3.1.5 Power Dissipation

Power dissipation of the MPC5200 is caused by 3 different components: the dissipation of the internal or core digital logic (supplied by VDD_CORE), the dissipation of the analog circuitry (supplied by SYS_PLL_AVDD and CORE_PLL_AVDD) and the dissipation of the IO logic (supplied by VDD_IO_MEM and VDD_IO). Table 6 details typical measured core and analog power dissipation figures for a range of operating modes. However, the dissipation due to the switching of the IO pins can not be given in general, but must be calculated by the user for each application case using the following formula

$$P_{IO} = P_{IOint} + \sum_{M} N \times C \times VDD_IO^2 \times f$$

where N is the number of output pins switching in a group M, C is the capacitance per pin, VDD_IO is the IO voltage swing, f is the switching frequency and PIOint is the power consumed by the unloaded IO stage. The total power consumption of the MPC5200 processor must not exceed the value, which would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{analog} + P_{IO}$$

**Table 6. Power Dissipation**

| Core Power Supply (VDD_CORE) | | | | | SpecID |
|---|---|---|---|---|---|
| Mode | SYS_XTAL/XLB/PCI/IPG/CORE (MHz) | | Unit | Notes | |
| | 33/66/33/33/264 | 33/132/66/132/396 | | | |
| | Typ | Typ | | | |
| Operational | 727.5 | 1080 | mW | 1,2 | D5.1 |
| Doze | — | 600 | mW | 1,3 | D5.2 |
| Nap | — | 225 | mW | 1,4 | D5.3 |
| Sleep | — | 225 | mW | 1,5 | D5.4 |
| Deep-Sleep | 52.5 | 52.5 | mW | 1,6 | D5.5 |
| PLL Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD) | | | | | |
| Mode | Typ | | Unit | Notes | |
| Typical | 2 | | mW | 7 | D5.6 |
| Unloaded I/O Power Supplies (VDD_IO, VDD_MEM_IO[8]) | | | | | |
| Mode | Typ | | Unit | Notes | |
| Typical | 33 | | mW | 9 | D5.7 |

NOTES:

1 Typical core power is measured at VDD_CORE = 1.5 V, Tj = 25 C

2 Operational power is measured while running an entirely cache-resident program with floating-point multiplication instructions in parallel with a continuous PCI transaction via BestComm.

3 Doze power is measured with the G2_LE core in Doze mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

4 Nap power is measured with the G2_LE core in Nap mode, the stem oscillator, System PLL and Core PLL are active, all other system modules are inactive

5 Sleep power is measured with the G2_LE core in Sleep mode, the stem oscillator, System PLL and Core PLL are active, all other system modules are inactive

6 Deep-Sleep power is measured with the G2_LE core in Sleep mode, the stem oscillator, System PLL, Core PLL and all other system modules are inactive

7 Typical PLL power is measured at SYS_PLL_AVDD = CORE_PLL_AVDD = 1.5 V, Tj = 25 C

8 IO power figures given in the table represent the worst case scenario. For the mem_io rail connected to 2.5V the IO power is expected to be lower and bounded by the worst case with VDD_MEM_IO connected to 3.3V.

9 Unloaded typical I/O power is measured in Deep-Sleep mode at VDD_IO = $VDD_MEM_IO_{SDR}$= 3.3 V, Tj = 25 C

### 3.1.6 Thermal Characteristics

**Table 7. Thermal Resistance Data**

| Rating | | | Value | Unit | Notes | SpecID |
|---|---|---|---|---|---|---|
| Junction to Ambient Natural Convection | Single layer board (1s) | $R_{\theta JA}$ | 30 | °C/W | 1,2 | D6.1 |
| Junction to Ambient Natural Convection | Four layer board (2s2p) | $R_{\theta JMA}$ | 22 | °C/W | 1,3 | D6.2 |
| Junction to Ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 24 | °C/W | 1,3 | D6.3 |
| Junction to Ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 19 | °C/W | 1,3 | D6.4 |
| Junction to Board | | $R_{\theta JB}$ | 14 | °C/W | 4 | D6.5 |
| Junction to Case | | $R_{\theta JC}$ | 8 | °C/W | 5 | D6.6 |
| Junction to Package Top | Natural Convection | $\Psi_{JT}$ | 2 | °C/W | 6 | D6.7 |

NOTES:

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### 3.1.7 Heat Dissipation

An estimation of the chip-junction temperature, $T_J$, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

$T_A$ = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$P_D$ = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance[1-3]. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 3}$$

where:

$T_T$ = thermocouple temperature on top of package (°C)

$\Psi_{JT}$ = thermal characterization parameter (°C/W)

$P_D$ = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 3.2 Oscillator and PLL Electrical Characteristics

The MPC5200 System requires a system-level clock input SYS_XTAL. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200 clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The G2_LE core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The G2_LE core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

### 3.2.1 System Oscillator Electrical Characteristics

**Table 8. System Oscillator Electrical Characteristics**

| Characteristic | Symbol | Notes | Min | Typical | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| SYS_XTAL frequency | $f_{sys_xtal}$ | | 15.6 | 33.3 | 35.0 | MHz | O1.1 |
| Oscillator start-up time | $t_{up_osc}$ | | — | — | 100 | μs | O1.2 |

### 3.2.2 RTC Oscillator Electrical Characteristics

**Table 9. RTC Oscillator Electrical Characteristics**

| Characteristic | Symbol | Notes | Min | Typical | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| RTC_XTAL frequency | $f_{rtc_xtal}$ | | — | 32.768 | — | kHz | O2.1 |

### 3.2.3 System PLL Electrical Characteristics

**Table 10. System PLL Specifications**

| Characteristic | Symbol | Notes | Min | Typical | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| SYS_XTAL frequency | $f_{sys_xtal}$ | 1 | 15.6 | 33.3 | 35.0 | MHz | O3.1 |
| SYS_XTAL cycle time | $T_{sys_xtal}$ | (1) | 66.6 | 30.0 | 28.5 | ns | O3.2 |
| SYS_XTAL clock input jitter | $t_{jitter}$ | 2 | — | — | 150 | ps | O3.3 |
| System VCO frequency | $f_{VCOsys}$ | (1) | 250 | 533 | 800 | MHz | O3.4 |
| System PLL relock time | $t_{lock}$ | 3 | — | — | 100 | μs | O3.5 |

NOTES:

1 The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.

2 This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.

3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

### 3.2.4 G2_LE Core PLL Electrical Characteristics

The internal clocking of the G2_LE core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

**Table 11. G2_LE PLL Specifications**

| Characteristic | Symbol | Notes | Min | Typical | Max | Unit | SpecID |
|---|---|---|---|---|---|---|---|
| G2_LE frequency | $f_{core}$ | 1 | 50 | — | 550 | MHz | O4.1 |
| G2_LE cycle time | $t_{core}$ | (1) | 2.85 | — | 40.0 | ns | O4.2 |
| G2_LE VCO frequency | $f_{VCOcore}$ | (1) | 400 | — | 1200 | MHz | O4.3 |
| G2_LE input clock frequency | $f_{XLB_CLK}$ | | 25 | — | 367 | MHz | O4.4 |
| G2_LE input clock cycle time | $t_{XLB_CLK}$ | | 2.73 | — | 50.0 | ns | O4.5 |
| G2_LE input clock jitter | $t_{jitter}$ | 2 | — | — | 150 | ps | O4.6 |
| G2_LE PLL relock time | $t_{lock}$ | 3 | — | — | 100 | µs | O4.7 |

NOTES:

1 The XLB_CLK frequency and G2_LE PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and G2_LE PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.

2 This represents total input jitter - short term and long term combined - and is guaranteed by design. Two different types of jitter can exist on the input to core_sysclk, systemic and true random jitter. True random jitter is rejected, but the PLL. Systemic jitter will be passed into and through the PLL to the internal clock circuitry, directly reducing the operating frequency.

3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable Vdd and core_sysclk are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

## 3.3 AC Electrical Characteristics

Hyperlinks to the indicated timing specification sections are provided below.

- AC Operating Frequency Data
- Clock AC Specifications
- Resets
- External Interrupts
- SDRAM
- PCI
- Local Plus Bus
- ATA
- Ethernet
- USB
- SPI
- MSCAN
- $I^2C$
- J1850
- PSC
- GPIOs and Timers
- IEEE 1149.1 (JTAG) AC Specifications

AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

- TA = -40 to 85 $^{o}$C
- Tj = -40 to 115 $^{o}$C
- VDD_CORE = 1.42 to 1.58 V
  VDD_IO = 3.0 to 3.6 V
- Input conditions:
  All Inputs: tr, tf <= 1 ns
- Output Loading:
  All Outputs: 50 pF

## 3.3.1 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200.

**Table 12. Clock Frequencies**

| | | Min | Max | Units | SpecID |
|---|---|---|---|---|---|
| 1 | G2_LE Processor Core | — | 400 | MHz | A1.1 |
| 2 | SDRAM Clock | — | 133 | MHz | A1.2 |
| 3 | XL Bus Clock | — | 133 | MHz | A1.3 |
| 4 | IP Bus Clock | — | 133 | MHz | A1.4 |
| 5 | PCI / Local Plus Bus Clock | — | 66 | MHz | A1.5 |
| 6 | PLL Input Range | 15.6 | 35 | MHz | A1.6 |

## 3.3.2 Clock AC Specifications

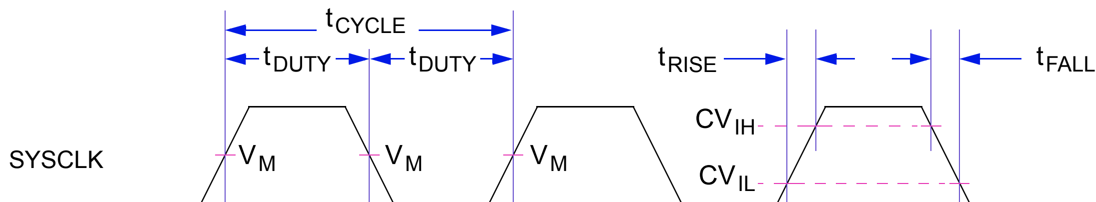



**Figure 2. Timing Diagram—SYS_XTAL_IN**

**Table 13. SYS_XTAL_IN Timing**

| Sym | Description | Min | Max | Units | SpecID |
|---|---|---|---|---|---|
| $t_{CYCLE}$ | SYS_XTAL_IN cycle time.[1] | 28.6 | 64.1 | ns | A2.1 |
| $t_{RISE}$ | SYS_XTAL_IN rise time. | — | 5.0 | ns | A2.2 |
| $t_{FALL}$ | SYS_XTAL_IN fall time. | — | 5.0 | ns | A2.3 |
| $t_{DUTY}$ | SYS_XTAL_IN duty cycle (measured at $V_M$).[2] | 40.0 | 60.0 | % | A2.4 |
| $CV_{IH}$ | SYS_XTAL_IN input voltage high | 2.0 | — | V | A2.5 |
| $CV_{IL}$ | SYS_XTAL_IN input voltage low | — | 0.8 | V | A2.6 |

NOTES:
[1] **CAUTION**—The SYS_XTAL_IN frequency and system PLL_CFG[0-6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the MPC5200 User Manual [1].
[2] SYS_XTAL_IN duty cycle is measured at $V_M$.

### 3.3.3 Resets

The MPC5200 has three reset pins:

- $\overline{\text{PORRESET}}$ - Power on Reset
- $\overline{\text{HRESET}}$ - Hard Reset
- $\overline{\text{SRESET}}$ - Software Reset

These signals are asynchronous I/O signals and can be asserted at any time. The input side uses a Schmitt trigger and requires the same input characteristics as other MPC5200 inputs, as specified in the DC Electrical Specifications section. Table 14 specifies the pulse widths of the Reset inputs.

**Table 14. Reset Pulse Width**

| Name | Description | Min Pulse Width | Max Pulse Width | Reference Clock | SpecID |
|---|---|---|---|---|---|
| $\overline{\text{PORRESET}}$ | Power On Reset | $t_{VDD_stable}+t_{up_osc}+t_{lock}$ | — | SYS_XTAL_IN | A3.1 |
| $\overline{\text{HRESET}}$ | Hardware Reset | 4 clock cycles | — | SYS_XTAL_IN | A3.2 |
| $\overline{\text{SRESET}}$ | Software Reset | 4 clock cycles | — | SYS_XTAL_IN | A3.3 |

Notes:
1. For $\overline{\text{PORRESET}}$ the value of the minimum pulse width reflects the power on sequence. If $\overline{\text{PORRESET}}$ is asserted afterwards its minimum pulse width equals the minimum given for $\overline{\text{HRESET}}$ related to the same reference clock.
2. The $t_{VDD_stable}$ describes the time which is needed to get all power supplies stable.
3. For $t_{lock,}$ refer to the Oscillator/PLL section of this specification for further details.
4. For $t_{up_osc,}$ refer to the Oscillator/PLL section of this specification for further details.
5. Following the deassertion of $\overline{\text{PORRESET}}$, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ remain low for 4096 reference clock cycles.
6. The deassertion of $\overline{\text{HRESET}}$ for at least the minimum pulse width forces the internal resets to be active for an additional 4096 clock cycles.

**NOTE**

As long as VDD is not stable the $\overline{\text{HRESET}}$ output is not stable.

**Table 15. Reset Rise / Fall Timing**

| Description | Min | Max | Unit | SpecID |
|---|---|---|---|---|
| $\overline{\text{PORRESET}}$ fall time | — | 1 | ms | A3.4 |
| $\overline{\text{PORRESET}}$ rise time | — | 1 | ms | A3.5 |
| $\overline{\text{HRESET}}$ fall time | — | 1 | ms | A3.6 |
| $\overline{\text{HRESET}}$ rise time | — | 1 | ms | A3.7 |
| $\overline{\text{SRESET}}$ fall time | — | 1 | ms | A3.8 |
| $\overline{\text{SRESET}}$ rise time | — | 1 | ms | A3.9 |

For additional information, see the MPC5200 User Manual [1].

**NOTE**

Make sure that the $\overline{\text{PORRESET}}$ does not carry any glitches. The MPC5200 has no filter to prevent them from getting into the chip.

**NOTE**

$\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ must have a monotonous rise time.

### 3.3.3.1 Reset Configuration Word

During reset ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) the Reset Configuration Word is cached in the related Reset Configuration Word Register with each rising edge of the SYS_XTAL signal. If both resets ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) are inactive (high), the contents of this register get locked after two further SYS_XTAL cycles (see Figure 3).

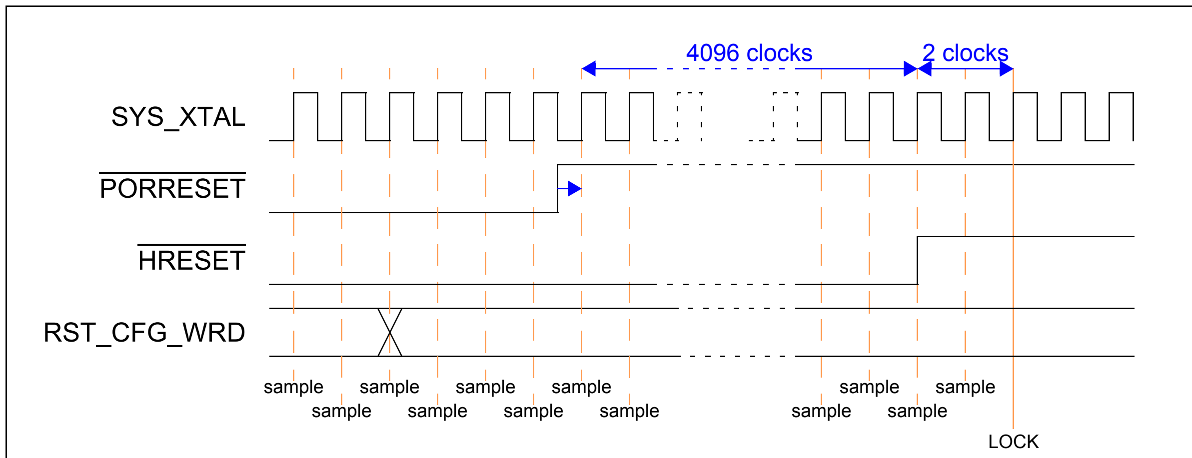



**Figure 3. Reset Configuration Word Locking**

**NOTE**

Beware of changing the values on the pins of the reset configuration word after the deassertion of PORRESET. This may cause problems because it may change the internal clock ratios and so extend the PLL locking process.

## 3.3.4 External Interrupts

The MPC5200 provides three different kinds of external interrupts:

- Four IRQ interrupts
- Eight GPIO interrupts with simple interrupt capability (not available in power-down mode)
- Eight WakeUp interrupts (special GPIO pins)

The propagation of these three kinds of interrupts to the core is shown in the following graphic:

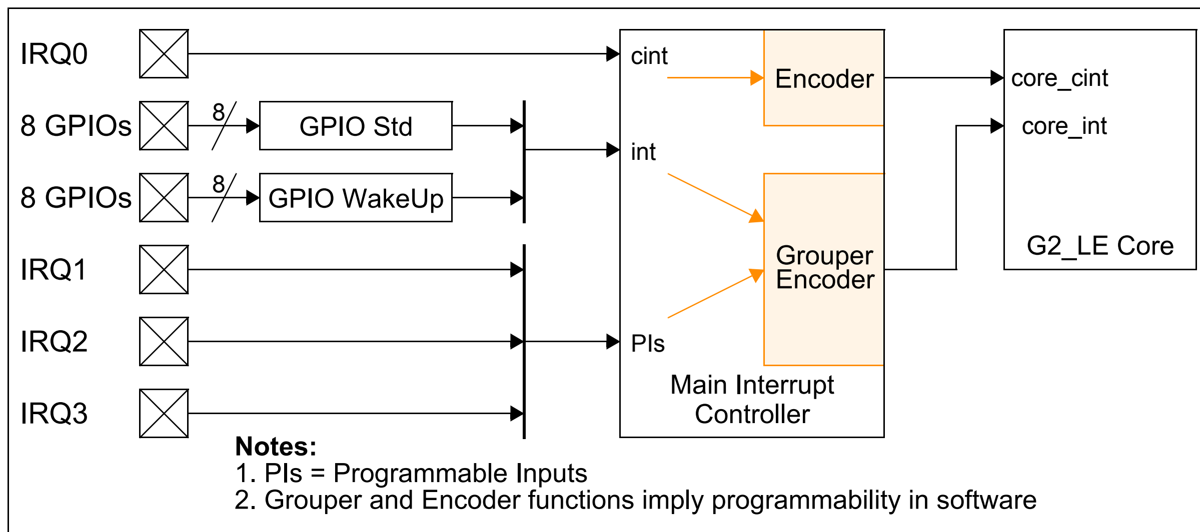



**Figure 4. External interrupt scheme**

Due to synchronization, prioritization, and mapping of external interrupt sources, the propagation of external interrupts to the core processor is delayed by several IP_CLK clock cycles. The following table specifies the interrupt latencies in IP_CLK cycles. The IP_CLK frequency is programmable in the Clock Distribution Module (see Note Table 16).

**Table 16. External interrupt latencies**

| Interrupt Type | Pin Name | Clock Cycles | Reference Clock | Core Interrupt | SpecID |
|---|---|---|---|---|---|
| Interrupt Requests | IRQ0 | 10 | IP_CLK | critical (cint) | A4.1 |
| | IRQ0 | 10 | IP_CLK | normal (int) | A4.2 |
| | IRQ1 | 10 | IP_CLK | normal (int) | A4.3 |
| | IRQ2 | 10 | IP_CLK | normal (int) | A4.5 |
| | IRQ3 | 10 | IP_CLK | normal (int) | A4.6 |

**Table 16. External interrupt latencies (continued)**

| Interrupt Type | Pin Name | Clock Cycles | Reference Clock | Core Interrupt | SpecID |
|---|---|---|---|---|---|
| Standard GPIO Interrupts | GPIO_PSC3_4 | 12 | IP_CLK | normal (int) | A4.7 |
| | GPIO_PSC3_5 | 12 | IP_CLK | normal (int) | A4.8 |
| | GPIO_PSC3_8 | 12 | IP_CLK | normal (int) | A4.9 |
| | GPIO_USB_9 | 12 | IP_CLK | normal (int) | A4.10 |
| | GPIO_ETHI_4 | 12 | IP_CLK | normal (int) | A4.11 |
| | GPIO_ETHI_5 | 12 | IP_CLK | normal (int) | A4.12 |
| | GPIO_ETHI_6 | 12 | IP_CLK | normal (int) | A4.13 |
| | GPIO_ETHI_7 | 12 | IP_CLK | normal (int) | A4.14 |
| GPIO WakeUp Interrupts | GPIO_PSC1_4 | 12 | IP_CLK | normal (int) | A4.15 |
| | GPIO_PSC2_4 | 12 | IP_CLK | normal (int) | A4.16 |
| | GPIO_PSC3_9 | 12 | IP_CLK | normal (int) | A4.17 |
| | GPIO_ETHI_8 | 12 | IP_CLK | normal (int) | A4.18 |
| | GPIO_IRDA_0 | 12 | IP_CLK | normal (int) | A4.19 |
| | DGP_IN0 | 12 | IP_CLK | normal (int) | A4.20 |
| | DGP_IN1 | 12 | IP_CLK | normal (int) | A4.21 |

Notes:
1) The frequency of IP_CLK depends on register settings in Clock Distribution Module. See the MPC5200 User Manual [1].
2) The interrupt latency descriptions in the table above are related to non competitive, non masked but enabled external interrupt sources. Take care of interrupt prioritization which may increase the latencies.

Since all external interrupt signals are synchronized into the internal processor bus clock domain, each of these signals has to exceed a minimum pulse width of more than one IP_CLK cycle.

**Table 17. Minimum pulse width for external interrupts to be recognized**

| Name | Min Pulse Width | Max Pulse Width | Reference Clock | SpecID |
|---|---|---|---|---|
| All external interrupts (IRQs, GPIOs) | > 1 clock cycle | — | IP_CLK | A4.22 |

NOTES:
1) The frequency of the IP_CLK depends on the register settings in Clock Distribution Module. See the MPC5200 User Manual [1] for further information.
2) If the same interrupt occurs a second time while its interrupt service routine has not cleared the former one, the second interrupt will not be recognized at all.

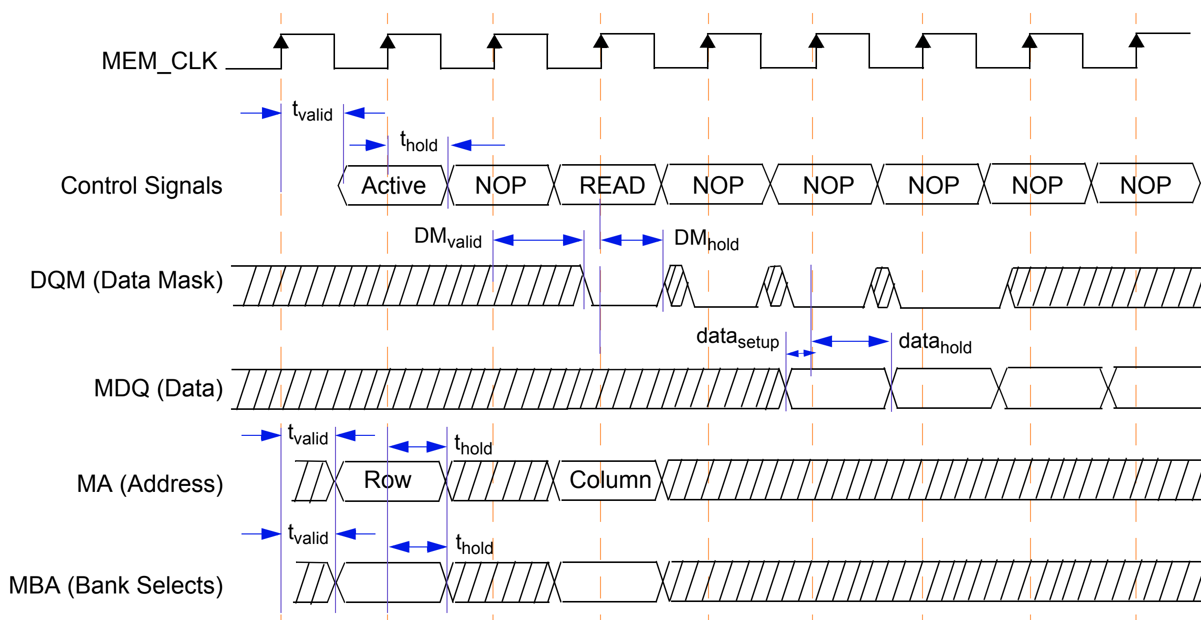
Besides synchronization, prioritization, and mapping the latency of an external interrupt to the start of its associated interrupt service routine also depends on the following conditions: To get a minimum interrupt service response time, it is recommended to enable the instruction cache and set up the maximum core clock, XL bus, and IP bus frequencies (depending on board design and programming). In addition, it is advisable to execute an interrupt handler, which has been implemented in assembly code.

## 3.3.5 SDRAM

### 3.3.5.1 Memory Interface Timing-Standard SDRAM Read Command

**Table 18. Standard SDRAM Memory Read Timing**

| Sym | Description | Min | Max | Units | SpecID |
|---|---|---|---|---|---|
| $t_{mem_clk}$ | MEM_CLK period | 7.5 | — | ns | A5.1 |
| $t_{valid}$ | Control Signals, Address and MBA Valid after rising edge of MEM_CLK | — | $t_{mem_clk}$*0.5+0.4 | ns | A5.2 |
| $t_{hold}$ | Control Signals, Address and MBA Hold after rising edge of MEM_CLK | $t_{mem_clk}$*0.5 | — | ns | A5.3 |
| $DM_{valid}$ | DQM valid after rising edge of MEM_CLK | — | $t_{mem_clk}$*0.25+0.4 | ns | A5.4 |
| $DM_{hold}$ | DQM hold after rising edge of MEM_CLK | $t_{mem_clk}$*0.25-0.7 | — | ns | A5.5 |
| $data_{setup}$ | MDQ setup to rising edge of MEM_CLK | — | 0.3 | ns | A5.6 |
| $data_{hold}$ | MDQ hold after rising edge of MEM_CLK | 0.2 | — | ns | A5.7 |




NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM_WE}}$, $\overline{\text{MEM_CS}}$, $\overline{\text{MEM_CS1}}$ and CLK_EN

**Figure 5. Timing Diagram—Standard SDRAM Memory Read Timing**

### 3.3.5.2 Memory Interface Timing-Standard SDRAM Write Command

In Standard SDRAM, all signals are activated on the Mem_clk from the Memory Controller and captured on the Mem_clk clock at the memory device.

**Table 19. Standard SDRAM Write Timing**

| Sym | Description | Min | Max | Units | SpecID |
|---|---|---|---|---|---|
| $t_{mem_clk}$ | MEM_CLK period | 7.5 | — | ns | A5.8 |
| $t_{valid}$ | Control Signals, Address and MBA Valid after rising edge of MEM_CLK | — | $t_{mem_clk}$*0.5+0.4 | ns | A5.9 |
| $t_{hold}$ | Control Signals, Address and MBA Hold after rising edge of MEM_CLK | $t_{mem_clk}$*0.5 | — | ns | A5.10 |
| $DM_{valid}$ | DQM valid after rising edge of MEM_CLK | — | $t_{mem_clk}$*0.25+0.4 | ns | A5.11 |
| $DM_{hold}$ | DQM hold after rising edge of Mem_clk | $t_{mem_clk}$*0.25-0.7 | — | ns | A5.12 |
| $data_{valid}$ | MDQ valid after rising edge of MEM_CLK | — | $t_{mem_clk}$*0.75+0.4 | ns | A5.13 |
| $data_{hold}$ | MDQ hold after rising edge of MEM_CLK | $t_{mem_clk}$*0.75-0.7 | — | ns | A5.14 |

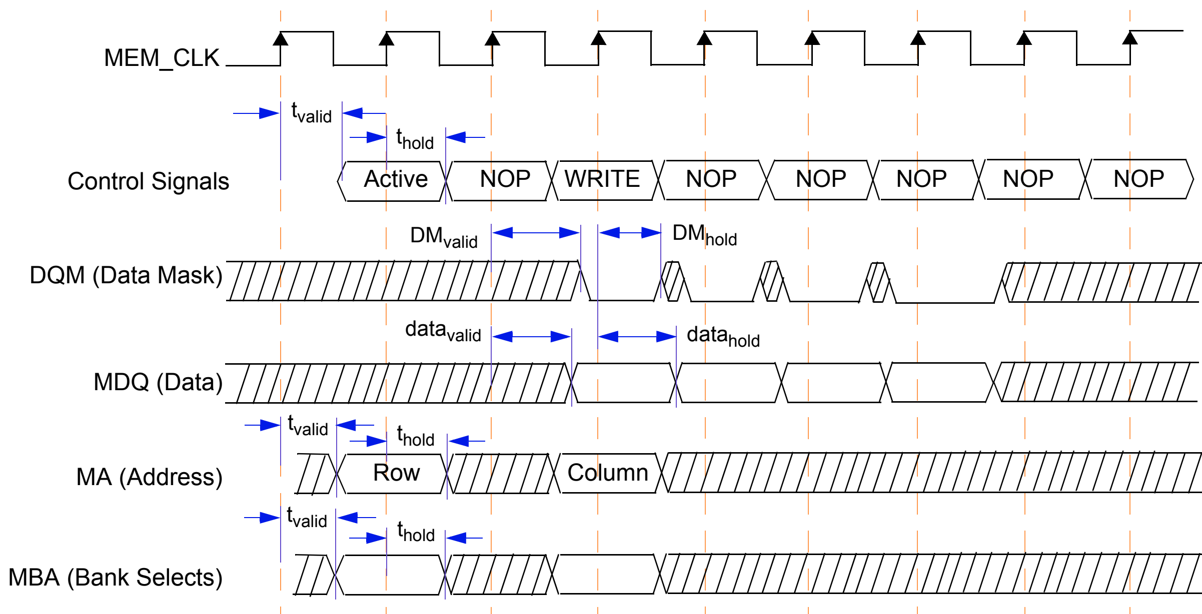



**Figure 6. Timing Diagram—Standard SDRAM Memory Write Timing**

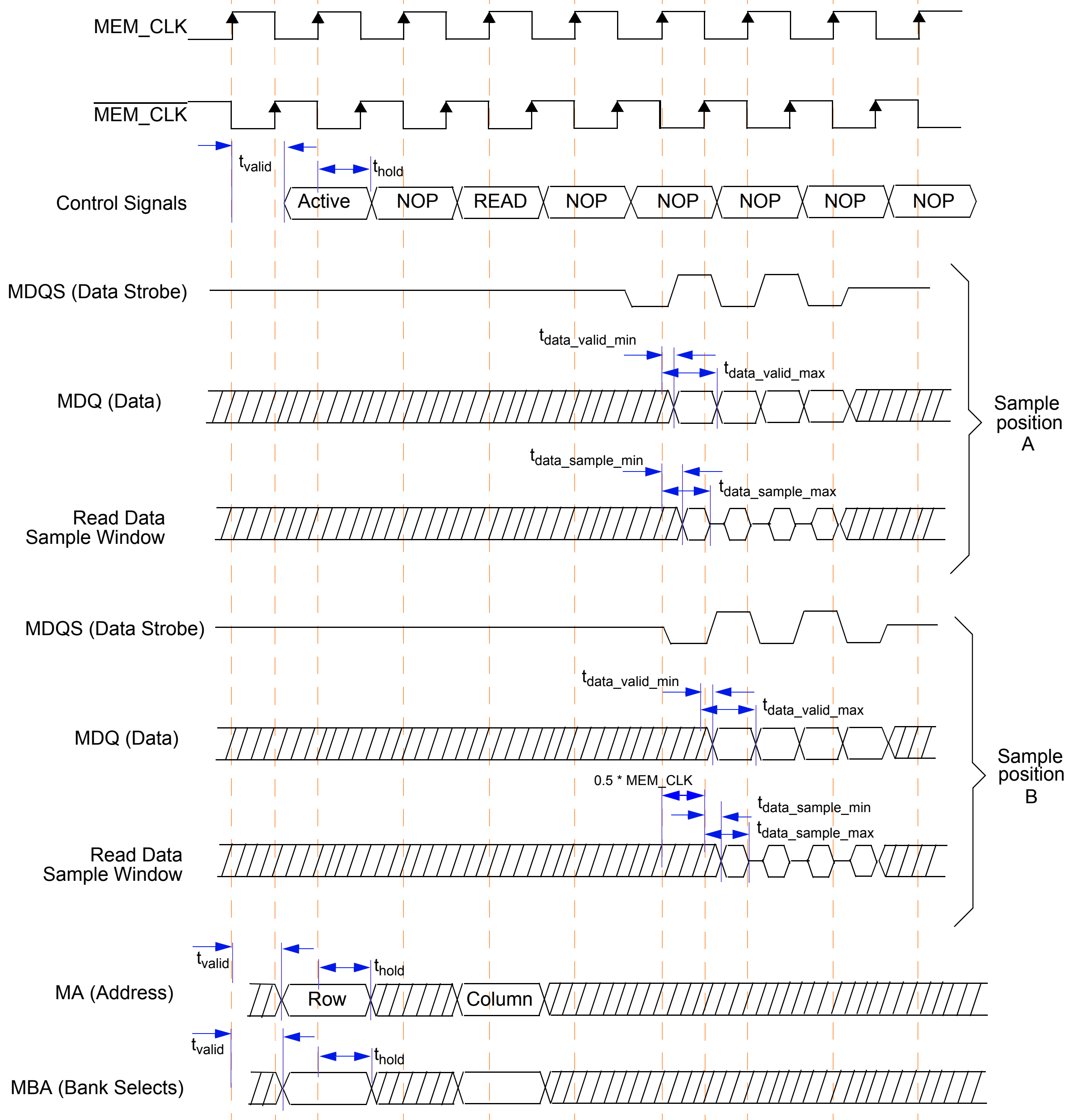
## 3.3.5.3 Memory Interface Timing-DDR SDRAM Read Command

The SDRAM Memory Controller uses an internally skewed clock for reading DDR memory. The programmable bits in the Reset Configuration Register used to account for unknown board delays are in the CDM module. The internal read clock can be delayed up to 3 ns under worst operating conditions in 32 increments of 95 ps, (1.4 ns in 45 ps increments under best case operating conditions) by programming the CDM Reset Configuration Register tap delay bits. Note: These bits in the CDM Reset Configuration register are not ‘reset configured’ but have a hard coded reset value **and** are writable during operation.

**Table 20. DDR SDRAM Memory Read Timing**

| Sym | Description | Min | Max | Units | SpecID |
|---|---|---|---|---|---|
| $t_{mem_clk}$ | MEM_CLK period | 7.5 | — | ns | A5.15 |
| $t_{valid}$ | Control Signals, Address and MBA valid after rising edge of MEM_CLK | — | $t_{mem_clk}$*0.5+0.4 | ns | A5.16 |
| $t_{hold}$ | Control Signals, Address and MBA hold after rising edge of MEM_CLK | $t_{mem_clk}$*0.5 | — | ns | A5.17 |
| $t_{data_sample_max}$ | Read Data sample window | — | 4.59[1] | ns | A5.18 |
| $t_{data_sample_min}$ | Read Data sample window | 1.55[2] | — | ns | A5.19 |

NOTES:
1 Calculated with maximum number of Tap delay, 31 Tap delay are selected.
2 Calculated with minimum number of Tap delay, 0 Tap delay are selected.




Sample position A: data are sampled on the expected edge of MEM_CLK, the MDQS signal indicate the valid data

Sample position B: data are sampled on a later edge of MEM_CLK, SDRAM controller is waiting for the vaild MDQS signal

NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM_WE}}$, $\overline{\text{MEM_CS}}$, $\overline{\text{MEM_CS1}}$ and CLK_EN

**Figure 7. Timing Diagram—DDR SDRAM Memory Read Timing**

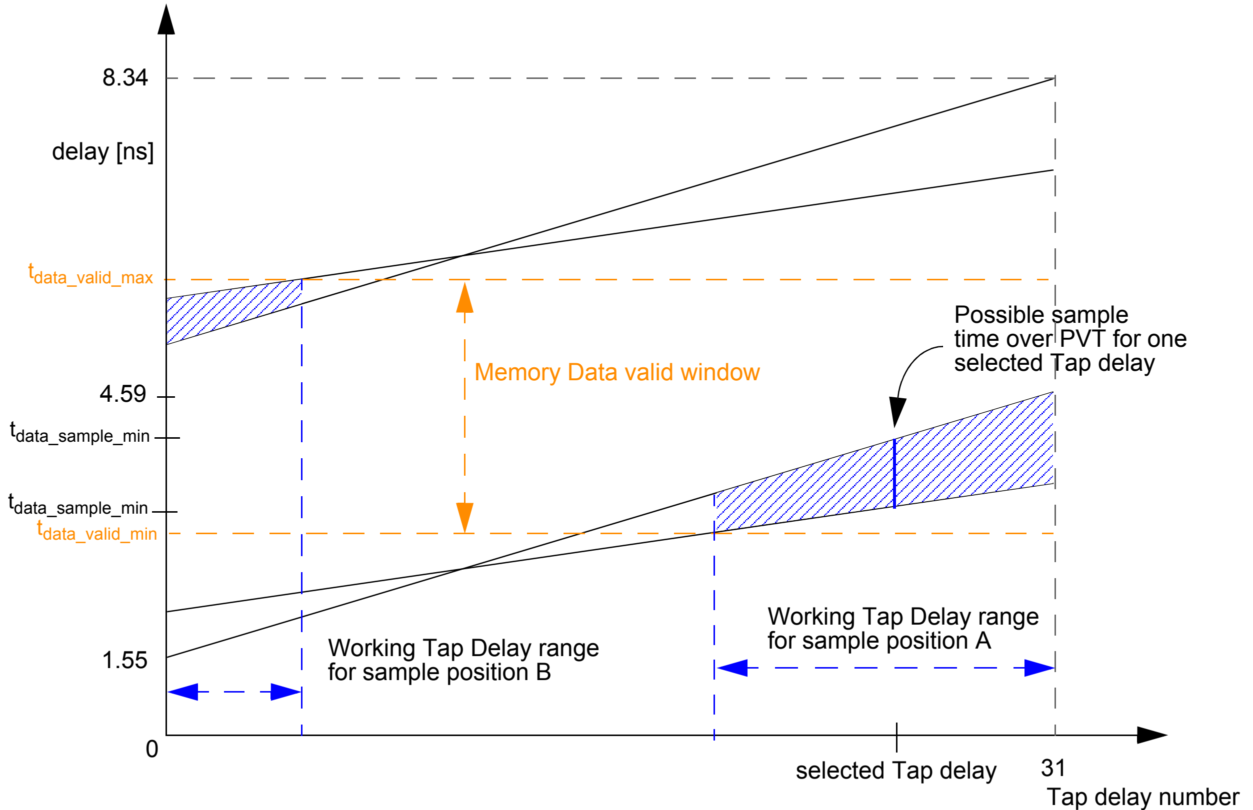



**Figure 8. Read Data sample window depend on the number of Tap delay**

The position of the $t_{data_valid}$ window is depend on the clock / data flight time on the board. The MDQS signal indicate if the read data are valid. If the controller is not able to detect a valid MDQS signal on the sample time (sample position A) then the controller will look for valid MDQS / data on the next edge of the MEM_CLK signal (sample position B). Depend on the board travel time, different working tap delay configurations are possible. For a fast connection the data will be sampled with the next edge of MEM_CLK, this shows Figure 8, sample position A. With a longer connection maybe two sample positions are possible. Figure 8 shows a example with two working sample position (A and B). With a bigger board delay only sample position B will be possible.

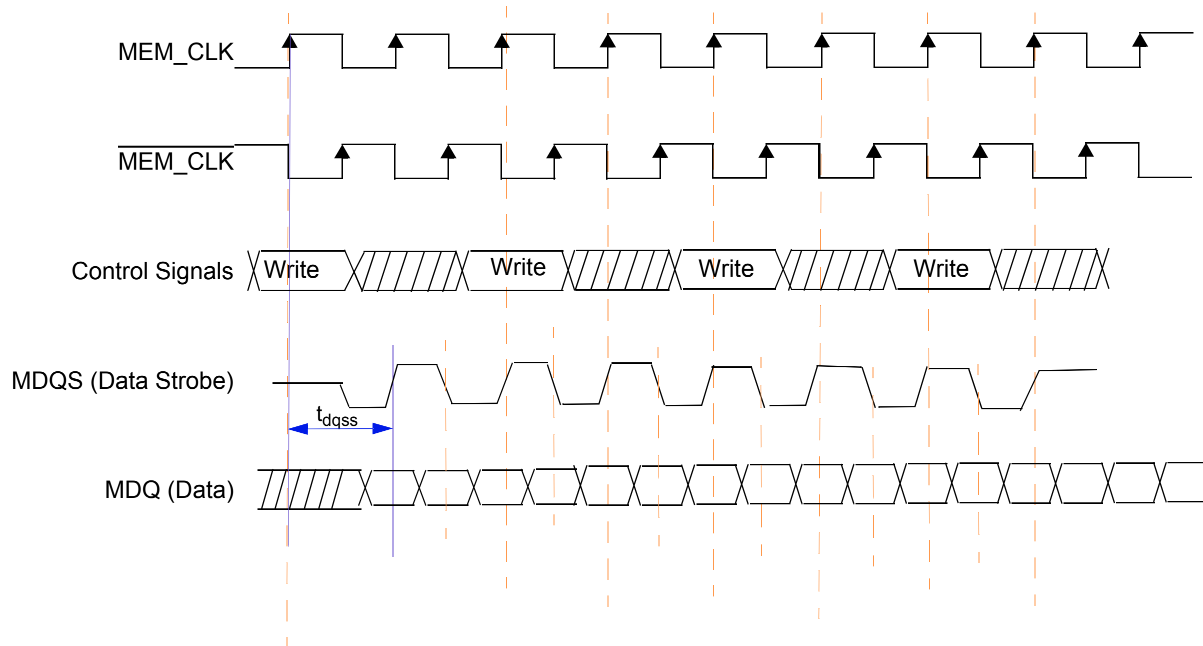
The equation below shows how to calculate the upper and lower limit. The right Tap delay number is selected, when the possible max and min sample timing is within the memory data valid window.

- $t_{data_sample_max}$ = max((1.55 + TapNum * 0.095), (1.74 + TapNum * 0.045))
- $t_{data_sample_min}$ = min((1.55 + TapNum * 0.095), (1.74 + TapNum * 0.045))

### 3.3.5.4 Memory Interface Timing-DDR SDRAM Write Command

**Table 21. DDR SDRAM Memory Write Timing**

| Sym | Description | Min | Max | Units | SpecID |
|---|---|---|---|---|---|
| $t_{mem_clk}$ | MEM_CLK period | 7.5 | — | ns | A5.20 |
| $t_{DQSS}$ | Delay from write command to first rising edge of MDQS | — | $t_{mem_clk}$+0.4 | ns | A5.21 |




NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM_WE}}$, $\overline{\text{MEM_CS}}$, $\overline{\text{MEM_CS1}}$ and CLK_EN

**Figure 9. DDR SDRAM Memory Write Timing**

## 3.3.6 PCI

The PCI interface on the MPC5200 is designed to PCI Version 2.2 and supports 33-MHz and 66-MHz PCI operations. See the PCI Local Bus Specification [4]; the component section specifies the electrical and timing parameters for PCI components with the intent that components connect directly together whether on the planar or an expansion board, without any external buffers or other “glue logic.” Parameters apply at the package pins, not at expansion board edge connectors.

The MPC5200 is always the source of the PCI CLK. The clock waveform must be delivered to each 33-MHz or 66-MHz PCI component in the system. Figure 10 shows the clock waveform and required measurement points for 3.3 V signaling environments. Table 22 summarizes the clock specifications.