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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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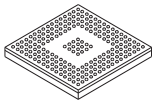
MPC5200B Data Sheet



TEPBGA–272
27 mm x 27 mm

Key features are shown below.

- MPC603e series e300 core
  - Superscalar architecture
  - 760 MIPS at 400 MHz (–40 °C to +85 °C)
  - 16 KB Instruction cache, 16 KB Data cache
  - Double precision FPU
  - Instruction and Data MMU
  - Standard and Critical interrupt capability
- SDRAM / DDR Memory Interface
  - Up to 133 MHz operation
  - SDRAM and DDR SDRAM support
  - 256 MB addressing range per CS, two CS available
  - 32-bit data bus
  - Built-in initialization and refresh
- Flexible multi-function External Bus Interface
  - Supports interfacing to ROM/Flash/SRAM memories or other memory mapped devices
  - 8 programmable Chip Selects
  - Non-multiplexed data access using 8-/16-/32-bit databus with up to 26-bit address
  - Short or Long Burst capable
  - Multiplexed data access using 8-/16-/32-bit databus with up to 25-bit address
- Peripheral Component Interconnect (PCI) Controller
  - Version 2.2 PCI compatibility
  - PCI initiator and target operation
  - 32-bit PCI Address/Data bus
  - 33 and 66 MHz operation
  - PCI arbitration function
- ATA Controller
  - Version 4 ATA compatible external interface—IDE Disk Drive connectivity
- BestComm DMA subsystem
  - Intelligent virtual DMA Controller
  - Dedicated DMA channels to control peripheral reception and transmission
  - Local memory (SRAM 16 KB)
- 6 Programmable Serial Controllers (PSC)
  - UART or RS232 interface
  - CODEC interface for Soft Modem, Master/Slave CODEC Mode, I^2S and AC97
  - Full duplex SPI mode
  - IrDA mode from 2400 bps to 4 Mbps
- Fast Ethernet Controller (FEC)
  - Supports 100Mbps IEEE 802.3 MII, 10 Mbps IEEE 802.3 MII, 10 Mbps 7-wire interface
- Universal Serial Bus Controller (USB)
  - USB Revision 1.1 Host
  - Open Host Controller Interface (OHCI)
  - Integrated USB Hub, with two ports.
- Two Inter-Integrated Circuit Interfaces (I^2C)
- Serial Peripheral Interface (SPI)
- Dual CAN 2.0 A/B Controller (MSCAN)
  - Implementation of version 2.0A/B CAN protocol
  - Standard and extended data frames
- J1850 Byte Data Link Controller (BDLC)
- J1850 Class B data communication network interface compatible and ISO compatible for low speed (<125 kbps) serial data communications in automotive applications.
- Supports 4X mode, 41.6 kbps
- In-frame response (IFR) types 0, 1, 2, and 3 supported
- Systems level features
  - Interrupt Controller supports four external interrupt request lines and 47 internal interrupt sources
  - GPIO/Timer functions
    Up to 56 total GPIO pins that support a variety of interrupt/WakeUp capabilities.
    Eight GPIO pins with timer capability supporting input capture, output compare, and pulse width modulation (PWM) functions
  - Real-time Clock with one-second resolution
  - Systems Protection (watch dog timer, bus monitor)
  - Individual control of functional block clock sources
  - Power management: Nap, Doze, Sleep, Deep Sleep modes
  - Support of WakeUp from low power modes by different sources (GPIO, RTC, CAN)
- Test/Debug features
  - JTAG (IEEE 1149.1 test access port)
  - Common On-chip Processor (COP) debug port
- On-board PLL and clock generation

Table of Contents

Figure 1 shows a simplified MPC5200B block diagram.

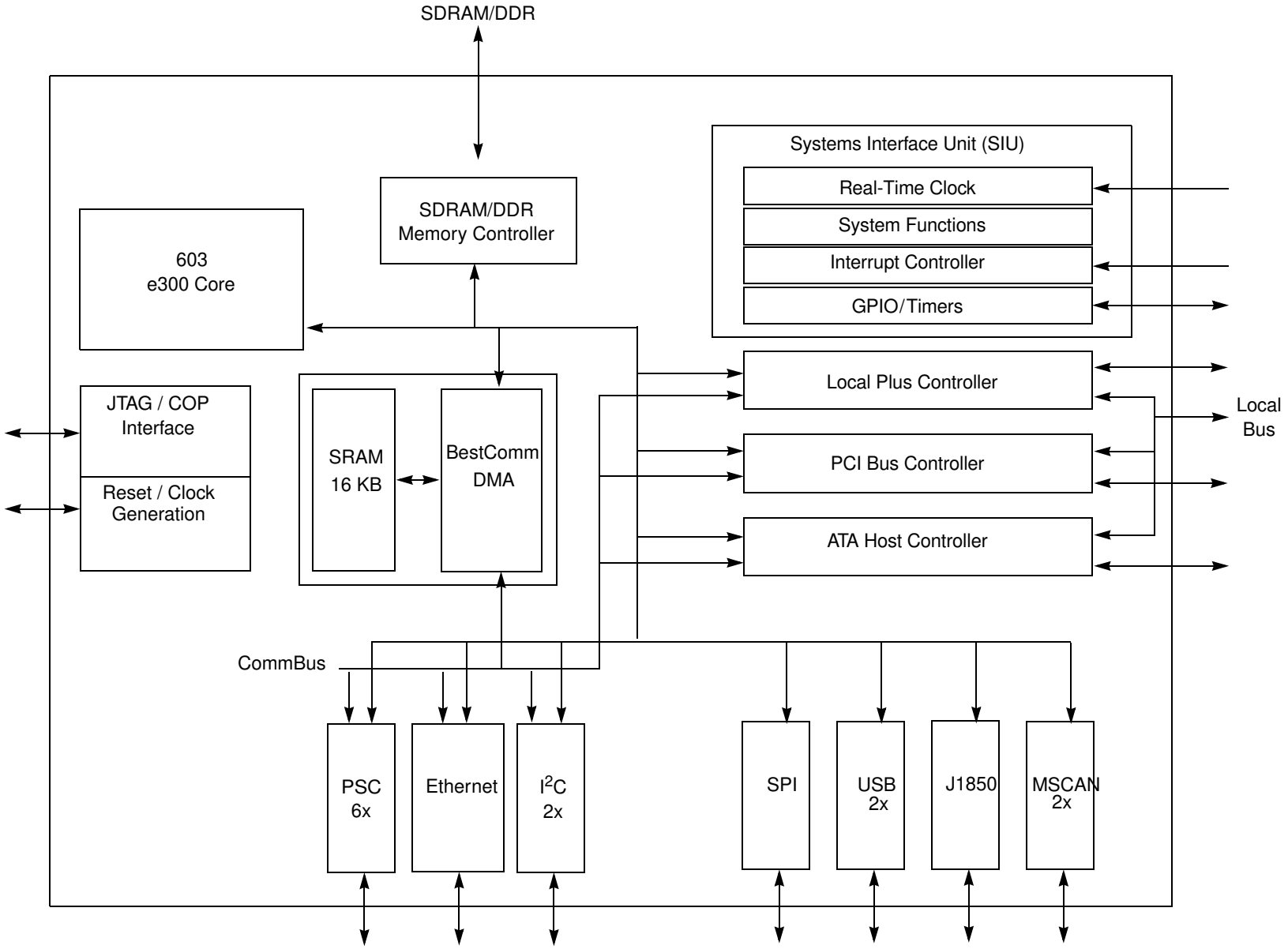


Figure 1. Simplified Block Diagram—MPC5200B

1 Electrical and Thermal Characteristics

1.1 DC Electrical Characteristics

1.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5200B DC Electrical characteristics. Table 1 gives the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Sym	Min	Max	Unit	SpecID
Supply voltage — e300 core and peripheral logic	VDD_CORE	–0.3	1.8	V	D1.1
Supply voltage — I/O buffers	VDD_IO, VDD_MEM_IO	–0.3	3.6	V	D1.2
Supply voltage — System APLL	SYS_PLL_AVDD	–0.3	2.1	V	D1.3
Supply voltage — e300 APLL	CORE_PLL_AVDD	–0.3	2.1	V	D1.4
Input voltage (VDD_IO)	Vin	–0.3	VDD_IO + 0.3	V	D1.5
Input voltage (VDD_MEM_IO)	Vin	–0.3	VDD_MEM_IO + 0.3	V	D1.6
Input voltage overshoot	Vinos	—	1.0	V	D1.7
Input voltage undershoot	Vinus	—	1.0	V	D1.8
Storage temperature range	Tstg	–55	150	°C	D1.9

1 Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

1.1.2 Recommended Operating Conditions

Table 2 gives the recommended operating conditions.

Table 2. Recommended Operating Conditions

Characteristic	Sym	Min[1]	Max[1]	Unit	SpecID
Supply voltage — e300 core and peripheral logic	VDD_CORE	1.42	1.58	V	D2.1
Supply voltage — standard I/O buffers	VDD_IO	3.0	3.6	V	D2.2
Supply voltage — memory I/O buffers (SDR)	$VDD\_MEM\_IO_{SDR}$	3.0	3.6	V	D2.3
Supply voltage — memory I/O buffers (DDR)	$VDD\_MEM\_IO_{DDR}$	2.42	2.63	V	D2.4
Supply voltage — System APLL	SYS_PLL_AVDD	1.42	1.58	V	D2.5
Supply voltage — e300 APLL	CORE_PLL_AVDD	1.42	1.58	V	D2.6

Table 2. Recommended Operating Conditions (continued)

Characteristic	Sym	Min[1]	Max[1]	Unit	SpecID
Input voltage — standard I/O buffers	Vin	0	VDD_IO	V	D2.7
Input voltage — memory I/O buffers (SDR)	Vin_{SDR}	0	$VDD\_MEM\_IO_{SDR}$	V	D2.8
Input voltage — memory I/O buffers (DDR)	Vin_{DDR}	0	$VDD\_MEM\_IO_{DDR}$	V	D2.9
Ambient operating temperature range[2]	T_A	–40	+85	°C	D2.10
Die junction operating temperature range	Tj	–40	+115	°C	D2.12

1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

2 Maximum e300 core operating frequency is 400 MHz.

1.1.3 DC Electrical Specifications

Table 3 gives the DC Electrical characteristics for the MPC5200B at recommended operating conditions (see Table 2).

Table 3. DC Electrical Specifications

Characteristic	Condition	Sym	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL $VDD\_IO/VDD\_MEM\_IO_{SDR}$	V_{IH}	2.0	—	V	D3.1
Input high voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IH}	1.7	—	V	D3.2
Input high voltage	Input type = PCI VDD_IO	V_{IH}	2.0	—	V	D3.3
Input high voltage	Input type = SCHMITT VDD_IO	V_{IH}	2.0	—	V	D3.4
Input high voltage	SYS_XTAL_IN	CV_{IH}	2.0	—	V	D3.5
Input high voltage	RTC_XTAL_IN	CV_{IH}	2.0	—	V	D3.6
Input low voltage	Input type = TTL $VDD\_IO/VDD\_MEM\_IO_{SDR}$	V_{IL}	—	0.8	V	D3.7
Input low voltage	Input type = TTL $VDD\_MEM\_IO_{DDR}$	V_{IL}	—	0.7	V	D3.8
Input low voltage	Input type = PCI VDD_IO	V_{IL}	—	0.8	V	D3.9
Input low voltage	Input type = SCHMITT VDD_IO	V_{IL}	—	0.8	V	D3.10
Input low voltage	SYS_XTAL_IN	CV_{IL}	—	0.8	V	D3.11
Input low voltage	RTC_XTAL_IN	CV_{IL}	—	0.8	V	D3.12
Input leakage current	Vin = 0 or $VDD\_IO/VDD\_IO\_MEM_{SDR}$ (depending on input type[1])	I_{IN}	—	±2	µA	D3.13
Input leakage current	SYS_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.14

Table 3. DC Electrical Specifications (continued)

Characteristic	Condition	Sym	Min	Max	Unit	SpecID
Input leakage current	RTC_XTAL_IN Vin = 0 or VDD_IO	I_{IN}	—	±10	µA	D3.15
Input current, pullup resistor	PULLUP VDD_IO Vin = 0	I_{INpu}	40	109	µA	D3.16
Input current, pullup resistor — memory I/O buffers	PULLUP_MEM $VDD\_IO\_MEM_{SDR}$ Vin = 0	I_{INpu}	41	111	µA	D3.17
Input current, pulldown resistor	PULLDOWN VDD_IO Vin = VDD_IO	I_{INpd}	36	106	µA	D3.18
Output high voltage	IOH is driver dependent(2) $VDD\_IO, VDD\_IO\_MEM_{SDR}$	V_{OH}	2.4	—	V	D3.19
Output high voltage	IOH is driver dependent(2) $VDD\_IO\_MEM_{DDR}$	V_{OHDDR}	1.7	—	V	D3.20
Output low voltage	IOL is driver dependent(2) $VDD\_IO, VDD\_IO\_MEM_{SDR}$	V_{OL}	—	0.4	V	D3.21
Output low voltage	IOL is driver dependent(2) $VDD\_IO\_MEM_{DDR}$	V_{OLDDR}	—	0.4	V	D3.22
DC Injection Current Per Pin(3)		I_{CS}	–1.0	1.0	mA	D3.23
Capacitance	Vin = 0 V, f = 1 MHz	C_{in}	—	15	pF	D3.24

1 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.

2 See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 52.

3 All injection current is transferred to VDD_IO/VDD_IO_MEM. An external load is required to dissipate this current to maintain the power supply within the specified voltage range. Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 4. Drive Capability of MPC5200B Output Pins

Driver Type	Supply Voltage	I_{OH}	I_{OL}	Unit	SpecID
DRV4	VDD_IO = 3.3 V	4	4	mA	D3.25
DRV8	VDD_IO = 3.3 V	8	8	mA	D3.26
DRV8_OD	VDD_IO = 3.3 V	—	8	mA	D3.27
DRV16_MEM	VDD_IO_MEM = 3.3 V	16	16	mA	D3.28
DRV16_MEM	VDD_IO_MEM = 2.5 V	16	16	mA	D3.29
PCI	VDD_IO = 3.3 V	16	16	mA	D3.30

1.1.4 Electrostatic Discharge

CAUTION

This device contains circuitry that protects against damage due to high-static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (GND or V_{CC}). Table 7 gives package thermal characteristics for this device.

Table 5. ESD and Latch-Up Protection Characteristics

Sym	Rating	Min	Max	Unit	SpecID
V_{HBM}	Human Body Model (HBM)—JEDEC JESD22-A114-B	2000	—	V	D4.1
V_{MM}	Machine Model (MM)—JEDEC JESD22-A115	200	—	V	D4.2
V_{CDM}	Charge Device Model (CDM)—JEDEC JESD22-C101	500	—	V	D4.3
I_{LAT}	Latch-up Current at T_A=85 °C positive negative	 +100 –100	—	mA	D4.4
I_{LAT}	Latch-up Current at T_A=27 °C positive negative	 +200 –200	—	mA	D4.5

1.1.5 Power Dissipation

Power dissipation of the MPC5200B is caused by 3 different components: the dissipation of the internal or core digital logic (supplied by VDD_CORE), the dissipation of the analog circuitry (supplied by SYS_PLL_AVDD and CORE_PLL_AVDD) and the dissipation of the IO logic (supplied by VDD_IO_MEM and VDD_IO). Table 6 details typical measured core and analog power dissipation figures for a range of operating modes. However, the dissipation due to the switching of the IO pins can not be given in general, but must be calculated by the user for each application case using the following formula:

$$P_{IO} = P_{IOint} + \sum_{M} N \times C \times VDD\_IO^2 \times f \qquad \textbf{Eqn. 1}$$

where N is the number of output pins switching in a group M, C is the capacitance per pin, VDD_IO is the IO voltage swing, f is the switching frequency and PIOint is the power consumed by the unloaded IO stage. The total power consumption of the MPC5200B processor must not exceed the value, which would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{analog} + P_{IO} \qquad \textbf{Eqn. 2}$$

Table 6. Power Dissipation

Core Power Supply (VDD_CORE)					
Mode	SYS_XTAL/XLB/PCI/IPB/CORE (MHz)		Unit	Notes	SpecID
	33/66/33/33/264	33/132/66/132/396			
	Typ	Typ			
Operational	727.5	1080	mW	(1),(2)	D5.1
Doze	—	600	mW	(1),(3)	D5.2
Nap	—	225	mW	(1),(4)	D5.3
Sleep	—	225	mW	(1),(5)	D5.4
Deep-Sleep	52.5	52.5	mW	(1),(6)	D5.5
PLL Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD)					
Mode	**Typ**		**Unit**	**Notes**	
Typical	2		mW	(7)	D5.6
Unloaded I/O Power Supplies (VDD_IO, VDD_MEM_IO[8])					
Mode	**Typ**		**Unit**	**Notes**	
Typical	33		mW	(9)	D5.7

1 Typical core power is measured at VDD_CORE = 1.5 V, Tj = 25 °C

2 Operational power is measured while running an entirely cache-resident program with floating-point multiplication instructions in parallel with a continuous PCI transaction via BestComm.

3 Doze power is measured with the e300 core in Doze mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

4 Nap power is measured with the e300 core in Nap mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

5 Sleep power is measured with the e300 core in Sleep mode, the system oscillator, System PLL and Core PLL are active, all other system modules are inactive

6 Deep-Sleep power is measured with the e300 core in Sleep mode, the system oscillator, System PLL, Core PLL and all other system modules are inactive

7 Typical PLL power is measured at SYS_PLL_AVDD = CORE_PLL_AVDD = 1.5 V, Tj = 25 °C

8 IO power figures given in the table represent the worst case scenario. For the VDD_MEM_IO rail connected to 2.5 V the IO power is expected to be lower and bounded by the worst case with VDD_MEM_IO connected to 3.3 V.

9 Unloaded typical I/O power is measured in Deep-Sleep mode at VDD_IO = $VDD\_MEM\_IO_{SDR}$= 3.3 V, Tj = 25 °C

1.1.6 Thermal Characteristics

Table 7. Thermal Resistance Data

Rating	Board Layers	Sym	Value	Unit	Notes	SpecID
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	30	°C/W	(1),(2)	D6.1
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JMA}$	22	°C/W	(1),(3)	D6.2
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	24	°C/W	(1),(3)	D6.3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	19	°C/W	(1),(3)	D6.4
Junction to Board	—	$R_{\theta JB}$	14	°C/W	(4)	D6.5
Junction to Case	—	$R_{\theta JC}$	8	°C/W	(5)	D6.6
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	(6)	D6.7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

1.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \text{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

1.2 Oscillator and PLL Electrical Characteristics

The MPC5200B System requires a system-level clock input SYS_XTAL. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent Real-Time Clock (RTC) system.

The MPC5200B clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The e300 core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The e300 core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

1.2.1 System Oscillator Electrical Characteristics

Table 8. System Oscillator Electrical Characteristics

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}		15.6	33.3	35.0	MHz	O1.1
Oscillator start-up time	t_{up_osc}		—	—	10	ms	O1.2

1.2.2 RTC Oscillator Electrical Characteristics

Table 9. RTC Oscillator Electrical Characteristics

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
RTC_XTAL frequency	f_{rtc_xtal}		—	32.768	—	kHz	O2.1

1.2.3 System PLL Electrical Characteristics

Table 10. System PLL Specifications

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}	(1)	15.6	33.3	35.0	MHz	O3.1
SYS_XTAL cycle time	t_{sys_xtal}	(1)	66.6	30.0	28.5	ns	O3.2
SYS_XTAL clock input jitter	t_{jitter}	(2)	—	—	150	ps	O3.3
System VCO frequency	f_{VCOsys}	(1)	250	533	800	MHz	O3.4
System PLL relock time	t_{lock}	(3)	—	—	100	µs	O3.5

1 The SYS_XTAL frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.

2 This represents total input jitter—short term and long term combined—and is guaranteed by design. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.

3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLKare reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

1.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 11. e300 PLL Specifications

Characteristic	Sym	Notes	Min	Typical	Max	Unit	SpecID
e300 frequency	f_{core}	(1)	50	—	550	MHz	O4.1
e300 cycle time	t_{core}	(1)	2.85	—	40.0	ns	O4.2
e300 VCO frequency	$f_{VCOcore}$	(1)	400	—	1200	MHz	O4.3
e300 input clock frequency	f_{XLB_CLK}	—	25	—	367	MHz	O4.4
e300 input clock cycle time	t_{XLB_CLK}	—	2.73	—	50.0	ns	O4.5
e300 input clock jitter	t_{jitter}	(2)	—	—	150	ps	O4.6
e300 PLL relock time	t_{lock}	(3)	—	—	100	µs	O4.7

1 The XLB_CLK frequency and e300 PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and e300 PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies in Table 12.

2 This represents total input jitter—short term and long term combined—and is guaranteed by design. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.

3 Relock time is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

1.3 AC Electrical Characteristics

Hyperlinks to the indicated timing specification sections are provided below.

- AC Operating Frequency Data
- Clock AC Specifications
- Resets
- External Interrupts
- SDRAM
- PCI
- Local Plus Bus
- ATA
- Ethernet
- USB
- SPI
- MSCAN
- I^2C
- J1850
- PSC
- GPIOs and Timers
- IEEE 1149.1 (JTAG) AC Specifications

1.3.1 AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

- TA = –40 to 85 °C
- Tj = –40 to 115 °C
- VDD_CORE = 1.42 to 1.58 V
  VDD_IO = 3.0 to 3.6 V

- Input conditions:
  All Inputs: tr, tf <= 1 ns
- Output Loading:
  All Outputs: 50 pF

1.3.2 AC Operating Frequency Data

Table 12 provides the operating frequency information for the MPC5200B.

Table 12. Clock Frequencies

		Min	Max	Units	SpecID
1	e300 Processor Core	—	400	MHz	A1.1
2	SDRAM Clock	—	133	MHz	A1.2
3	XL Bus Clock	—	133	MHz	A1.3
4	IP Bus Clock	—	133	MHz	A1.4
5	PCI / Local Plus Bus Clock	—	66	MHz	A1.5
6	PLL Input Range	15.6	35	MHz	A1.6

1.3.3 Clock AC Specifications

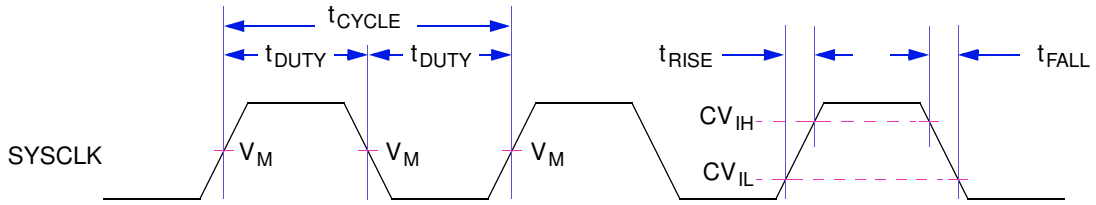


Figure 2. Timing Diagram—SYS_XTAL_IN

Table 13. SYS_XTAL_IN Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTAL_IN cycle time.[1]	28.6	64.1	ns	A2.1
t_{RISE}	SYS_XTAL_IN rise time.	—	5.0	ns	A2.2
t_{FALL}	SYS_XTAL_IN fall time.	—	5.0	ns	A2.3
t_{DUTY}	SYS_XTAL_IN duty cycle (measured at V_M).[2]	40.0	60.0	%	A2.4
CV_{IH}	SYS_XTAL_IN input voltage high	2.0	—	V	A2.5
CV_{IL}	SYS_XTAL_IN input voltage low	—	0.8	V	A2.6

1 **CAUTION**—The SYS_XTAL_IN frequency and system PLL_CFG[0–6] settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the *MPC5200B User's Manual (MPC5200BUM)*.

2 SYS_XTAL_IN duty cycle is measured at V_M.

1.3.4 Resets

The MPC5200B has three reset pins:

- $\overline{\text{PORRESET}}$—Power on Reset
- $\overline{\text{HRESET}}$—Hard Reset
- $\overline{\text{SRESET}}$—Software Reset

These signals are asynchronous I/O signals and can be asserted at any time. The input side uses a Schmitt trigger and requires the same input characteristics as other MPC5200B inputs, as specified in the DC Electrical Specifications section. Table 14 specifies the pulse widths of the Reset inputs.

Table 14. Reset Pulse Width

Name	Description	Min Pulse Width	Max Pulse Width	Reference Clock	SpecID
$\overline{\text{PORRESET}}$	Power On Reset	$t_{VDD\_stable} + t_{up\_osc} + t_{lock}$	—	SYS_XTAL_IN	A3.1
$\overline{\text{HRESET}}$	Hardware Reset	4 clock cycles	—	SYS_XTAL_IN	A3.2
$\overline{\text{SRESET}}$	Software Reset	4 clock cycles	—	SYS_XTAL_IN	A3.3

For $\overline{\text{PORRESET}}$ the value of the minimum pulse width reflects the power on sequence. If $\overline{\text{PORRESET}}$ is asserted afterwards its minimum pulse width equals the minimum given for $\overline{\text{HRESET}}$ related to the same reference clock.

The t_{VDD_stable} describes the time which is needed to get all power supplies stable.

For t_{lock}, refer to the Oscillator/PLL section of this specification for further details.

For t_{up_osc}, refer to the Oscillator/PLL section of this specification for further details.

Following the deassertion of $\overline{\text{PORRESET}}$, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ remain low for 4096 reference clock cycles.

The deassertion of $\overline{\text{HRESET}}$ for at least the minimum pulse width forces the internal resets to be active for an additional 4096 clock cycles.

NOTE

As long as VDD is not stable the $\overline{\text{HRESET}}$ output is not stable.

Table 15. Reset Rise/Fall Timing

Description	Min	Max	Unit	SpecID
$\overline{\text{PORRESET}}$ fall time	—	1	ms	A3.4
$\overline{\text{PORRESET}}$ rise time	—	1	ms	A3.5
$\overline{\text{HRESET}}$ fall time	—	1	ms	A3.6
$\overline{\text{HRESET}}$ rise time	—	1	ms	A3.7
$\overline{\text{SRESET}}$ fall time	—	1	ms	A3.8
$\overline{\text{SRESET}}$ rise time	—	1	ms	A3.9

NOTE

Make sure that the $\overline{\text{PORRESET}}$ does not carry any glitches. The MPC5200B has no filter to prevent them from getting into the chip. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ must have a monotonous rise time. The assertion of $\overline{\text{HRESET}}$ becomes active at Power on Reset without any SYS_XTAL clock.

For additional information, see the *MPC5200B User's Manual (MPC5200BUM).*

1.3.4.1 Reset Configuration Word

During reset ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) the Reset Configuration Word is latched in the related Reset Configuration Word Register with each rising edge of the SYS_XTAL signal. If both resets ($\overline{\text{HRESET}}$ and $\overline{\text{PORRESET}}$) are inactive (high), the contents of this register are locked immediately with the SYS_XTAL clock (see Figure 3).

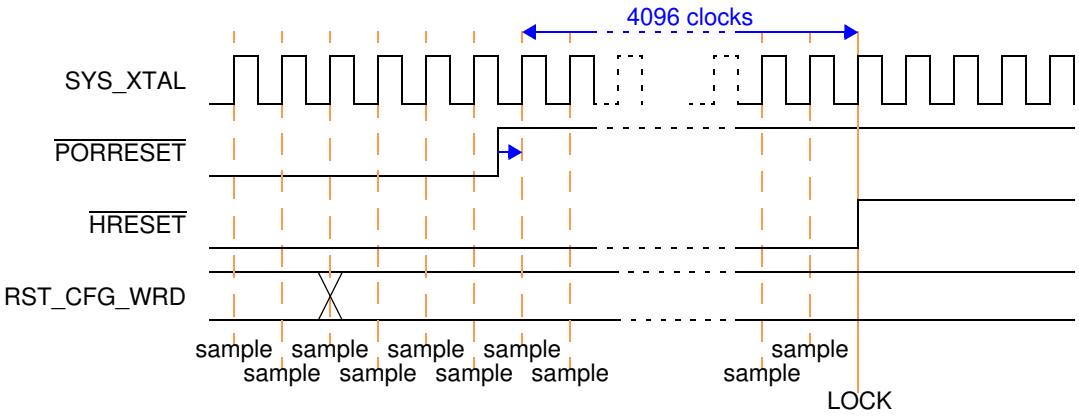


Figure 3. Reset Configuration Word Locking

NOTE

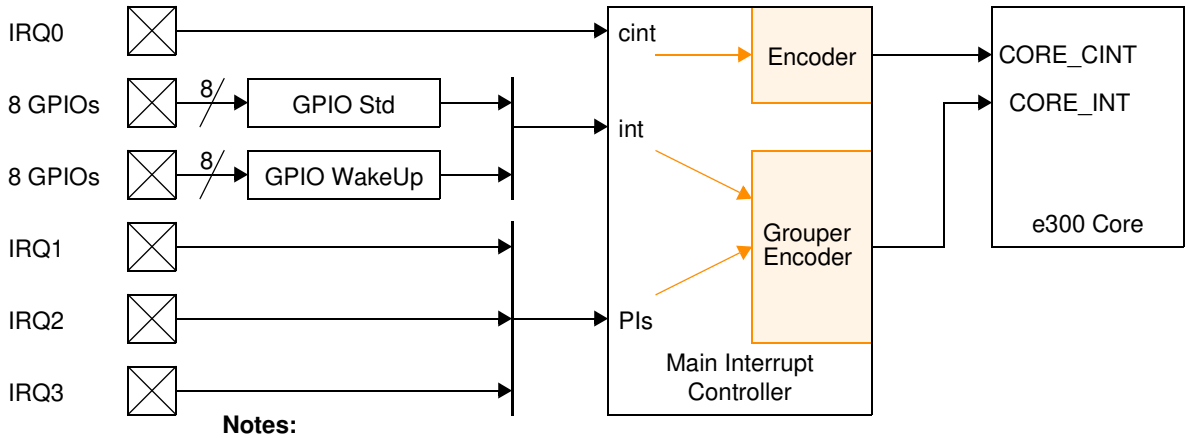
Beware of changing the values on the pins of the reset configuration word after the deassertion of $\overline{\text{PORRESET}}$. This may cause problems because it may change the internal clock ratios and so extend the PLL locking process.

1.3.5 External Interrupts

The MPC5200B provides three different kinds of external interrupts:

- Four IRQ interrupts
- Eight GPIO interrupts with simple interrupt capability (not available in power-down mode)
- Eight WakeUp interrupts (special GPIO pins)

The propagation of these three kinds of interrupts to the core is shown in the following graphic:



Notes:
1. PIs = Programmable Inputs
2. Grouper and Encoder functions imply programmability in software

Figure 4. External Interrupt Scheme

Due to synchronization, prioritization, and mapping of external interrupt sources, the propagation of external interrupts to the core processor is delayed by several IP_CLK clock cycles. The following table specifies the interrupt latencies in IP_CLK cycles. The IP_CLK frequency is programmable in the Clock Distribution Module (see Table 16).

Table 16. External Interrupt Latencies

Interrupt Type	Pin Name	Clock Cycles	Reference Clock	Core Interrupt	SpecID
Interrupt Requests	IRQ0	10	IP_CLK	critical (cint)	A4.1
	IRQ0	10	IP_CLK	normal (int)	A4.2
	IRQ1	10	IP_CLK	normal (int)	A4.3
	IRQ2	10	IP_CLK	normal (int)	A4.4
	IRQ3	10	IP_CLK	normal (int)	A4.5
Standard GPIO Interrupts	GPIO_PSC3_4	12	IP_CLK	normal (int)	A4.6
	GPIO_PSC3_5	12	IP_CLK	normal (int)	A4.7
	GPIO_PSC3_8	12	IP_CLK	normal (int)	A4.8
	GPIO_USB_9	12	IP_CLK	normal (int)	A4.9
	GPIO_ETHI_4	12	IP_CLK	normal (int)	A4.10
	GPIO_ETHI_5	12	IP_CLK	normal (int)	A4.11
	GPIO_ETHI_6	12	IP_CLK	normal (int)	A4.12
	GPIO_ETHI_7	12	IP_CLK	normal (int)	A4.13
GPIO WakeUp Interrupts	GPIO_PSC1_4	12	IP_CLK	normal (int)	A4.15
	GPIO_PSC2_4	12	IP_CLK	normal (int)	A4.16
	GPIO_PSC3_9	12	IP_CLK	normal (int)	A4.17
	GPIO_ETHI_8	12	IP_CLK	normal (int)	A4.18
	GPIO_IRDA_0	12	IP_CLK	normal (int)	A4.19
	DGP_IN0	12	IP_CLK	normal (int)	A4.20
	DGP_IN1	12	IP_CLK	normal (int)	A4.21

NOTES:
1) The frequency of IP_CLK depends on register settings in Clock Distribution Module. See the *MPC5200B User's Manual*.

2) The interrupt latency descriptions in the table above are related to non competitive, non masked but enabled external interrupt sources. Take care of interrupt prioritization which may increase the latencies.

Because all external interrupt signals are synchronized into the internal processor bus clock domain, each of these signals has to exceed a minimum pulse width of more than one IP_CLK cycle.

Table 17. Minimum Pulse Width for External Interrupts to be Recognized

Name	Min Pulse Width	Max Pulse Width	Reference Clock	SpecID
All external interrupts (IRQs, GPIOs)	> 1 clock cycle	—	IP_CLK	A4.22

NOTES:

1) The frequency of the IP_CLK depends on the register settings in Clock Distribution Module. See the *MPC5200B User's Manual (MPC5200BUM)* for further information.

2) If the same interrupt occurs a second time while its interrupt service routine has not cleared the former one, the second interrupt is not recognized at all.

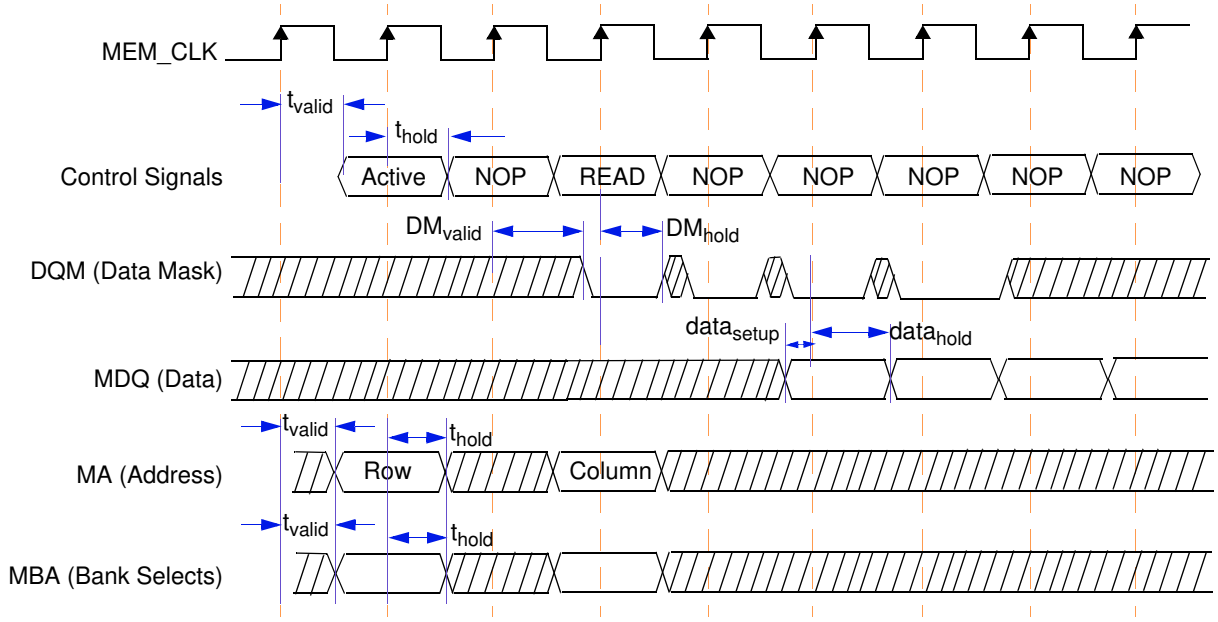
Besides synchronization, prioritization, and mapping the latency of an external interrupt to the start of its associated interrupt service routine also depends on the following conditions: To get a minimum interrupt service response time, it is recommended to enable the instruction cache and set up the maximum core clock, XL bus, and IP bus frequencies (depending on board design and programming). In addition, it is advisable to execute an interrupt handler, which has been implemented in assembly code.

1.3.6 SDRAM

1.3.6.1 Memory Interface Timing-Standard SDRAM Read Command

Table 18. Standard SDRAM Memory Read Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.1
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.5 + 0.4$	ns	A5.2
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.5$	—	ns	A5.3
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.25 + 0.4$	ns	A5.4
DM_{hold}	DQM hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.25 - 0.7$	—	ns	A5.5
$data_{setup}$	MDQ setup to rising edge of MEM_CLK	—	0.3	ns	A5.6
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	0.2	—	ns	A5.7



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

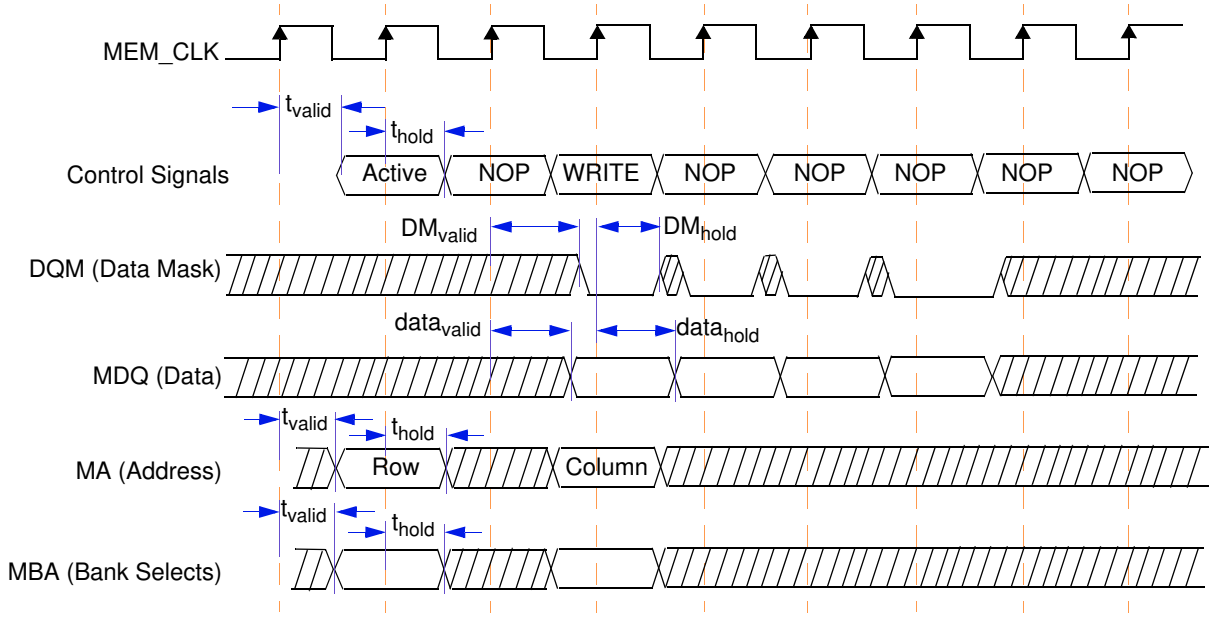
Figure 5. Timing Diagram—Standard SDRAM Memory Read Timing

1.3.6.2 Memory Interface Timing-Standard SDRAM Write Command

In Standard SDRAM, all signals are activated on the MEM_CLK from the Memory Controller and captured on the MEM_CLK clock at the memory device.

Table 19. Standard SDRAM Write Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.8
t_{valid}	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.5 + 0.4$	ns	A5.9
t_{hold}	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.5$	—	ns	A5.10
DM_{valid}	DQM valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.25 + 0.4$	ns	A5.11
DM_{hold}	DQM hold after rising edge of Mem_clk	$t_{mem\_clk} \times 0.25 - 0.7$	—	ns	A5.12
$data_{valid}$	MDQ valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.75 + 0.4$	ns	A5.13
$data_{hold}$	MDQ hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.75 - 0.7$	—	ns	A5.14



NOTE: Control Signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

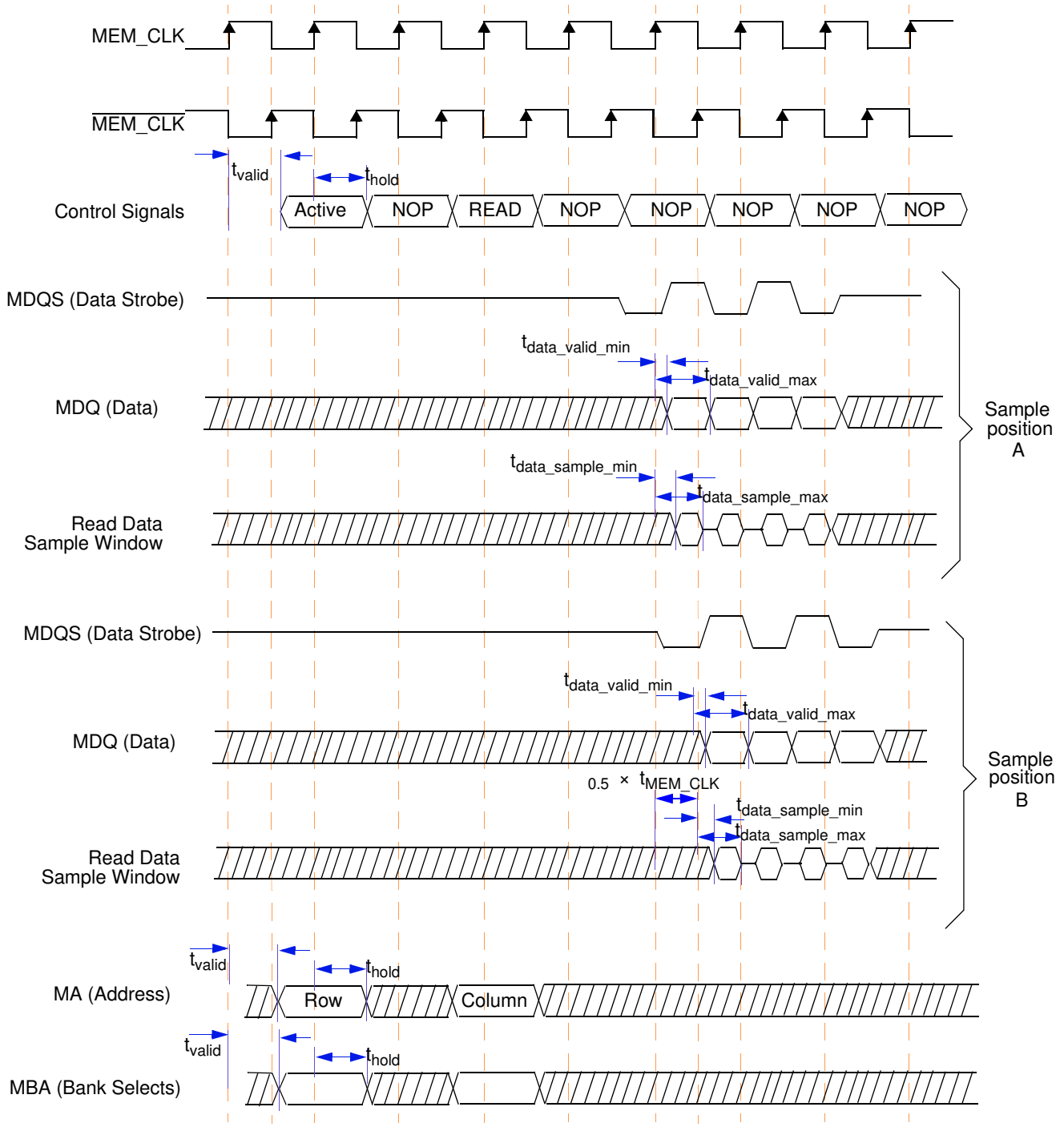
Figure 6. Timing Diagram—Standard SDRAM Memory Write Timing

1.3.6.3 Memory Interface Timing-DDR SDRAM Read Command

The SDRAM Memory Controller uses a 1/4 period delayed MDQS strobe to capture the MDQ data. The 1/4 period delay value is calculated automatically by hardware.

Table 20. DDR SDRAM Memory Read Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.15
t_{valid}	Control Signals, Address and MBA valid after rising edge of MEM_CLK	—	$t_{mem\_clk} \times 0.5 + 0.4$	ns	A5.16
t_{hold}	Control Signals, Address and MBA hold after rising edge of MEM_CLK	$t_{mem\_clk} \times 0.5$	—	ns	A5.17
$data_{setup}$	Setup time relative to MDQS	—	0.4	ns	A5.18
$data_{hold}$	Hold time relative to MDQS	2.6	—	ns	A5.19



Sample position A: data are sampled on the expected edge of MEM_CLK, the MDQS signal indicate the valid data
Sample position B: data are sampled on a later edge of MEM_CLK, SDRAM controller is waiting for the valid MDQS signal

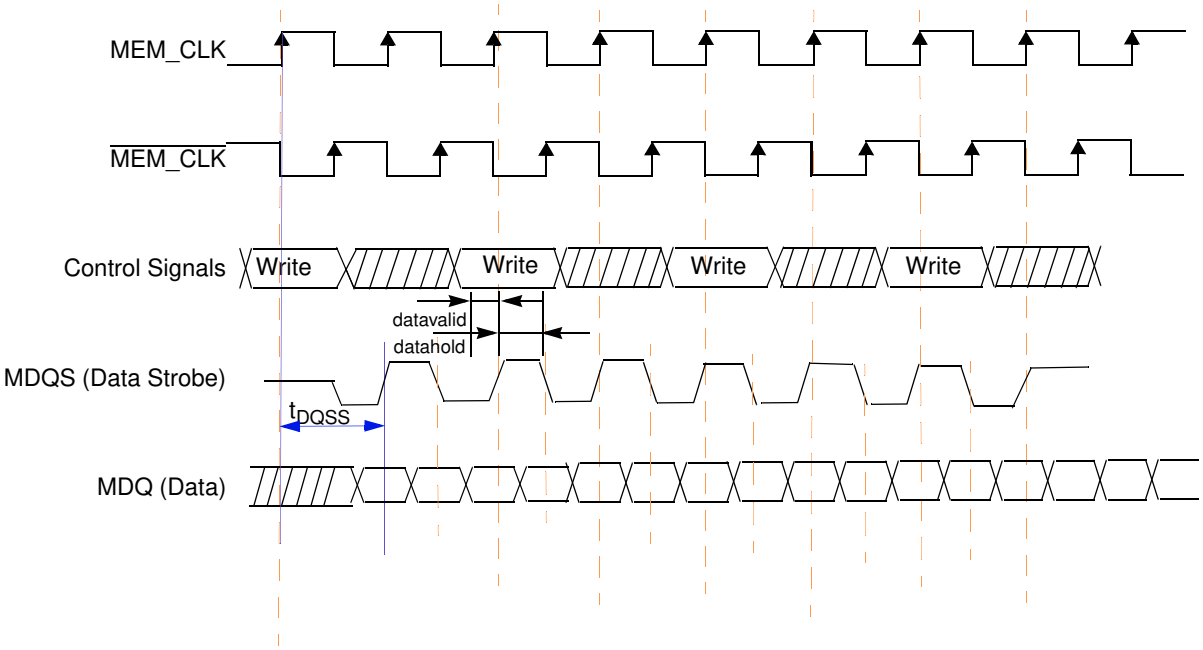
NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$ and CLK_EN

Figure 7. Timing Diagram—DDR SDRAM Memory Read Timing

1.3.6.4 Memory Interface Timing-DDR SDRAM Write Command

Table 21. DDR SDRAM Memory Write Timing

Sym	Description	Min	Max	Units	SpecID
t_{mem_clk}	MEM_CLK period	7.5	—	ns	A5.20
t_{DQSS}	Delay from write command to first rising edge of MDQS	—	t_{mem_clk} + 0.4	ns	A5.21
$data_{valid}$	MDQ valid before rising edge of MDQS	1.0	—	ns	A5.22
$data_{hold}$	MDQ valid after rising edge of MDQS	1.0	—	ns	A5.23



NOTE: Control Signals signals are composed of RAS, CAS, $\overline{\text{MEM\_WE}}$, $\overline{\text{MEM\_CS}}$, $\overline{\text{MEM\_CS1}}$, and CLK_EN

Figure 8. DDR SDRAM Memory Write Timing

1.3.7 PCI

The PCI interface on the MPC5200B is designed to PCI Version 2.2 and supports 33 MHz and 66 MHz PCI operations. See the PCI Local Bus Specification; the component section specifies the electrical and timing parameters for PCI components with the intent that components connect directly together whether on the planar or an expansion board, without any external buffers or other “glue logic.” Parameters apply at the package pins, not at expansion board edge connectors.

The MPC5200B is always the source of the PCI CLK. The clock waveform must be delivered to each 33 MHz or 66 MHz PCI component in the system. Figure 9 shows the clock waveform and required measurement points for 3.3 V signaling environments. Table 22 summarizes the clock specifications.

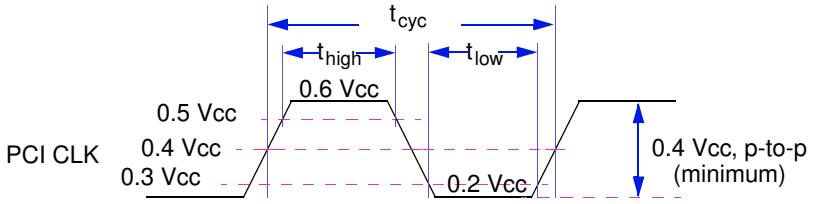


Figure 9. PCI CLK Waveform

Table 22. PCI CLK Specifications

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
t_{cyc}	PCI CLK Cycle Time	15	30	30	—	ns	(1),(3)	A6.1
t_{high}	PCI CLK High Time	6	—	11	—	ns	—	A6.2
t_{low}	PCI CLK Low Time	6	—	11	—	ns	—	A6.3
—	PCI CLK Slew Rate	1.5	4	1	4	V/ns	(2)	A6.4
—	PCI Clock Jitter (peak to peak)	—	200	—	200	ps	—	—

NOTES:
1. In general, all 66 MHz PCI components must work with any clock frequency up to 66 MHz. CLK requirements vary depending upon whether the clock frequency is above 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 9.
3. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

Table 23. PCI Timing Parameters

Sym	Description	66 MHz		33 MHz		Units	Notes	SpecID
		Min	Max	Min	Max			
t_{val}	CLK to Signal Valid Delay — bused signals	2	6	2	11	ns	(1),(2),(3)	A6.5
t_{val}(ptp)	CLK to Signal Valid Delay — point to point	2	6	2	12	ns	(1),(2),(3)	A6.6
t_{on}	Float to Active Delay	2	—	2	—	ns	(1)	A6.7
t_{off}	Active to Float Delay		14		28	ns	(1)	A6.8
t_{su}	Input Setup Time to CLK — bused signals	3	—	7	—	ns	(3),(4)	A6.9
t_{su}(ptp)	Input Setup Time to CLK — point to point	5	—	10,12	—	ns	(3),(4)	A6.10
t_h	Input Hold Time from CLK	0	—	0	—	ns	(4)	A6.11

NOTES:
1. See the timing measurement conditions in the PCI Local Bus Specification. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.

2. Minimum times are measured at the package pin with the load circuit, and maximum times are measured with the load circuit as shown in the PCI Local Bus Specification.
3. REQ# and GNT# are point-to-point signals and have different input setup times than do bused signals. GNT# and REQ# have a setup of 5 ns at 66 MHz. All other signals are bused.
4. See the timing measurement conditions in the PCI Local Bus Specification.

For Measurement and Test Conditions, see the PCI Local Bus Specification.

1.3.8 Local Plus Bus

The Local Plus Bus is the external bus interface of the MPC5200B. A maximum of eight configurable chip selects (CS) are provided. There are two main modes of operation: non-MUXed (Legacy and Burst) and MUXED. The reference clock is the PCI CLK. The maximum bus frequency is 66 MHz.

Definition of Acronyms and Terms:

- WS = Wait State
- DC = Dead Cycle
- LB = Long Burst
- DS = Data Size in Bytes
- t_{PCIck} = PCI clock period
- t_{IPBIck} = IPBI clock period

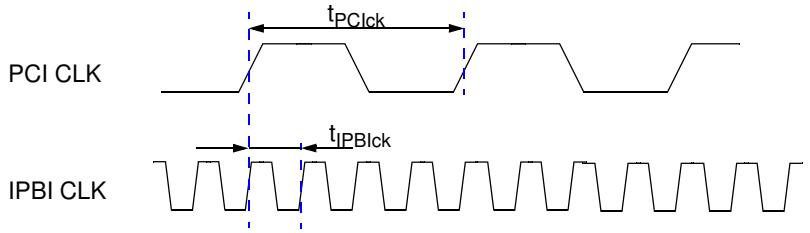


Figure 10. Timing Diagram—IPBI and PCI clock (example ratio: 4:1)

1.3.8.1 Non-MUXed Mode

Table 24. Non-MUXed Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	4.6	10.6	ns	—	A7.1
t_{CSN}	PCI CLK to CS negation	2.9	7.0	ns	—	A7.2
t_1	CS pulse width	(2 + WS) × t_{PCIck}	(2 + WS) × t_{PCIck}	ns	(1)	A7.3
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns	—	A7.4
t_3	ADDR hold after CS negation	t_{IPBIck}	—	ns	(2)	A7.5
t_4	OE assertion before CS assertion	—	4.8	ns	—	A7.6
t_5	OE negation before CS negation	—	2.7	ns	—	A7.7
t_6	RW valid before CS assertion	t_{PCIck}	—	ns	—	A7.8
t_7	RW hold after CS negation	t_{IPBIck}	—	ns	—	A7.9
t_8	DATA output valid before CS assertion	t_{IPBIck}	—	ns	—	A7.10
t_9	DATA output hold after CS negation	t_{IPBIck}	—	ns	—	A7.11

Table 24. Non-MUXed Mode Timing (continued)

Sym	Description	Min	Max	Units	Notes	SpecID
t_{10}	DATA input setup before CS negation	8.5	—	ns	—	A7.12
t_{11}	DATA input hold after CS negation	0	(DC + 1) × t_{PCIck}	ns	(6)	A7.13
t_{12}	ACK assertion after CS assertion	t_{PCIck}	—	ns	(3)	A7.14
t_{13}	ACK negation after CS negation	—	t_{PCIck}	ns	(3)	A7.15
t_{14}	TS assertion before CS assertion	—	6.9	ns	(4)	A7.16
t_{15}	TS pulse width	t_{PCIck}	t_{PCIck}	ns	(4)	A7.17
t_{16}	TSIZ valid before CS assertion	t_{IPBIck}	—	ns	(5)	A7.18
t_{17}	TSIZ hold after CS negation	t_{IPBIck}	—	ns	(5)	A7.19
t_{18}	ACK change before PCI clock	—	2.0	ns	(1)	A7.20
t_{19}	ACK change after PCI clock	—	4.4	ns	(1)	A7.21

NOTES:

1. ACK can shorten the CS pulse width.
   Wait States (WS) can be programmed in the Chip Select X Register, Bit field WaitP and WaitX. It can be specified from 0–65535.
2. In Large Flash and MOST Graphics mode the shared PCI/ATA pins, used as address lines, are released at the same moment as the CS. This can cause the address to change before CS is deasserted.
3. ACK is input and can be used to shorten the CS pulse width.
4. Only available in Large Flash and MOST Graphics mode.
5. Only available in MOST Graphics mode.
6. Deadcycles are only used, if no arbitration to an other module (ATA or PCI) of the shared local bus happens. If arbitration happens the bus can be driven within 4 IPB clocks by an other modules.

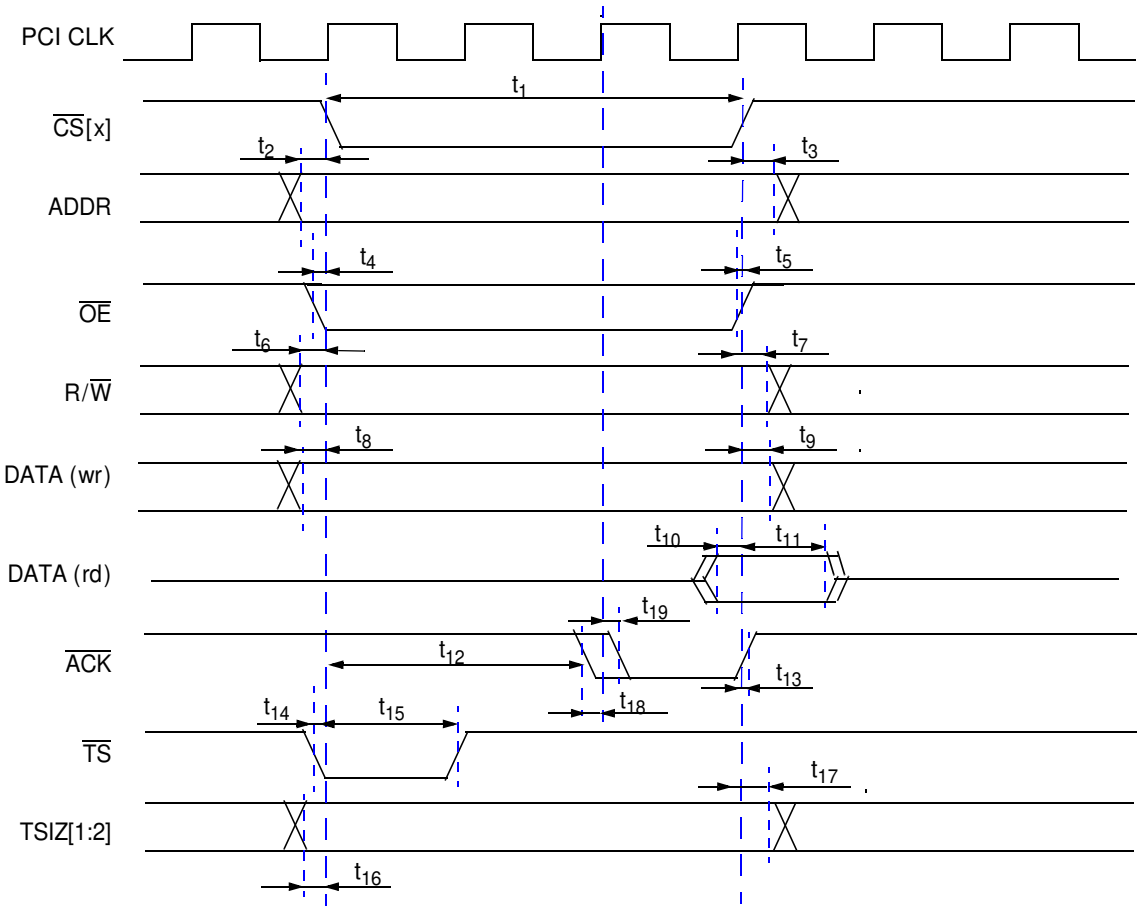


Figure 11. Timing Diagram—Non-MUXed Mode

1.3.8.2 Burst Mode

Table 25. Burst Mode Timing

Sym	Description	Min	Max	Units	Notes	SpecID
t_{CSA}	PCI CLK to CS assertion	4.6	10.6	ns	—	A7.22
t_{CSN}	PCI CLK to CS negation	2.9	7.0	ns	—	A7.23
t_1	CS pulse width	$(1 + WS + 4^{LB} \times 2 \times (32/DS)) \times t_{PCIck}$	$(1 + WS + 4^{LB} \times 2 \times (32/DS)) \times t_{PCIck}$	ns	(1),(2)	A7.24
t_2	ADDR valid before CS assertion	t_{IPBIck}	t_{PCIck}	ns	—	A7.25
t_3	ADDR hold after CS negation	–0.7	—	ns	—	A7.26
t_4	OE assertion before CS assertion	—	4.8	ns	—	A7.27
t_5	OE negation before CS negation	—	2.7	ns	—	A7.28
t_6	RW valid before CS assertion	t_{PCIck}	—	ns	—	A7.29
t_7	RW hold after CS negation	t_{PCIck}	—	ns	—	A7.30
t_8	DATA setup before rising edge of PCI clock	3.6	—	ns	—	A7.31