



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**Product Brief**

MPC533PB/D  
Rev. 0, 2/2003

MPC533/MPC534  
Product Brief


This document provides an overview of the MPC533/MPC534 microcontroller, including a block diagram showing the major modular components, sections that list the major features, and differences between the MPC533 and the MPC555. The MPC533 and MPC534 devices are members of the Motorola MPC500 RISC Microcontroller family. The parts herein will be referred to only as MPC533 unless specific parts need to be referenced.

**Table 1. MPC533/MPC534 Features**

Device	Flash	Code Compression
MPC533	512 Kbytes	Code compression not supported
MPC534	512 Kbytes	Code compression supported

# 1 Introduction

The MPC533 device offers the following features:

- 32-bit single issue PowerPC™ core
- Unified system integration unit (USIU) with a flexible memory controller and enhanced interrupt controller (EIC)
- 64-bit floating-point unit (FPU)
- 512-Kbytes of Flash EEPROM memory
  - Typical endurance of 100,000 write/erase cycles @ 25°C
  - Typical data retention of 100 years @ 25°C
- 32-Kbytes of static RAM in one CALRAM module, configured as
  - 28-Kbyte normal access only array
  - 4-Kbyte normal access or overlay access array (eight 512-byte regions)
- One 22-timer channel modular I/O system (MIOS14)
- One TouCAN module (TouCAN B)
- Enhanced queued analog system (QADC64E)
- One queued serial multi-channel module (QSMCM), which contains one queued serial peripheral interface (QSPI) and two serial controller interfaces (SCI/UART)
- One peripheral pin multiplexing module (PPM) with a parallel to serial driver

- Debug features:
  - Nexus debug port (Level 3)
  - Background debug mode (BDM)
  - IEEE1194.1 compliant interface (JTAG)
- Plastic ball grid array (PBGA) packaging
  - 388 ball PBGA
  - 27 mm x 27 mm body size
  - 1.0 mm ball pitch
- 40-MHz operation
- -40°C–85°C
- Two power supplies
  - 5-V I/O ( $5.0 \pm 0.25$  V)
  - $2.6 \pm 0.1$ -V external bus with a 5-V tolerant I/O system
  - $2.6 \pm 0.1$ -V internal logic
  - IRAMSTBY on-chip voltage regulator

## 1.1 Block Diagram

Figure 1 is a block diagram of the MPC533.

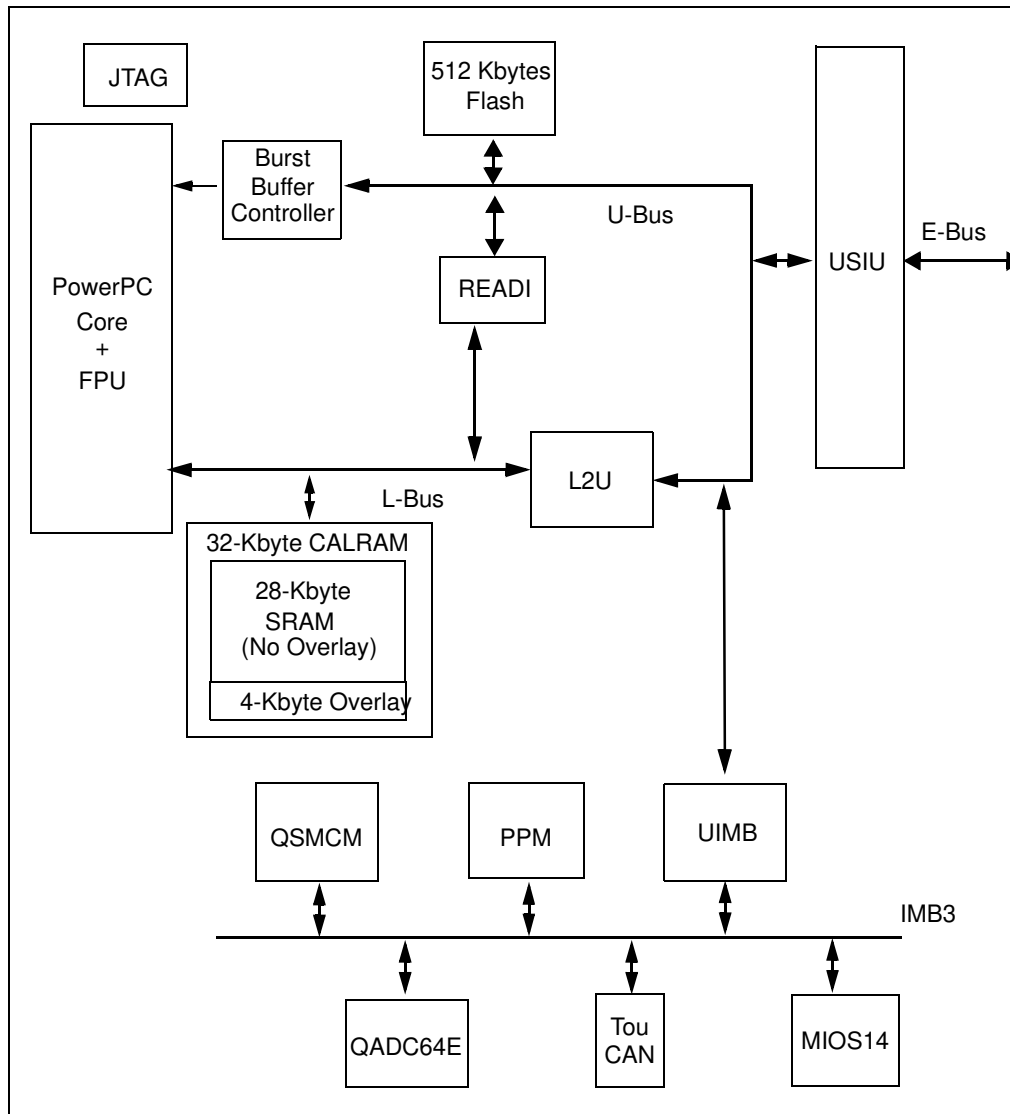


Figure 1. MPC533 Block Diagram

## 1.2 Key Features

The MPC533 key features are explained in the following sections.

### 1.2.1 High Performance CPU System

- Fully static design
- Four major power saving modes
  - On, doze, sleep, deep-sleep, and power-down



### 1.2.1.1 RISC MCU Central Processing Unit (RCPU)

- 32-bit single issue PowerPC core
- Precise exception model
- 64-bit floating point unit (FPU)
- Code compression supported on MPC534
  - Reduces usage of internal/external Flash memory (up to 50% for code)
  - The code compression feature is optimized for automotive (non-cached) applications
- Extensive system development support
  - On-chip watchpoints and breakpoints
  - Program flow tracking

### 1.2.1.2 MPC500 System Interface (USIU)

- System configuration and protection features:
  - Periodic-interrupt timer
  - Bus monitor
  - Software watchdog timer
  - Real-time clock (RTC)
  - PPC decrementer
  - Time base
- Clock synthesizer
- Power management
- Reset controller
- External bus interface that tolerates 5-V inputs, provides 2.6-V outputs, and supports multiple-master designs
- Enhanced interrupt controller that supports up to eight external and 40 internal interrupts, simplifies the interrupt structure, and decreases interrupt processing time
- USIU supports dual mapping to map part of one internal/external memory to another external memory
- External bus, supporting non-wraparound burst for instruction fetches, with up to 8 instructions per memory cycle

### 1.2.1.3 Burst Buffer Controller (BBC) Module

- Support for enhanced interrupt controller (EIC)
- Support for enhanced exception table relocation feature
- Branch target buffer
- Contains 2 Kbytes of decompression RAM (DECRAM) for code compression. This RAM may also be used as general-purpose RAM when code compression feature not used.

### 1.2.1.4 Flexible Memory Protection Unit

- Flexible memory protection units (MPU) in BBC and L2U
- Default attributes available in one global entry
- Attribute support for speculative accesses
- Up to eight memory regions are supported, four for data and four for instructions

### 1.2.1.5 Memory Controller

- Four flexible chip selects via memory controller
- 24-bit address and 32-bit data buses
- 4-Kbyte to one 16-Mbyte (data) or 4-Gbyte (instruction) region size support
- Supports enhanced external burst
- Up to eight-beat transfer bursts, two-clock minimum bus transactions
- Use with SRAM, EPROM, flash and other peripherals
- Byte selects or write enables
- 32-bit address decodes with bit masks
- Four regions

### 1.2.1.6 512-Kbytes of CDR3 Flash EEPROM Memory (UC3F)

- One 512-Kbyte module
- Page read mode
- Block (64 Kbytes) erasable
- External 4.75- to 5.25-V VFLASH power supply for program, erase, and read operations
- Typical endurance of 100,000 write/erase cycles @ 25°C
- Typical data retention of 100 years @ 25°C

### 1.2.1.7 32-Kbyte Static RAM (CALRAM)

- Composed of one 32-Kbyte CALRAM module
  - 28-Kbyte static RAM
  - 4-Kbyte calibration (overlay) RAM feature that allows calibration of flash-based constants
- Eight 512-byte overlay regions
- One clock fast accesses
- Two clock cycle access option for power saving
- Keep-alive power (IRAMSTBY) for data retention

### 1.2.1.8 General Purpose I/O Support (GPIO)

- 24 address pins and 32 data pins can be used for general-purpose I/O in single-chip mode
- 16 GPIO in MIOS14
- Many peripheral pins can be used as GPIO when not used as primary functions
- 2.6-V outputs on external bus pins
- 5-V outputs with slew rate control

## 1.2.2 Nexus Debug Port (Class 3)

- Compliant with Class 3 of the IEEE-ISTO 5001-1999
- Program trace via branch trace messaging (BTM)
- Data trace via data write messaging (DWM) and data read messaging (DRM)
- Ownership trace via ownership trace messaging (OTM)
- Run-time access to on-chip memory map and special purpose registers (SPRs) via the READI read/write access protocol
- Watchpoint messaging via the auxiliary port
- 9 or 16 full-duplex auxiliary pin interface for medium and high visibility throughput
- All features configurable and controllable via the auxiliary port
- Security features for production environment
- Supports the RCPU debug mode via the auxiliary port
- READI module can be reset independent of system reset

## 1.2.3 Integrated I/O System

### 1.2.3.1 22-Channel Modular I/O System (MIOS14)

- Six modulus counter sub-modules (MCSM)
- 10 double-action sub-modules (DASM)
- 12 dedicated PWM sub-modules (PWMSM)
- One MIOS14 16-bit parallel port I/O sub-modules (MPIOSM)

### 1.2.3.2 Enhanced Queued Analog-to-Digital Converter Module (QADC64E)

- Queued analog-to-digital converter module (QADC64E\_A) providing a total of 16 analog channels using internal multiplexing
- Directly supports up to four external multiplexers
- Up to 41 total input channels on the QADC64E module with external multiplexing
- Software configurable to operate in enhanced or legacy (MPC555 compatible) mode
- Unused analog channels can be used as digital input/output pins
- GPIO on all channels in enhanced mode
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of less than 5  $\mu$ s (>200 K samples/second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
  - External edge trigger
  - Software command
  - Periodic/interval timer within QADC64E module, that can be assigned to both queue 1 and 2
  - External gated trigger (queue 1 only)
- 64 result registers
  - Output data is right- or left-justified, signed or unsigned.
- Alternate reference input (ALTREF), with control in the conversion command word (CCW)

### 1.2.3.3 One CAN 2.0B Controller (TouCAN) Module

- One TouCAN module (TouCAN B)
- TouCAN provides the following features:
  - 16 message buffers, programmable I/O modes
  - Maskable interrupts
  - Independent of the transmission medium (external transceiver is assumed)
  - Open network architecture, multi-master concept
  - High immunity to EMI
  - Short latency time for high-priority messages
  - Low-power sleep mode, with programmable wake-up on bus activity

### 1.2.3.4 Queued Serial Multi-Channel Module (QSMCM)

- One queued serial module with one queued SPI and two SCIs (QSMCM)
- QSMCM matches full MPC555 QSMCM functionality
- Queued SPI
  - Provides full-duplex communication port for peripheral expansion or inter-processor communication
  - Up to 32 preprogrammed transfers, reducing overhead
  - Synchronous serial interface with baud rate of up to system clock / 4
  - Four programmable peripheral-selects pins:
    - Support up to 16 devices with external decoding
    - Support up to eight devices with internal decoding
  - Special wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial analog-to-digital (A/D) converters
- SCI
  - UART mode provides NRZ format and half- or full-duplex interface
  - 16 register receive buffers and 16 register transmit buffers on one SCI
  - Advanced error detection and optional parity generation and detection
  - Word-length programmable as eight or nine bits
  - Separate transmitter and receiver enable bits, and double buffering of data
  - Wake-up functions allow the CPU to run uninterrupted until either a true idle line is detected, or a new address byte is received

### 1.2.3.5 Peripheral Pin Multiplexing (PPM)

- Synchronous serial interface between the microprocessor and an external device
- Two internal parallel data sources can be multiplexed through the PPM
  - MIOS14: 12 PWM channels, four MDA channels
  - Internal GPIO: 16 general-purpose inputs, 16 general-purpose outputs
- Software configurable stream size
- Software configurable clock (TCLK) based on system clock
- Software selectable clock modes (SPI mode and TDM mode)



- Software selectable operation modes
  - Continuous mode
  - Start-transmit-receive (STR) mode
- Software configurable internal modules interconnect (shorting)

## 1.3 MPC533 Optional Features

The following features of the MPC533 are optional features and may not appear in certain configurations:

- Code compression on MPC534

## 2 Comparison of MPC533 and MPC555

The MPC533 is a derivative of the MPC555. Most functional features of the MPC555 are unchanged on the MPC533. Refer to Table 2 for a comparison of features.

**Table 2. Differences Between MPC555 and MPC533**

Module	MPC555	MPC533
CPU Core	Identical	
BBC	Basic	Enhanced Code Compression (classes scheme with 2 Kbytes DEGRAM) Code Compression is available only on MPC534.
L2U	Identical	
SRAM	26 Kbytes	32 Kbytes calibration SRAM with overlay features
Flash	448-Kbyte CMF (2 modules, 256-Kbyte and 192-Kbyte)	512-Kbyte UC3F (1 module)
USIU	Basic	Enhanced Interrupt Controller
JTAG	Selectable by RCW	Selectable at $\overline{\text{PORESET}}$
READI	None	New Debut Module (Class 3 Nexus IEEE-ISTO 5001-1999)
UIMB	Identical	
QADC64	(2)	(1) Enhanced
QSMCM	(1) Identical (1)	
MIOS	MIOS1	MIOS14 4 Extra PWMSM 4 Extra MCSM no Real-Time Clock
TouCAN	(2) Identical (1)	
PPM	—	New Module

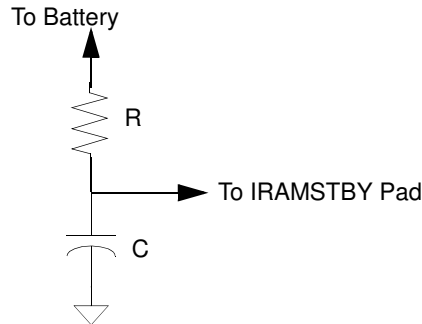
## 2.1 Additional MPC533 Differences

- The MPC533 is very similar to the MPC555 with the following differences:
  - CDR3 technology
  - Two power supplies: 5.0-V I/O, 2.6-V external bus pins, 2.6-V internal logic
  - New modules: READI, CALRAM, PPM
  - One less TouCAN module, 6 Kbytes extra of SRAM on L-bus (32 Kbytes total) (with CALRAM overlay features)
- QADC64
  - GPO on all channel pins in addition to GPI functions
- TouCAN, QSMCM, UIMB, Core, L2U
  - No changes
- BBC
  - Enhanced interrupt controller support
  - Enhanced exception relocation table
  - Branch target buffer
  - 2 Kbytes of decompression RAM for code compression. This may also be used as general-purpose RAM while not used for code compression.
- CALRAM (with overlay features)
  - New module
  - Overlay features allow calibration of Flash-based constants
- UC3F (U-bus CDR3 Flash module)
  - 512 Kbytes of non-volatile memory (NVM)
  - Designed for use in embedded microcontroller (MCU) applications targeted for high speed read performance and high density byte count requirements
- READI
  - New module
- USIU
  - Enhanced interrupt controller
  - ENGCLK default frequency
  - READI support
  - Reduced data setup time
  - Enhanced external burst support
- MIOS14
  - Four additional PWM channels
  - Four additional MCSM timers
- PPM (peripheral pin multiplexing)
  - New module
  - Two-to-one multiplexing
  - Parallel to serial (SPI and TDM)

### 3 SRAM Keep-Alive Power Behavior

One keep-alive power pin (IRAMSTBY) provides keep-alive power to RAM.

The IRAMSTBY pin can be powered directly from a battery using an internal shunt regulator or via a small battery for standby use. See Figure 2.



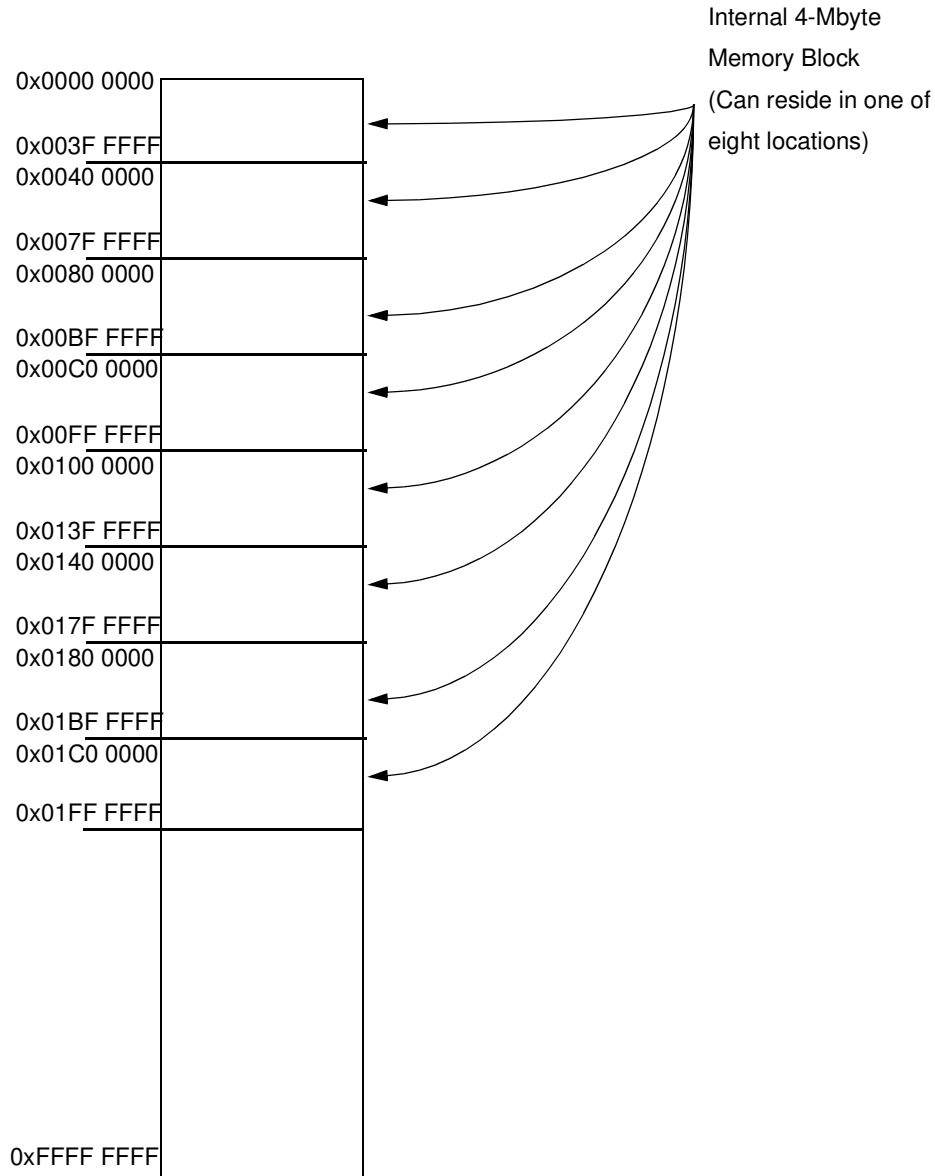
**Figure 2. Recommended Connection Diagram for IRAMSTBY**

While power is off to the MPC533, the IRAMSTBY supply powers the following:

- 32-Kbyte CALRAM
- 2-Kbyte BBC DECRAM module

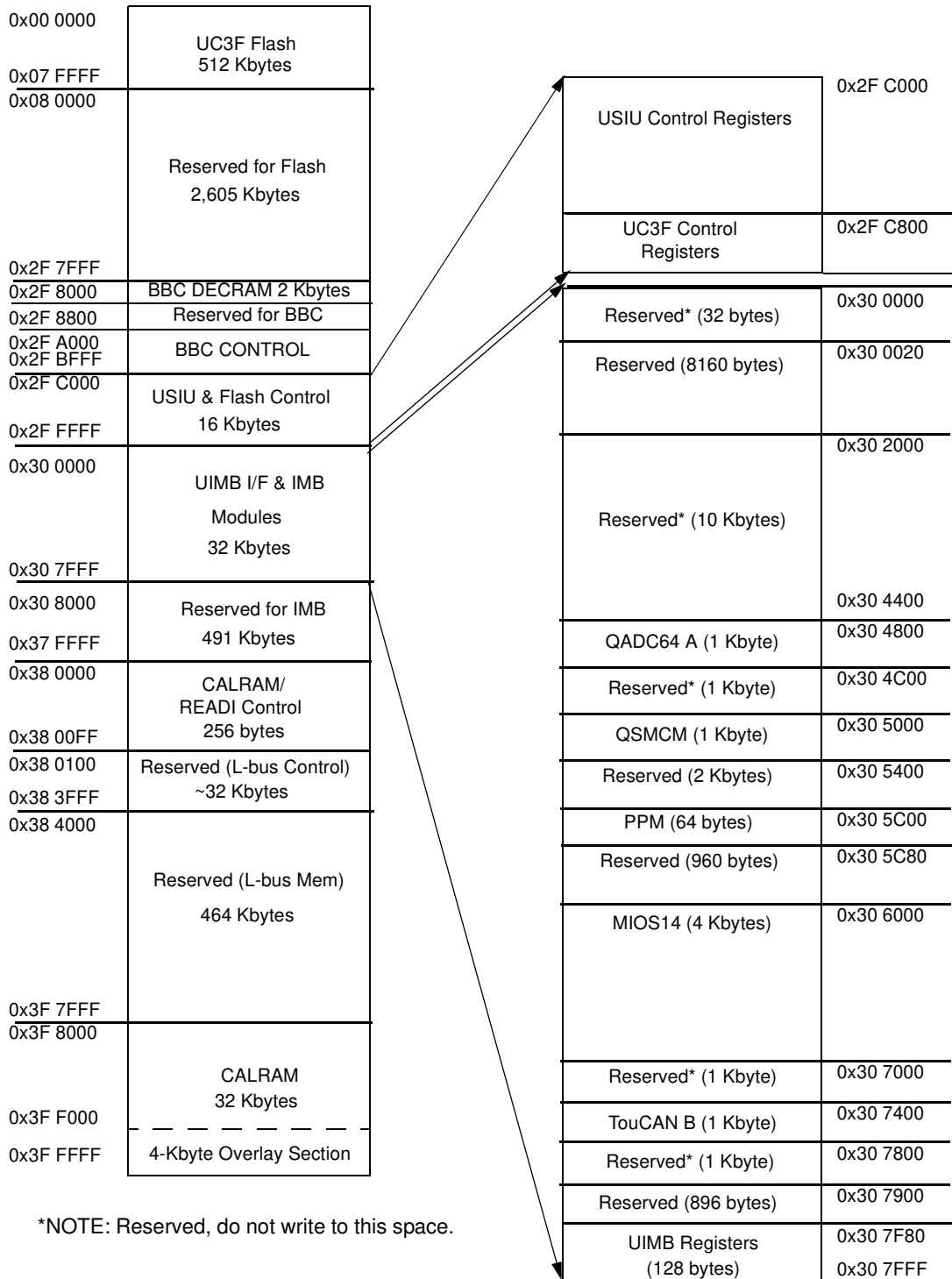
### 4 MPC533 Address Map

The internal memory map is organized as a single 4-Mbyte block. The user can assign this block to one of eight locations by programming a register in the USIU (IMMR[ISB]). The eight possible locations are the first eight 4-Mbyte memory blocks starting with address 0x0000 0000 (refer to Figure 3). The programmability of the internal memory map location allows the user to implement a multiple-chip system.


**Figure 3. MPC533 Memory Map**

The internal memory space is divided into the following sections. Refer to Figure 4.

- Flash memory (512-Kbytes)
- CALRAM static RAM memory (32-Kbytes)
- Control registers and IMB3 modules (64 Kbytes)
  - BBC control registers (16-Kbytes)
  - USIU and Flash control registers (16-Kbytes)
  - UIMB interface and IMB3 modules (32-Kbytes)
  - CALRAM/READI control registers (256-bytes)



**Figure 4. MPC533 Internal Memory Map**

## 5 MPC533 Pinout Diagram

Figure 5 shows the pinout for the MPC533.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSSA	VRL	A_AN3_A NZ_POB3	A_AN51_P QB7	A_AN55_ POA3	A_AN56_ POA4	VSS	VSS	VSS	VSS	VSS	ETRIG2_ PCS7	MDA13	MDA28	VSS	VSS	VDD	VSS
B	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSSA	ALTREF	A_AN2_A NY_POB2	A_AN50_P QB6	A_AN54_ MA2_PO A2	A_AN58_ POA6	VSS	VSS	VSS	VSS	VSS	ETRIG1_ PCS6	MDA14	MDA29	VSS	VDD	VSS	QVDDL
C	VSS	VSS	VDD	VSS	VSS	VSS	VSS	VSS	NVDDL	VRH	A_AN0_A NW_POB0	A_AN48_P QB4	A_AN52_ MA0_PO A0	A_AN59_ POA7	VSS	VSS	VSS	VSS	VSS	VDDH	MDA11	MDA15	VDDH	VDD	VSS	QVDDL
D	VSS	VSS	VSS	VDD	VSS	VSS	VSS	VSS	NVDDL	VDDA	A_AN1_A NX_POB1	A_AN49_P QB5	A_AN53_ MA1_PO A1	A_AN57_ POA5	VSS	VSS	VSS	VSS	VSS	VDDH	MDA12	MDA27	VDD	VSS	QVDDL	VSS
E	VDDH	VSS	VSS	VSS																			VDDH	VSS	VSS	VSS
F	PCS4	PCS5	VSS	QVDDL																			VDDH	MDA30	MDA31	MPWM0_ MD11
G	VSS	VSS	VSS	VSS																			MPWM1_ MD02	MPWM16	MPWM3_ PPM_RX1	MPWM2_ PPM_TX1
H	VSS	VSS	VSS	VSS																			MPWM17_ MD03	MPWM18_ MD06	MPWM19_ MD07	MPIO32B5_ MD05
J	VSS	VSS	VSS	VSS																			MPIO32B6_ MPWM4_ MD06	MPIO32B7_ MPWM5	MPIO32B8_ MPWM20	MPIO32B9_ MPWM21
K	VSS	VSS	VSS	VSS																			MPIO32B12_ C_CNTRX0	MPIO32B11_ C_CNTRX0	MPIO32B10_ PPM_TSYNC	MPIO32B13_ PPM_TCLK
L	JCOMP_ RS TL_B	TCK_DSCK _MCKI	B_CNTRX0	B_CNTRX0							VSS	VSS	VSS	VSS	VSS	VSS							VF0_MPIO32 B0_MDO1	VF1_MPIO32B 1_MCKO	MPIO32B15_ PPM_TX0	MPIO32B14_ PPM_RX0
M	TDL_DSDL MDI0	TMS_EVTI _B	VDDSRAM	TDO_DSD O_MDO0							VSS	VSS	VSS	VSS	VSS	VSS							NC	VF2_MPIO32B 2_MSEL_B	VFLS0_MPIO 32B3_MSE0 B	VFLS1_MPIO 32B4
N	IRQ3_B_KR _B_RETRY _B_SGPIO C3	IWP0_VFL S0	IWP1_VFL S1	SGPIO6_ FRZ_PTR_ B							VSS	VSS	VSS	VSS	VSS	VSS							PCS2_OGPI O2	PCS1_OGPIO1	PCS0_SS_B_ OGPIO0	VSS
P	IRQ4_B_AT 2_SGPIOC4	IRQ2_B_C R_B_SGPI OC2_MDO 5_MTS	IRQ0_B_S GPIOC0_ MDO4	IRQ1_B_R SV_B_SG PIOC1							VSS	VSS	VSS	VSS	VSS	VSS							SCK_OGPI O6	MOSI_OGPIO5	MISO_OGPI O4	PCS3_OGPI O3
R	SGPIOCT1 RQOUT_B_ LWP0	BB_B_VF2 _JWP3	BG_B_VF0 _LWP1	BR_B_VF1 _JWP2							VSS	VSS	VSS	VSS	VSS	VSS							RXD1_ OGPI1	TXD2_ OGPO2	TXD1_ OGPO1	PULL-SEL
T	WE_B_AT0	WE_B_AT1	WE_B_AT2	WE_B_AT3							VSS	VSS	VSS	VSS	VSS	VSS							EPEE	BOPEEE	VDDH	RXD2_ OGPI2
U	CS0_B	CS1_B	CS2_B	CS3_B																			CLKOUT	VSSF	VDDF	VFLASH
V	RD_WR_B	OE_B	TEA_B	TSIZ0																			VDD	EXTCLK	VSS	ENGCLK_BU CLK
W	TSIZ1	TS_B	TA_B	BDIP_B																			HRESET_B	SRESET_B	PORESET_B _TRST_B	KAPWR
Y	BURST_B	BI_B_STS _B	ADDR_SG PIOA12	ADDR_SG PIOA11																			NVDDL	IRQ7_B_MODC K3	RSTCONF_B _TEXP	VDDSYN
AA	VSS	VSS	VSS	QVDDL																			VSS	VSS	VSS	XFC
AB	VSS	VSS	QVDDL	VSS																			QVDDL	VSS	VSS	VSSSYN
AC	VSS	QVDDL	VSS	NVDDL	VSS	ADDR_SG IOA10	ADDR_SG PIOA18	ADDR_SGPI OA20	ADDR_SG PIOA23	NVDDL	ADDR_S GPIOA26	DATA_SG PIOD1	DATA_SG PIOD5	DATA_SG PIOD7	NVDDL	DATA_SG PIOD9	DATA_SGPI IOD11	DATA_SG PIOD12	NVDDL	DATA_S GPIO14	VSS	VDD	VSS	QVDDL	VSS	EXTAL
AD	QVDDL	VSS	NVDDL	VSS	VSS	QVDDL	ADDR_SG PIOA13	ADDR_SGPI OA16	ADDR_SG PIOA19	ADDR_SGPI IOA21	ADDR_S GPIOA24	ADDR_SG PIOD25	DATA_SG PIOD28	DATA_SG PIOD29	DATA_SG PIOD26	DATA_SG PIOD24	DATA_SGPI IOD22	DATA_SG PIOD13	DATA_SGPI OD15	DATA_S GPIO16	IRQ5_B_S GPIOC5_M ODCK1	VSS	VDD	VSS	QVDDL	XTAL
AE	VSS	NVDDL	VSS	VSS	VSS	QVDDL	ADDR_SG PIOA14	ADDR_SGPI OA17	ADDR_SG PIOA31	ADDR_SGPI IOA30	ADDR_S GPIOA28	ADDR_SG PIOD29	DATA_SG PIOD30	DATA_SG PIOD29	DATA_SG PIOD27	DATA_SG PIOD25	DATA_SGPI IOD23	DATA_SG PIOD21	DATA_SGPI OD19	DATA_S GPIO17	IRQ6_B_M ODCK2	VSS	VSS	VDD	VSS	QVDDL
AF	NVDDL	VSS	VSS	VSS	VDDH	VSS	ADDR_SG PIOA15	ADDR_SGPI OA9	ADDR_SG PIOA8	ADDR_SGPI IOA22	ADDR_S GPIOA27	DATA_SG PIOD3	DATA_SG PIOD3	DATA_SG PIOD2	DATA_SG PIOD4	DATA_SG PIOD6	DATA_SGPI IOD8	DATA_SG PIOD10	DATA_SGPI OD20	DATA_S GPIO18	VDDH	VSS	VSS	VSS	VDD	VSS

(As viewed from top, through the package and silicon)

VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS

Figure 5. MPC533 Pinout Diagram

MOTOROLA

MPC533/MPC534 Product Brief

13

For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)

## 6 Supporting Documentation List

This list contains references to currently available and planned documentation.

- *MPC555 User's Manual* (MPC555UM/AD)
- *MPC533 Reference Manual* (MPC533RM/D)
- *RCPU Reference Manual* (RCPURM/AD)
- Nexus Standard Specification (non-Motorola document)
- Nexus Web Site: <http://www.nexus5001.org/>
- IEEE 1149.1 Specification (non-Motorola document)



THIS PAGE INTENTIONALLY LEFT BLANK

**Freescale Semiconductor, Inc.**

## HOW TO REACH US:

### USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution  
P.O. Box 5405, Denver, Colorado 80217  
1-303-675-2140 or 1-800-441-2447

### JAPAN:

Motorola Japan Ltd.  
SPS, Technical Information Center  
3-20-1, Minami-Azabu Minato-ku  
Tokyo 106-8573 Japan  
81-3-3440-3569

### ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.  
Silicon Harbour Centre, 2 Dai King Street  
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong  
852-26668334

### TECHNICAL INFORMATION CENTER:

1-800-521-6274

### HOME PAGE:

<http://www.motorola.com/semiconductors>

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein.

Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.



Motorola and the Stylized M Logo are registered in the U.S. Patent and Trademark Office. digital dna is a trademark of Motorola, Inc. The described product contains a PowerPC processor core. The PowerPC name is a trademark of IBM Corp. and used under license. All other product or service names are the property of their respective owners. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

© Motorola, Inc. 2003

MPC533PB/D

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**