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Product BriefMPC535PB/D
Rev. 0, 2/2003MPC535/MPC536
Product Brief**MOTOROLA**
intelligence everywhere™**digital dna™**

This document provides an overview of the MPC535/MPC536 microcontrollers, including a block diagram showing the major modular components, sections that list the major features, and differences between the MPC535/MPC536 and the MPC555. The MPC535 and MPC536 devices are members of the Motorola MPC500 RISC Microcontroller family. The parts herein will be referred to only as MPC535 unless specific parts need to be referenced.

Table 1. MPC535/MPC536 Features

Device	Flash	Code Compression
MPC535	1 Mbyte	Code compression not supported
MPC536	1 Mbyte	Code compression supported

1 Introduction

The MPC535 device offers the following features:

- PowerPC™ core with a floating point unit (FPU) and a burst buffer controller (BBC)
- Unified system integration unit (USIU), a flexible memory controller, and improved interrupt controller
- 1 Mbyte of Flash memory (UC3F)
 - Typical endurance of 100,000 write/erase cycles @ 25°C
 - Typical data retention of 100 years @ 25°C
- 36 Kbytes of static RAM (two CALRAM modules)
 - 8 Kbytes of normal access or overlay access (sixteen 512-byte regions)
 - 4 Kbytes in CALRAM A, 4 Kbytes in CALRAM B
- A 22-timer channel modular I/O system (MIOS14)
 - Same as MIOS1 plus a real-time clock sub-module (MRTCSM), 4 counter sub-modules (MCSM), and 4 PWM sub-modules (MPWMSM)
- One TouCAN module (TouCAN_B)
- One enhanced queued analog to digital converter (QADC64E A).
- One queued serial multi-channel module (QSMCM A) which contains a queued serial peripheral interface (QSPI) and two serial controller interfaces (SCI/UART)
- -40°C – 85°C ambient temperature

- Debug features:
 - A Nexus debug port (class 3) – IEEE-ISTO 5001-1999
 - JTAG and background debug mode (BDM)
- Packaging and Electrical

1.1 Block Diagram

Figure 1 is a block diagram of the MPC535.

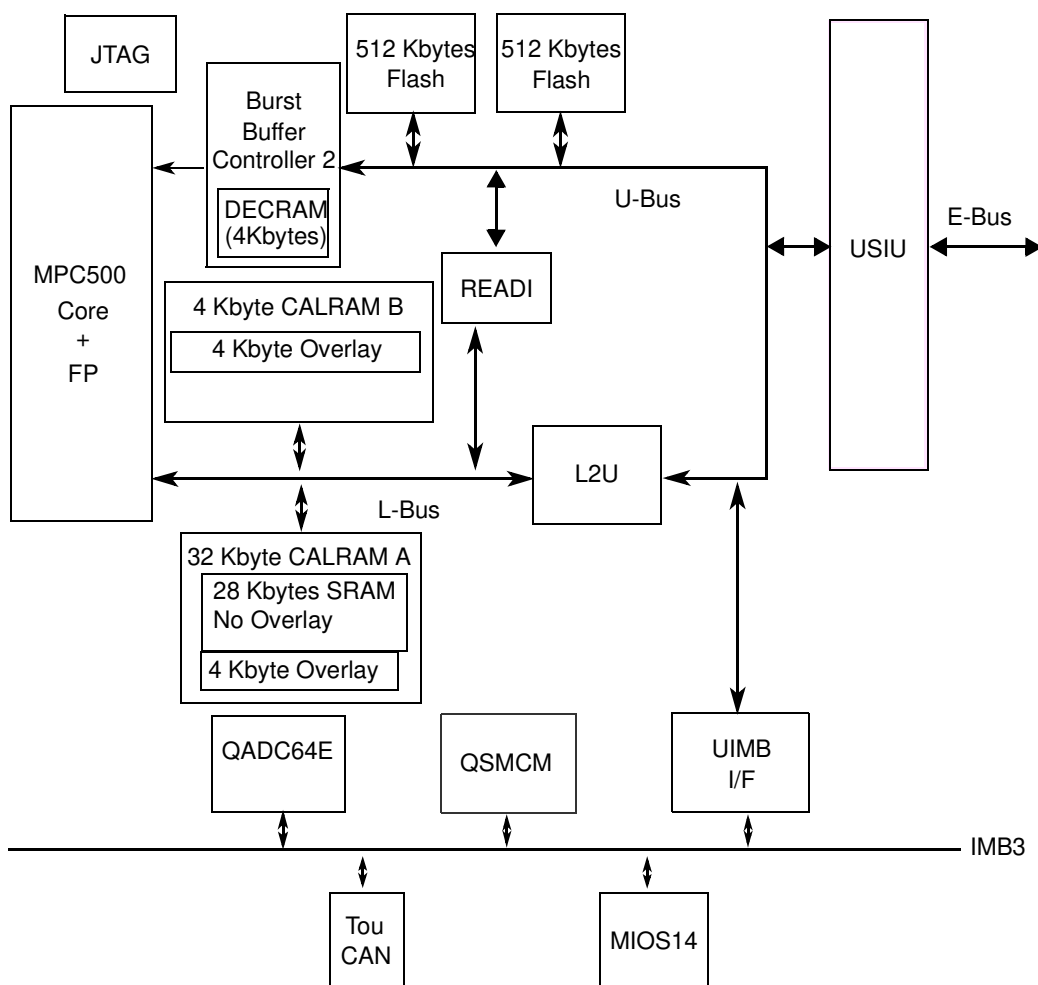


Figure 1. MPC535 Block Diagram

1.2 Detailed Feature List

The MPC535 key features are explained in the following sections.

1.2.1 High Performance CPU System

- Fully static design
- Four major power saving modes
 - On, doze, sleep, deep-sleep and power-down

1.2.2 RISC MCU Central Processing Unit (RCPU)

- High-performance core
 - PowerPC single issue integer core
 - Precise exception model
 - Floating point
 - Code compression (MPC536 only)
 - Compression reduces usage of internal or external Flash memory
 - Compression optimized for automotive (non-cached) applications
 - New compression scheme decreases code size to 40% –50% of source

1.2.3 MPC500 System Interface (USIU)

- MPC500 system interface (USIU, BBC, L2U)
- Periodic interrupt timer, bus monitor, clocks, decremter and time base
- Clock synthesizer, power management, reset controller
- External bus tolerates 5-V inputs, provides 2.6-V outputs
- Enhanced interrupt controller supports a separate interrupt vector for up to eight external and 40 internal interrupts
- IEEE 1149.1 JTAG test access port
- Bus supports multiple master designs
- USIU supports dual-mapping of Flash to move part of internal Flash memory to external bus for development
- External bus, supporting non-wraparound burst for instruction fetches, with up to 8 instructions per memory cycle

1.2.4 Burst Buffer Controller (BBC) Module

- Exception vector table relocation features allow exception table to be relocated to following locations:
 - 0x0000 0000 - 0x0000 1FFF (normal MPC500 exception table location)
 - 0x0001 0000 - 0x0001 1FFF (0 + 64 Kbytes; second page of internal Flash)
 - Second internal Flash module
 - Internal SRAM
 - 0x0FFF_0100 (external memory space; normal MPC500 exception table location)

1.2.5 Flexible Memory Protection Unit

- Flexible memory protection units in BBC (IMPU) and L2U (DMPU)
- Default attributes available in one global entry
- Attribute support for speculative accesses

1.2.6 Memory Controller

- Flexible chip selects via memory controller
- 24-bit address and 32-bit data buses
- 4- to 16-Mbyte (data) or 4-Gbyte (instruction) region size support
- Four-beat transfer bursts, two-clock minimum bus transactions
- Use with SRAM, EPROM, Flash and other peripherals
- Byte selects or write enables
- 32-bit address decodes with bit masks
- Four instruction regions
- Four data regions

1.2.7 1 Mbyte of CDR3 Flash EEPROM Memory (UC3F)

- 1 Mbyte Flash
 - Two UC3F modules, 512 Kbytes each
- Page mode read
- Block (64-Kbyte) erasable
- External 4.75- to 5.25-V VPP program and erase power supply
- Typical endurance of 100,000 write/erase cycles @ 25°C
- Typical data retention of 100 years @ 25°C

1.2.8 36-Kbyte Static RAM (CALRAM)

- 36-Kbyte static calibration RAM
 - Composed of 4-Kbyte and 32-Kbyte CALRAM modules
- Fast access: one clock
- Keep-alive power
- Soft defect detection (SDD)
- 4 Kbyte calibration (overlay) RAM per module (8 Kbytes total)
- Eight 512-byte overlay regions per module (16 regions total)

1.2.9 General Purpose I/O Support (GPIO)

- General-purpose I/O support
- Address (24) and data (32) pins can be used as GPIO in single-chip mode
- 16 GPIO in MIOS14
- Many peripheral pins can be used as GPIO when not used as primary functions
- 5-V outputs with slew rate control

1.2.10 Debug Features

- Extensive system debug support
- On-chip watchpoints and breakpoints
- Program flow tracking
- Background debug mode (BDM)

1.2.10.1 Nexus Debug Port (Class 3)

- Nexus/IEEE – ISTO 5001-1999 debug port (Class 3)
- Nine- or 16-pin interface

1.2.11 Integrated I/O System

- True 5-V I/O

1.2.11.1 22-Channel Modular I/O System (MIOS14)

- 22-channel MIOS timer (MIOS14)
- Six modulus counter submodules (MCSM)
 - Four additional MCSM submodules compared to MIOS1
- 10 double action submodules (DASM).
- 12 dedicated PWM submodules (PWMSM)
 - Four additional PWM submodules compared to MIOS1 (shared with MIOS GPIO pins)
- MIOS real-time clock submodule (MRTCSM) provides low power clock/counter
 - Requires external 32-KHz crystal
 - Uses four pins: two for 32-KHz crystal, two for power/ground.

1.2.12 One Enhanced Queued Analog-to-Digital Converter Module (QADC64E)

- One enhanced queued analog to digital converter (QADC64E A) with 16 total analog channels.
- 10 bit A/D converter with internal sample/hold
 - Typical conversion time is 4 μ s (250-Kbyte samples/sec)
 - Two conversion command queues of variable length
- Automated queue modes initiated by:
 - External edge trigger/level gate
 - Software command
 - Periodic/interval timer, assignable to both queue 1 and 2
- 64 result registers
 - Output data is right or left justified, signed or unsigned
- Conversions alternate reference (ALTREF) pin. This pin can be connected to a different reference voltage

1.2.13 One CAN 2.0B Controller (TouCAN) Module

- One TouCAN module (TouCAN_B)
- 16 message buffers, programmable I/O mode
- Maskable interrupts
- Programmable loopback for self-test operation
- Independent of the transmission medium (external transceiver is assumed)
- Open network architecture, multimaster concept

- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode, with programmable wake up on bus activity

1.2.14 Queued Serial Multi-Channel Module (QSMCM)

- One queued serial module with one queued-SPI and two SCI (QSMCM_A)
 - QSMCM_A matches full MPC555 QSMCM functionality
- Queued-SPI
 - Provides full-duplex communication port for peripheral expansion or interprocessor communication
 - Up to 32 preprogrammed transfers, reducing overhead
 - Synchronous serial interface with baud rate of up to system clock / 4
 - Four programmable peripheral-select pins support up to 16 devices
 - Special wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial analog-to-digital (A/D) converters
- SCI
 - UART mode provides NRZ format and half- or full-duplex interface
 - 16 register receive buffer and 16 register transmit buffer on one SCI
 - Advanced error detection, and optional parity generation and detection
 - Word length programmable as 8 or 9 bits
 - Separate transmitter and receiver enable bits, and double buffering of data
 - Wake-up functions allow the CPU to run uninterrupted until either a true idle line is detected, or a new address byte is received

1.2.15 Electrical Specifications and Packaging

- 40 MHz operation
- -40°C – 85°C ambient temperature
- 2.6 V \pm 0.1 V external bus
 - External bus is compatible with external memory devices operating from 2.5 V to 3.4 V.
 - Extended voltage range (2.7 – 3.4 V) degrades data drive timing by 1.1 ns on data writes.
- 2.6 \pm 0.1 V internal logic
- 5-V I/O (5.0 \pm 0.25 V)
- Plastic ball grid array (PBGA) packaging
 - 388 ball PBGA
 - 27 mm x 27 mm body size
- 1.0 mm ball pitch

1.3 MPC535 Optional Features

The following features of the MPC535 are optional features and may not appear in certain configurations:

- 40-MHz operation
- MPC536 supports code compression

2 Differences between the MPC535 and the MPC555

The MPC535 is an enhanced version of the MPC555. Most functional features of the MPC555 are unchanged on the MPC535. Table 2 shows the high level differences.

Table 2. Differences Between Modules of the MPC555 and the MPC535

Module	MPC555	MPC535
CPU Core	No Change	
BBC	BBC	BBC with improved code compression ¹
L2U	No Change	
SRAM	26-Kbytes	36-Kbyte CALRAM with overlay features
Flash	448-Kbyte CMF	1-Mbyte UC3F (new programming, etc.)
USIU	USIU	USIU with enhanced interrupt controller
JTAG	No Change	
READI	None	New Module
UIMB	No Change	
QADC64	2 QADC64 (16 channels on each QADC for 32 total channels)	1 QADC64E (16 channels accessible)
QSMCM	(1) No Change (1)	
MIOS	MIOS1	MIOS14: MIOS1 with real-time clock (MRTC SM), 4 more PWMSMs and 4 more MCSMs
TouCAN	(2) No Change (1)	
Power Supplies		
—	40 MHz with two power supplies: nominal 3.3-V to 5.0-V power supplies	40 MHz with two power supplies: 5.0-V I/O, 2.6-V internal logic

¹ Available on some options.

2.1 Additional MPC535 Differences

The following are additional differences between the MPC555 and the MPC535.

- SPI (MISO, MOSI, and SCK) pin drive.
 - MPC535 provides 21-ns rise/fall with 200-pf load using CMOS (20%/70%) levels
- GPIO on MODCK1 pin outputs only 2.6 V
 - MODCK1 pin is in keep-alive power section with no 5-V rail available
 - 5.0-V compatibility modes
 - Input is 5-V friendly
 - 2.6-V output has less slew rate control
 - 2.6-V: V_{OH} = 2.3 V
- Power supplies for external bus pins
 - QVDDL is quiet supply to hold non-switching outputs quiet even when noisy supply (NVDDL) sags
 - QVDDL supplies pre-drive and other pad logic
 - NVDDL only supplies final PMOS driver stage
 - QVDDL and NVDDL shorted on customer board after filtering
- Pull-up and pull-down changes during PORESET and HRESET
 - All 2.6-V/5-V pads (external bus: address/data/control) pull down at reset
 - All 5-V pads pull up at reset
 - Additional control granularity in the PDMCR register
- No pull-ups on QSMCM SCI receive pads
- A_RXD1_QGPI1, A_RXD2_QGPI2 pins do not have weak pull-up during reset or any other time
- CLKOUT has 3 drive strength options
 - Better matches drive to requirements to reduce EMI
 - 25, 50, 100 pf instead of 45 and 90 pf
- Change reset value of ENGCLK to maximum divide (crystal/128)
 - For a 4-MHz crystal, this is 31.25 KHz
 - ENGCLK is selectable between 2.6 V and 5 V
- A daisy chain between UC3F modules allows either module to provide the reset configuration word (RCW)
- Censorship operation
 - A RCW bit controls whether or not the entire UC3F can be erased while censorship is violated
- BBC SPRs (PPC regs) access in two clocks instead of one clock
- CALRAM internal protection block size is 8 Kbytes
 - Instead of 4 Kbytes on MPC555 LRAM
- CALRAM causes machine check exception instead of data storage interrupt (DSI) exception in certain cases
 - For non-overlay CPU core accesses, a DSI exception is taken
 - For overlay accesses and any non-core access (slave mode), a machine check exception is taken

- CALRAM causes DSI exception only if the data relocation (DR) bit in the core machine state register, MSR[DR], is set.
 - L2U on MPC555 already followed this protocol, but the LRAM did not. Now all L-bus peripherals follow this protocol.
 - The MSR[DR] bit is described in the reference manual for more information.
- Four additional PRDS control bits were added to the USIU to allow more granularity of PRDS control on a part
- BBC includes a 4-Kbyte DECRAM that can be used if compression is not used or is not available.

3 SRAM Keep-Alive Power Behavior

The SRAM has three keep-alive power pins (VDDSRAM1, VDDSRAM2, and VDDSRAM3). These pins provide keep-alive power to the SRAM arrays in the CALRAM modules.

The VDDSRAM1 pin powers the 32-Kbyte CALRAM A during keep-alive while power is off to the MPC535 (except for the keep-alive power supplies). CALRAM A keeps all of its 32 Kbytes powered during power down.

The VDDSRAM2 pin powers the 4-Kbyte CALRAM B module. The CALRAM modules only power their arrays from the VDDSRAM pins during keep-alive. During normal operation, they are powered by the normal internal VDD of the part.

The 4-Kbyte DECRAM in the BBC module power its arrays via the VDDSRAM3 pin during keep-alive and are supplied by VDD during normal operation.

4 MPC535 Memory Map

The internal memory map is organized as a single 4-Mbyte block. This is shown in Figure 3. This block can be moved to one of eight different locations. The internal memory space is divided into the following sections:

- Flash memory (1 Mbyte) — U-bus memory
- Static RAM memory (36 Kbytes CALRAM) — L-bus memory
- Control registers and IMB3 modules (64 Kbytes), partitioned as
 - USIU and flash control registers
 - UIMB interface and IMB3 modules
 - CALRAM and READI control registers (L-bus control register space)

The internal memory block can reside in one of eight possible 4-Mbyte memory spaces. These eight locations are the first eight 4-Mbyte memory blocks starting with address 0x0000 0000, as shown in Figure 2. There is a user programmable register in the USIU to configure the internal memory map to one of the eight possible locations. Programmability of internal memory map location allows multiple chip system.

The IMB3 address space block in Figure 3 shows memory allocation for IMB3 modules. It does not show the actual memory space required for individual modules. All modules are mapped to the low address, numerically, of the memory allocated for that module in the IMB3 address space.

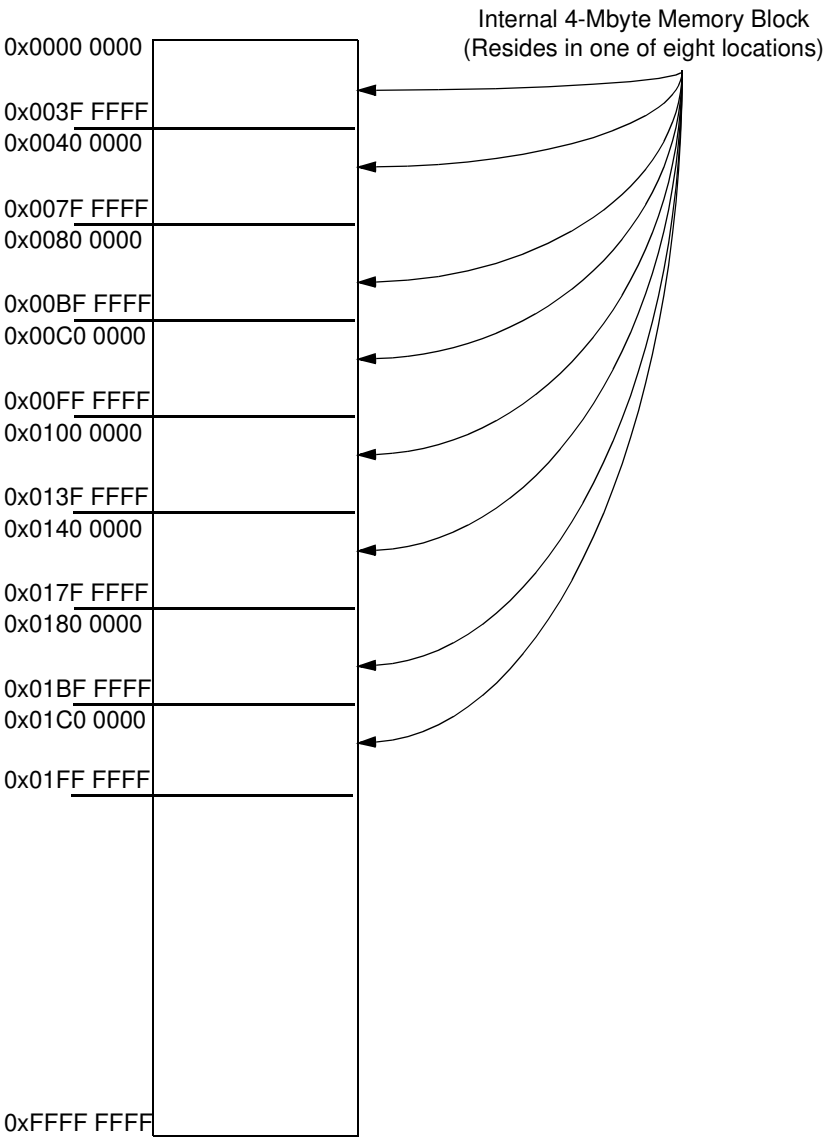


Figure 2. Memory Map

0x00 0000	UC3F_A Flash 512 Kbytes	USIU Control Registers	0x2F C000
0x07 FFFF		UC3F_A Control (64 bytes)	0x2F C800
0x08 0000	UC3F_B Flash 512 Kbytes	UC3F_B Control (64 bytes)	0x2F C840
0x0F FFFF			0x2F C87F
0x10 0000	Reserved for Flash (2,016 Kbytes)		
0x2F 7FFF		Reserved* (144 bytes)	0x30 0000
0x2F 8000	DECRAM 4 Kbytes		
0x2F 8FFF			0x30 0080
0x2F 9000	Reserved	Reserved (3952 bytes)	0x30 0090
0x2F 9FFF			
0x2F A000	BBC Control Registers 8 Kbytes	Reserved* (10 Kbytes)	0x30 1000
0x2F BFFF			0x30 2000
0x2F C000	USIU & Flash Control 16 Kbytes	Reserved (2 Kbytes)	0x30 3800
0x2F FFFF		Reserved* (2 Kbytes)	0x30 4000
0x30 0000	UIMB I/F & IMB Modules 32 Kbytes		0x30 4400
0x30 7FFF		QADC64_A (1 Kbytes)	0x30 4800
0x30 8000	Reserved for IMB 480 Kbytes	Reserved* (1 Kbytes)	0x30 4C00
0x37 FFFF		QSMCM_A (1 Kbytes)	0x30 5000
0x38 0000	CALRAM/ Readi Control 256 bytes	Reserved* (1 Kbytes)	0x30 5400
0x38 00FF		Reserved (1 Kbytes)	0x30 5800
0x38 0100	Reserved (L-bus Control) ~32 Kbytes	Reserved* (1 Kbytes)	0x30 5C00
0x38 3FFF		MIOS14 (4 Kbytes)	0x30 6000
0x38 4000	Reserved (L-bus Mem) 444 Kbytes	Reserved* (1 Kbytes)	0x30 7000
0x3F 6FFF		TOUCAN_B (1 Kbytes)	0x30 7400
0x3F 7000	All 4-Kbytes can be Overlay Section	Reserved* (1 Kbytes)	0x30 7800
0x3F 7FFF	CALRAM_B (4 Kbyte)	Reserved (896 bytes)	0x30 7900
0x3F 8000		UIMB Control Registers (128 bytes)	0x30 7F80
	CALRAM_A (32 Kbyte)		0x30 7FFF

0x3F FFFF	4-Kbyte Overlay Section		

Note: Reserved, do not write to this space.

Figure 3. Internal Memory Block

5 MPC535 Pinout Diagram

Figure 4 shows the pinout for the MPC535.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26			
A	VDD	VSS	VRH	VRL	VSS	VSS	AN48_A_POB4	AN53_A_MA1_POA1	VDDA	VSSA	VSS	VSS	VSS	VSS	QVDDL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	A		
B	VSS	VDD	AN44_A_POB0	ALTREF	VSS	VSS	AN49_A_POB5	AN52_A_MA0_POA0	AN56_A_PQA4	AN58_A_PQA6	VSS	VSS	VSS	VSS	QVDDL	ETRIG2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	B		
C	VDDRTC	VSS	VDD	AN45_A_POB1	VSS	VSS	AN46_A_POB2	AN50_A_PQA6	AN54_A_MA2_POA2	AN57_A_POA5	VSS	VSS	VSS	VSS	QVDDL	ETRIG1	B_CNRX0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VSS	C		
D	EXTAL32	VDDSRAM2	VSS	VDD	VDDH	VSS	AN82	AN47_A_POB3	AN51_A_PQA3	AN55_A_PQA3	AN59_A_PQA7	VSS	VSS	VSS	QVDDL	VDDH	VSS	VSS	VSS	VSS	VSS	NVDDL	VSS	VDD	VSS	VSS	D		
E	XTAL32	B_CNTX0	VDDSRAM1	VSS																			VDD	VSS	VSS	MPWM17	E		
F	VSSRTC	VSS	VSS	NVDDL																			MPWM5_MPIO32B6	MPWM18	MDA11	MDA13	F		
G	VSS	VSS	VSS	VDDSRAM3																			MDA12	MDA27	MDA28	MDA29	G		
H	VSS	VSS	VSS	VSS																			MDA30	MDA31	MPWM0	MPWM1	H		
J	VSS	VSS	VSS	VSS																			MPWM3	MPWM2	MPWM16	MPWM20_MPIO32B11	J		
K	VSS	VSS	VSS	VSS																			MDA15	MDA14	MPWM21_MPIO32B12	MPIO32B13	K		
L	MDI_0	TCK_DSCK	MDI_1	MCKI											VSS	VSS	VSS	VSS	VSS	VSS					MPIO32B14	MPIO32B15	MPWM19	VF0_MPIO32B0	L
M	TDI_DSDI	EVTI_B	RSTI_B	MSEI_B											VSS	VSS	VSS	VSS	VSS	VSS					VF1_MPIO32B1	VF2_MPIO32B2	MPWM4_MPIO32B5	VFLS0_MPIO32B3	M
N	TMS	MDO_4_MPIO32B10	MDO_6_MPIO32B8	MDO_5_MPIO32B9											VSS	VSS	VSS	VSS	VSS	VSS					VDDH	VFLS1_MPIO32B4	VSS	VSS	N
P	MDO_7_MPIO32B7	JCOMP	MCKO	MDO_0											VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VSS	VSS	P
R	MDO_1	TDO_DSDO	MDO_2	IWP1_VFLS1											VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VSS	VSS	R
T	MDO_3	MSEO_B	IWP0_VFLS0	SGPIOC6_FRZ_PTR_B											VSS	VSS	VSS	VSS	VSS	VSS					A_TXD1_OGPI01	A_MISO_OGPI04	VSS	A_SCK_OGPI06(C3F_CLK)	T
U	ADDR_SGPIOA16	ADDR_SGPIOA17	ADDR_SGPIOA8	NVDDL																	A_PCS2_OGPI02	A_RXD1_QP1(C3F_SUP1)	A_MOSI_OGPI05	A_PCS3_OGPI03(C3F_IOUT)	U				
V	ADDR_SGPIOA18	ADDR_SGPIOA19	ADDR_SGPIOA9	ADDR_SGPIOA10																	A_PCS0_SS_B_OGPI00	A_TXD2_OGPI02	A_RXD2_QP2(C3F_SUP2)	VSS	V				
W	ADDR_SGPIOA20	ADDR_SGPIOA21	ADDR_SGPIOA1	ADDR_SGPIOA12																			NVDDL	VFLASH	A_PCS1_OGPI01	PULLSEL	W		
Y	ADDR_SGPIOA22	ADDR_SGPIOA23	ADDR_SGPIOA13	ADDR_SGPIOA14																			VDDF	EXTCLK	NC	KAPWR	Y		
AA	ADDR_SGPIOA24	ADDR_SGPIOA25	ADDR_SGPIOA15	ADDR_SGPIOA30																			PORESET_B_TRST_B	VSS	VSSF	XTAL	AA		
AB	ADDR_SGPIOA26	ADDR_SGPIOA27	ADDR_SGPIOA31	QVDDL																			HRESET_B	IRQ6_B_MODCK2	RSTCONF_B_TEXP	EXTAL	AB		
AC	ADDR_SGPIOA28	NC	QVDDL	VSS	VDD	VDDH	DATA_SGPIOD29	DATA_SGPIOD27	NVDDL	DATA_SGPIOD24	DATA_SGPIOD22	DATA_SGPIOD20	NVDDL	SGPIOC7_IRQOUT_B_LWP0	NVDDL	WE_B_AT1	NVDDL	CS3_B	BI_B_STS_B	VDDH	VDD	VSS	QVDDL	SRESET_B	IRQ7_B_MODCK3	VSSSN	AC		
AD	ADDR_SGPIOA25	QVDDL	VSS	VDD	NC	DATA_SGPIOD31	DATA_SGPIOD30	DATA_SGPIOD28	DATA_SGPIOD26	DATA_SGPIOD25	DATA_SGPIOD23	DATA_SGPIOD21	DATA_SGPIOD19	IRQ4_B_AT2_SGPIOC4	TEA_B	IRQ2_B_CR_B_SGPIOC2	WE_B_AT2	CS1_B	TSIZ0	BOEPEE	CLKOUT	VDD	VSS	QVDDL	IRQ5_B_SGPIOC5_MODCK1	XFC	AD		
AE	QVDDL	VSS	VDD	DATA_SGPIOD1	DATA_SGPIOD3	DATA_SGPIOD5	DATA_SGPIOD7	DATA_SGPIOD9	DATA_SGPIOD11	DATA_SGPIOD13	DATA_SGPIOD15	DATA_SGPIOD17	IRQ3_B_RSV_B_VF2_IWP3	BB_B_VF2_IWP3	RD_WR_B	OE_B	WE_B_AT0	CS0_B	BURST_B	TS_B	BDIP_B	NC	VDD	VSS	QVDDL	VDDSN	AE		
AF	VSS	VDD	DATA_SGPIOD0	DATA_SGPIOD2	DATA_SGPIOD4	DATA_SGPIOD6	DATA_SGPIOD8	DATA_SGPIOD10	DATA_SGPIOD12	DATA_SGPIOD14	DATA_SGPIOD16	DATA_SGPIOD18	IRQ1_B_RSV_B_VF0_LWP1	BG_B_VF0_LWP1	BR_B_VF1_IWP2	IRQ0_B_SGPIOC0	WE_B_AT3	CS2_B	TSIZ1	TA_B	EPEE	ENGCLK_BUCK	NC	VDD	VSS	QVDDL	AF		
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26			

NOTE: This is a top down view of the balls.

VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS	VSS	VSS

Figure 4. MPC535 Pinout Diagram



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