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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: [info@chipsmall.com](mailto:info@chipsmall.com) Web: [www.chipsmall.com](http://www.chipsmall.com)

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# MPC5553

# Microcontroller Data Sheet

by: Microcontroller Division

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5553 microcontroller device. For functional characteristics, refer to the *MPC5553/MPC5554 Microcontroller Reference Manual*.

## 1 Overview

The MPC5553 microcontroller (MCU) is a member of the MPC5500 family of microcontrollers built on the Power Architecture<sup>®</sup> embedded technology. This family of parts has many new features coupled with high performance CMOS technology to provide substantial reduction of cost per feature and significant performance improvement over the MPC500 family.

The host processor core of this device complies with the Power Architecture embedded category that is 100% user-mode compatible (including floating point library) with the original PowerPC instruction set. The embedded architecture enhancements improve the performance in embedded applications. The core also has additional instructions, including digital signal processing (DSP) instructions, beyond the original PowerPC instruction set.

## Contents

1	Overview .....	1
2	Ordering Information .....	3
3	Electrical Characteristics .....	4
3.1	Maximum Ratings .....	4
3.2	Thermal Characteristics .....	6
3.3	Package .....	9
3.4	EMI (Electromagnetic Interference) Characteristics .....	9
3.5	ESD (Electromagnetic Static Discharge) Characteristics .....	10
3.6	Voltage Regulator Controller (VRC) and Power-On Reset (POR) Electrical Specifications .....	10
3.7	Power-Up/Down Sequencing .....	11
3.8	DC Electrical Specifications .....	15
3.9	Oscillator and FMPLL Electrical Characteristics ..	21
3.10	eQADC Electrical Characteristics .....	23
3.11	H7Fa Flash Memory Electrical Characteristics ..	24
3.12	AC Specifications .....	25
3.13	AC Timing .....	27
3.14	Fast Ethernet AC Timing Specifications .....	46
4	Mechanicals .....	50
4.1	MPC5553 208 MAP BGA Pinout .....	50
4.2	MPC5553 324 PBGA Pinouts .....	51
4.3	MPC5553 416 PBGA Pinout .....	51
4.4	MPC5553 208-Pin Package Dimensions .....	55
4.5	MPC5553 324-Pin Package Dimensions .....	57
4.6	MPC5553 416-Pin Package Dimensions .....	59
5	Revision History for the MPC5553 Data Sheet .....	61
5.1	Information Changed Between Revisions 3.0 and 4.0 .....	61
5.2	Information Changed Between Revisions 2.0 and 3.0 .....	61



## Overview

The MPC5500 family of parts contains many new features coupled with high performance CMOS technology to provide significant performance improvement over the MPC565.

The MPC5553 has two levels of memory hierarchy. The fastest accesses are to the 8-kilobytes (KB) unified cache. The next level in the hierarchy contains the 64-KB on-chip internal SRAM and 1.5-megabytes (MB) internal flash memory. The internal SRAM and flash memory hold instructions and data. The external bus interface is designed to support most of the standard memories used with the MPC5xx family.

The complex input/output timer functions of the MPC5553 are performed by an enhanced time processor unit (eTPU) engine. The eTPU engine controls 32 hardware channels. The eTPU has been enhanced over the TPU by providing: 24-bit timers, double-action hardware channels, variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. The eTPU is programmed using a high-level programming language.

The less complex timer functions of the MPC5553 are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single-action, double-action, pulse-width modulation (PWM), and modulus-counter operations. Motor control capabilities include edge-aligned and center-aligned PWM.

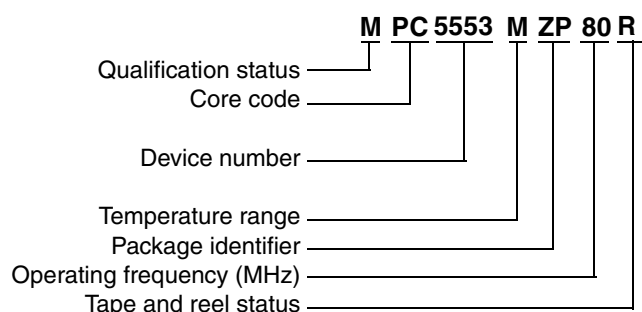
Off-chip communication is performed by a suite of serial protocols including controller area networks (FlexCANs), enhanced deserial/serial peripheral interfaces (DSPIs), and enhanced serial communications interfaces (eSCIs).

The MCU has an on-chip enhanced queued dual analog-to-digital converter (eQADC). The 324 and 416 packages have 40-channels.

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also determined by the SIU. The internal multiplexer submodule (SIU\_DISR) provides multiplexing of eQADC trigger sources and external interrupt signal multiplexing.

The Fast Ethernet (FEC) module is a RISC-based controller that supports both 10 and 100 Mbps Ethernet/IEEE® 802.3 networks and is compatible with three different standard MAC (media access controller) PHY (physical) interfaces to connect to an external Ethernet bus. The FEC supports the 10 or 100 Mbps MII (media independent interface), and the 10 Mbps-only with a seven-wire interface, which uses a subset of the MII signals. The upper 16-bits of the 32-bit external bus interface (EBI) are used to connect to an external Ethernet device. The FEC contains built-in transmit and receive message FIFOs and DMA support.

## 2 Ordering Information



**Temperature Range**  
M = -40° C to 125° C

**Package Identifier**  
ZP = 416PBGA SnPb  
VR = 416PBGA Pb-free  
VF = 208MAPBGA SnPb  
VM = 208MAPBGA Pb-free  
ZQ = 324PBGA SnPb  
VZ = 324PBGA Pb-free

**Operating Frequency**  
80 = 80 MHz  
112 = 112 MHz  
132 = 132 MHz

**Tape and Reel Status**  
R = Tape and reel  
(blank) = Trays

**Qualification Status**  
P = Pre qualification  
M = Fully spec. qualified, general market flow  
S = Fully spec. qualified, automotive flow

**Note:** Not all options are available on all devices. Refer to [Table 1](#).

**Figure 1. MPC5500 Family Part Number Example**

Unless noted in this data sheet, all specifications apply from  $T_L$  to  $T_H$ .

**Table 1. Orderable Part Numbers**

Freescale Part Number <sup>1</sup>	Package Description	Speed (MHz)		Operating Temperature <sup>2</sup>	
		Nominal	Max. <sup>3</sup> ( $f_{MAX}$ )	Min. ( $T_L$ )	Max. ( $T_H$ )
MPC5553MVR132	MPC5553 416 package Lead-free (Pb-free)	132	132	-40° C	125° C
MPC5553MVR112		112	114		
MPC5553MVR80		80	82		
MPC5553MVZ132	MPC5553 324 package Lead-free (Pb-free)	132	132	-40° C	125° C
MPC5553MVZ112		112	114		
MPC5553MVZ80		80	82		
MPC5553MVM132	MPC5553 208 package Lead-free (Pb-free)	132	132	-40° C	125° C
MPC5553MVM112		112	114		
MPC5553MVM80		80	82		
MPC5553MZP132	MPC5553 416 package Leaded (SnPb)	132	132	-40° C	125° C
MPC5553MZP112		112	114		
MPC5553MZP80		80	82		
MPC5553MZQ132	MPC5553 324 package Leaded (SnPb)	132	132	-40° C	125° C
MPC5553MZQ112		112	114		
MPC5553MZQ80		80	82		

Table 1. Orderable Part Numbers (continued)

Freescale Part Number <sup>1</sup>	Package Description	Speed (MHz)		Operating Temperature <sup>2</sup>	
		Nominal	Max. <sup>3</sup> (f <sub>MAX</sub> )	Min. (T <sub>L</sub> )	Max. (T <sub>H</sub> )
MPC5553MVF132	MPC5553 208 package Leaded (SnPb)	132	132	−40° C	125° C
MPC5553MVF112		112	114		
MPC5553MVF80		80	82		

<sup>1</sup> All devices are PPC5553, rather than MPC5553 or SPC5553, until product qualifications are complete. Not all configurations are available in the PPC parts.

<sup>2</sup> The lowest ambient operating temperature is referenced by T<sub>L</sub>; the highest ambient operating temperature is referenced by T<sub>H</sub>.

<sup>3</sup> Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM.

## 3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

### 3.1 Maximum Ratings

Table 2. Absolute Maximum Ratings<sup>1</sup>

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	1.5 V core supply voltage <sup>2</sup>	V <sub>DD</sub>	−0.3	1.7	V
2	Flash program/erase voltage	V <sub>PP</sub>	−0.3	6.5	V
4	Flash read voltage	V <sub>FLASH</sub>	−0.3	4.6	V
5	SRAM standby voltage	V <sub>STBY</sub>	−0.3	1.7	V
6	Clock synthesizer voltage	V <sub>DDSYN</sub>	−0.3	4.6	V
7	3.3 V I/O buffer voltage	V <sub>DD33</sub>	−0.3	4.6	V
8	Voltage regulator control input voltage	V <sub>RC33</sub>	−0.3	4.6	V
9	Analog supply voltage (reference to V <sub>SSA</sub> )	V <sub>DDA</sub>	−0.3	5.5	V
10	I/O supply voltage (fast I/O pads) <sup>3</sup>	V <sub>DDE</sub>	−0.3	4.6	V
11	I/O supply voltage (slow and medium I/O pads) <sup>3</sup>	V <sub>DDEH</sub>	−0.3	6.5	V
12	DC input voltage <sup>4</sup> V <sub>DDEH</sub> powered I/O pads V <sub>DDE</sub> powered I/O pads	V <sub>IN</sub>	−1.0 <sup>5</sup> −1.0 <sup>5</sup>	6.5 <sup>6</sup> 4.6 <sup>7</sup>	V
13	Analog reference high voltage (reference to V <sub>RL</sub> )	V <sub>RH</sub>	−0.3	5.5	V
14	V <sub>SS</sub> to V <sub>SSA</sub> differential voltage	V <sub>SS</sub> − V <sub>SSA</sub>	−0.1	0.1	V
15	V <sub>DD</sub> to V <sub>DDA</sub> differential voltage	V <sub>DD</sub> − V <sub>DDA</sub>	−V <sub>DDA</sub>	V <sub>DD</sub>	V
16	V <sub>REF</sub> differential voltage	V <sub>RH</sub> − V <sub>RL</sub>	−0.3	5.5	V
17	V <sub>RH</sub> to V <sub>DDA</sub> differential voltage	V <sub>RH</sub> − V <sub>DDA</sub>	−5.5	5.5	V
18	V <sub>RL</sub> to V <sub>SSA</sub> differential voltage	V <sub>RL</sub> − V <sub>SSA</sub>	−0.3	0.3	V

Table 2. Absolute Maximum Ratings <sup>1</sup> (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
19	V <sub>DDEH</sub> to V <sub>DDA</sub> differential voltage	V <sub>DDEH</sub> – V <sub>DDA</sub>	–V <sub>DDA</sub>	V <sub>DDEH</sub>	V
20	V <sub>DDF</sub> to V <sub>DD</sub> differential voltage	V <sub>DDF</sub> – V <sub>DD</sub>	–0.3	0.3	V
21	V <sub>RC33</sub> to V <sub>DDSYN</sub> differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a.				
22	V <sub>SSSYN</sub> to V <sub>SS</sub> differential voltage	V <sub>SSSYN</sub> – V <sub>SS</sub>	–0.1	0.1	V
23	V <sub>RCVSS</sub> to V <sub>SS</sub> differential voltage	V <sub>RCVSS</sub> – V <sub>SS</sub>	–0.1	0.1	V
24	Maximum DC digital input current <sup>8</sup> (per pin, applies to all digital pins) <sup>4</sup>	I <sub>MAXD</sub>	–2	2	mA
25	Maximum DC analog input current <sup>9</sup> (per pin, applies to all analog pins)	I <sub>MAXA</sub>	–3	3	mA
26	Maximum operating temperature range <sup>10</sup> Die junction temperature	T <sub>J</sub>	T <sub>L</sub>	150.0	°C
27	Storage temperature range	T <sub>STG</sub>	–55.0	150.0	°C
28	Maximum solder temperature <sup>11</sup> Lead free (Pb-free) Leaded (SnPb)	T <sub>SDR</sub>	— —	260.0 245.0	°C
29	Moisture sensitivity level <sup>12</sup>	MSL	—	3	

<sup>1</sup> Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond any of the listed maxima can affect device reliability or cause permanent damage to the device.

<sup>2</sup> 1.5 V ± 10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

<sup>3</sup> All functional non-supply I/O pins are clamped to V<sub>SS</sub> and V<sub>DDE</sub>, or V<sub>DDEH</sub>.

<sup>4</sup> AC signal overshoot and undershoot of up to ± 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

<sup>5</sup> Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than –0.6 V on SINB during the internal power-on reset (POR) state.

<sup>6</sup> Internal structures hold the input voltage less than the maximum voltage on all pads powered by V<sub>DDEH</sub> supplies, if the maximum injection current specification is met (2 mA for all pins) and V<sub>DDEH</sub> is within the operating voltage specifications.

<sup>7</sup> Internal structures hold the input voltage less than the maximum voltage on all pads powered by V<sub>DDE</sub> supplies, if the maximum injection current specification is met (2 mA for all pins) and V<sub>DDE</sub> is within the operating voltage specifications.

<sup>8</sup> Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

<sup>9</sup> Total injection current for all analog input pins must not exceed 15 mA.

<sup>10</sup> Lifetime operation at these specification limits is not guaranteed.

<sup>11</sup> Moisture sensitivity profile per IPC/JEDEC J-STD-020D.

<sup>12</sup> Moisture sensitivity per JEDEC test method A112.

## 3.2 Thermal Characteristics

The shaded rows in the following table indicate information specific to a four-layer board.

**Table 3. MPC5553 Thermal Characteristics**

Spec	MPC5553 Thermal Characteristic	Symbol	Packages			Unit
			208 MAPBGA	324 PBGA	416 PBGA	
1	Junction to ambient, natural convection (one-layer board) <sup>1, 2</sup>	$R_{\theta JA}$	41	30	29	°C/W
2	Junction to ambient, natural convection <sup>1, 3</sup> (four-layer board 2s2p)	$R_{\theta JA}$	25	21	21	°C/W
3	Junction to ambient (@200 ft./min., one-layer board)	$R_{\theta JMA}$	33	24	23	°C/W
4	Junction to ambient (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	22	17	18	°C/W
5	Junction to board (four-layer board 2s2p) <sup>4</sup>	$R_{\theta JB}$	15	12	13	°C/W
6	Junction to case <sup>5</sup>	$R_{\theta JC}$	7	8	9	°C/W
7	Junction to package top, natural convection <sup>6</sup>	$\Psi_{JT}$	2	2	2	°C/W

<sup>1</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

<sup>2</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

<sup>3</sup> Per JEDEC JESD51-6 with the board horizontal.

<sup>4</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>5</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

<sup>6</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

### 3.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the device junction temperature,  $T_J$ , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$  = ambient temperature for the package (°C)

$R_{\theta JA}$  = junction to ambient thermal resistance (°C/W)

$P_D$  = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes

- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than  $0.02 \text{ W/cm}^2$

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.



## Electrical Characteristics

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$T_J$  = junction temperature ( $^{\circ}\text{C}$ )

$T_B$  = board temperature at the package perimeter ( $^{\circ}\text{C/W}$ )

$R_{\theta JB}$  = junction-to-board thermal resistance ( $^{\circ}\text{C/W}$ ) per JESD51-8

$P_D$  = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$  = junction-to-ambient thermal resistance ( $^{\circ}\text{C/W}$ )

$R_{\theta JC}$  = junction-to-case thermal resistance ( $^{\circ}\text{C/W}$ )

$R_{\theta CA}$  = case-to-ambient thermal resistance ( $^{\circ}\text{C/W}$ )

$R_{\theta JC}$  is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter ( $\Psi_{JT}$ ) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_T$  = thermocouple temperature on top of the package ( $^{\circ}\text{C}$ )

$\Psi_{JT}$  = thermal characterization parameter ( $^{\circ}\text{C/W}$ )

$P_D$  = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

## References:

Semiconductor Equipment and Materials International  
3081 Zanker Rd.  
San Jose, CA., 95134  
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at <http://www.jedec.org>.

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, "Thermal Modeling of a PBGA for Air-Cooled Applications," Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

## 3.3 Package

The MPC5553 is available in packaged form. Read the package options in [Section 2, "Ordering Information."](#) Refer to [Section 4, "Mechanicals,"](#) for pinouts and package drawings.

## 3.4 EMI (Electromagnetic Interference) Characteristics

Table 4. EMI Testing Specifications <sup>1</sup>

Spec	Characteristic	Minimum	Typical	Maximum	Unit
1	Scan range	0.15	—	1000	MHz
2	Operating frequency	—	—	f <sub>MAX</sub>	MHz
3	V <sub>DD</sub> operating voltages	—	1.5	—	V
4	V <sub>DDSYN</sub> , V <sub>RC33</sub> , V <sub>DD33</sub> , V <sub>FLASH</sub> , V <sub>DDE</sub> operating voltages	—	3.3	—	V
5	V <sub>PP</sub> , V <sub>DDEH</sub> , V <sub>DDA</sub> operating voltages	—	5.0	—	V
6	Maximum amplitude	—	—	14 <sup>2</sup> 32 <sup>3</sup>	dBuV
7	Operating temperature	—	—	25	°C

<sup>1</sup> EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03. Qualification testing was performed on the MPC5554 and applied to the MPC5500 family as generic EMI performance data.

<sup>2</sup> Measured with the single-chip EMI program.

<sup>3</sup> Measured with the expanded EMI program.

## 3.5 ESD (Electromagnetic Static Discharge) Characteristics

Table 5. ESD Ratings <sup>1, 2</sup>

Characteristic	Symbol	Value	Unit
ESD for human body model (HBM)		2000	V
HBM circuit description	R1	1500	$\Omega$
	C	100	pF
ESD for field induced charge model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of pulses per pin:			
Positive pulses (HBM)	—	1	—
Negative pulses (HBM)	—	1	—
Interval of pulses	—	1	second

<sup>1</sup> All ESD testing conforms to CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

<sup>2</sup> Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.

## 3.6 Voltage Regulator Controller ( $V_{RC}$ ) and Power-On Reset (POR) Electrical Specifications

The following table lists the  $V_{RC}$  and POR electrical specifications:

Table 6.  $V_{RC}$  and POR Electrical Specifications

Spec	Characteristic		Symbol	Min.	Max.	Units
1	1.5 V ( $V_{DD}$ ) POR <sup>1</sup>	Negated (ramp up) Asserted (ramp down)	$V_{POR15}$	1.1 1.1	1.35 1.35	V
2	3.3 V ( $V_{DDSYN}$ ) POR <sup>1</sup>	Asserted (ramp up) Negated (ramp up) Asserted (ramp down) Negated (ramp down)	$V_{POR33}$	0.0 2.0 2.0 0.0	0.30 2.85 2.85 0.30	V
3	$\overline{RESET}$ pin supply ( $V_{DDEH6}$ ) POR <sup>1, 2</sup>	Negated (ramp up) Asserted (ramp down)	$V_{POR5}$	2.0 2.0	2.85 2.85	V
4	$V_{RC33}$ voltage	Before $V_{RC}$ allows the pass transistor to start turning on	$V_{TRANS\_START}$	1.0	2.0	V
5		When $V_{RC}$ allows the pass transistor to completely turn on <sup>3, 4</sup>	$V_{TRANS\_ON}$	2.0	2.85	V
6		When the voltage is greater than the voltage at which the $V_{RC}$ keeps the 1.5 V supply in regulation <sup>5, 6</sup>	$V_{VRC33REG}$	3.0	—	V
7	Current can be sourced by $V_{RCCTL}$ at $T_j$ :	−40° C 25° C 150° C	$I_{VRCCTL}$ <sup>7</sup>	11.0 9.0 7.5	— — —	mA mA mA
8	Voltage differential during power up such that: $V_{DD33}$ can lag $V_{DDSYN}$ or $V_{DDEH6}$ before $V_{DDSYN}$ and $V_{DDEH6}$ reach the $V_{POR33}$ and $V_{POR5}$ minimums respectively.		$V_{DD33\_LAG}$	—	1.0	V

Table 6.  $V_{RC}$  and POR Electrical Specifications (continued)

Spec	Characteristic	Symbol	Min.	Max.	Units
9	Absolute value of slew rate on power supply pins	—	—	50	V/ms
10	Required gain at Tj: $I_{DD} \div I_{VRCCTL}$ (@ $f_{sys} = f_{MAX}$ ) 6, 7, 8, 9	BETA <sup>10</sup>	40 45 55	— — 500	— — —

<sup>1</sup> The internal POR signals are  $V_{POR15}$ ,  $V_{POR33}$ , and  $V_{POR5}$ . On power up, assert  $\overline{RESET}$  before the internal POR negates.  $\overline{RESET}$  must remain asserted until the power supplies are within the operating conditions as specified in Table 9 DC Electrical Specifications. On power down, assert  $\overline{RESET}$  before any power supplies fall outside the operating conditions and until the internal POR asserts.

<sup>2</sup>  $V_{IL\_S}$  (Table 9, Spec15) is guaranteed to scale with  $V_{DDEH6}$  down to  $V_{POR5}$ .

<sup>3</sup> Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range.

<sup>4</sup> It is possible to reach the current limit during ramp up—do not treat this event as short circuit current.

<sup>5</sup> At peak current for device.

<sup>6</sup> Requires compliance with Freescale's recommended board requirements and transistor recommendations. Board signal traces/routing from the  $V_{RCCTL}$  package signal to the base of the external pass transistor and between the emitter of the pass transistor to the  $V_{DD}$  package signals must have a maximum of 100 nH inductance and minimal resistance (less than 1  $\Omega$ ).  $V_{RCCTL}$  must have a nominal 1  $\mu F$  phase compensation capacitor to ground.  $V_{DD}$  must have a 20  $\mu F$  (nominal) bulk capacitor (greater than 4  $\mu F$  over all conditions, including lifetime). Place high-frequency bypass capacitors consisting of eight 0.01  $\mu F$ , two 0.1  $\mu F$ , and one 1  $\mu F$  capacitors around the package on the  $V_{DD}$  supply signals.

<sup>7</sup>  $I_{VRCCTL}$  is measured at the following conditions:  $V_{DD} = 1.35$  V,  $V_{RC33} = 3.1$  V,  $V_{VRCCTL} = 2.2$  V.

<sup>8</sup> Refer to Table 1 for the maximum operating frequency.

<sup>9</sup> Values are based on  $I_{DD}$  from high-use applications as explained in the  $I_{DD}$  Electrical Specification.

<sup>10</sup> BETA is the worst-case external transistor BETA. It is measured on a per-part basis and calculated as  $(I_{DD} \div I_{VRCCTL})$ .

## 3.7 Power-Up/Down Sequencing

Power sequencing between the 1.5 V power supply and  $V_{DDSYN}$  or the  $\overline{RESET}$  power supplies is required if using an external 1.5 V power supply with  $V_{RC33}$  tied to ground (GND). To avoid power-sequencing,  $V_{RC33}$  must be powered up within the specified operating range, even if the on-chip voltage regulator controller is not used. Refer to Section 3.7.2, “Power-Up Sequence (VRC33 Grounded),” and Section 3.7.3, “Power-Down Sequence (VRC33 Grounded).”

Power sequencing requires that  $V_{DD33}$  must reach a certain voltage where the values are read as ones before the POR signal negates. Refer to Section 3.7.1, “Input Value of Pins During POR Dependent on VDD33.”

Although power sequencing is not required between  $V_{RC33}$  and  $V_{DDSYN}$  during power up,  $V_{RC33}$  must not lead  $V_{DDSYN}$  by more than 600 mV or lag by more than 100 mV for the  $V_{RC}$  stage turn-on to operate within specification. Higher spikes in the emitter current of the pass transistor occur if  $V_{RC33}$  leads or lags  $V_{DDSYN}$  by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock starts to toggle, adding another large increase of the current consumed by  $V_{RC33}$ . If  $V_{RC33}$  lags  $V_{DDSYN}$  by more than 100 mV, the increase in current consumed can drop  $V_{DD}$  low enough to assert the 1.5 V POR again. Oscillations are possible when the 1.5 V POR asserts and stops the system clock, causing the voltage on  $V_{DD}$  to rise until the 1.5 V POR negates again. All oscillations stop when  $V_{RC33}$  is powered sufficiently.

## Electrical Characteristics

When powering down,  $V_{RC33}$  and  $V_{DDSYN}$  have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between  $V_{RC33}$  and  $V_{DDSYN}$  is required for the  $V_{RC}$  to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad\_fc (fast type).

**Table 7. Pin Status for Fast Pads During the Power Sequence**

$V_{DDE}$	$V_{DD33}$	$V_{DD}$	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
$V_{DDE}$	Low	Low	Asserted	High
$V_{DDE}$	Low	$V_{DD}$	Asserted	High
$V_{DDE}$	$V_{DD33}$	Low	Asserted	High impedance (Hi-Z)
$V_{DDE}$	$V_{DD33}$	$V_{DD}$	Asserted	Hi-Z
$V_{DDE}$	$V_{DD33}$	$V_{DD}$	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad\_mh (medium type) and pad\_sh (slow type).

**Table 8. Pin Status for Medium and Slow Pads During the Power Sequence**

$V_{DDEH}$	$V_{DD}$	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
$V_{DDEH}$	Low	Asserted	High impedance (Hi-Z)
$V_{DDEH}$	$V_{DD}$	Asserted	Hi-Z
$V_{DDEH}$	$V_{DD}$	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices

(up or down) are enabled as defined in the device reference manual. If  $V_{DD}$  is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to  $V_{DDE}$  and  $V_{DDEH}$ .

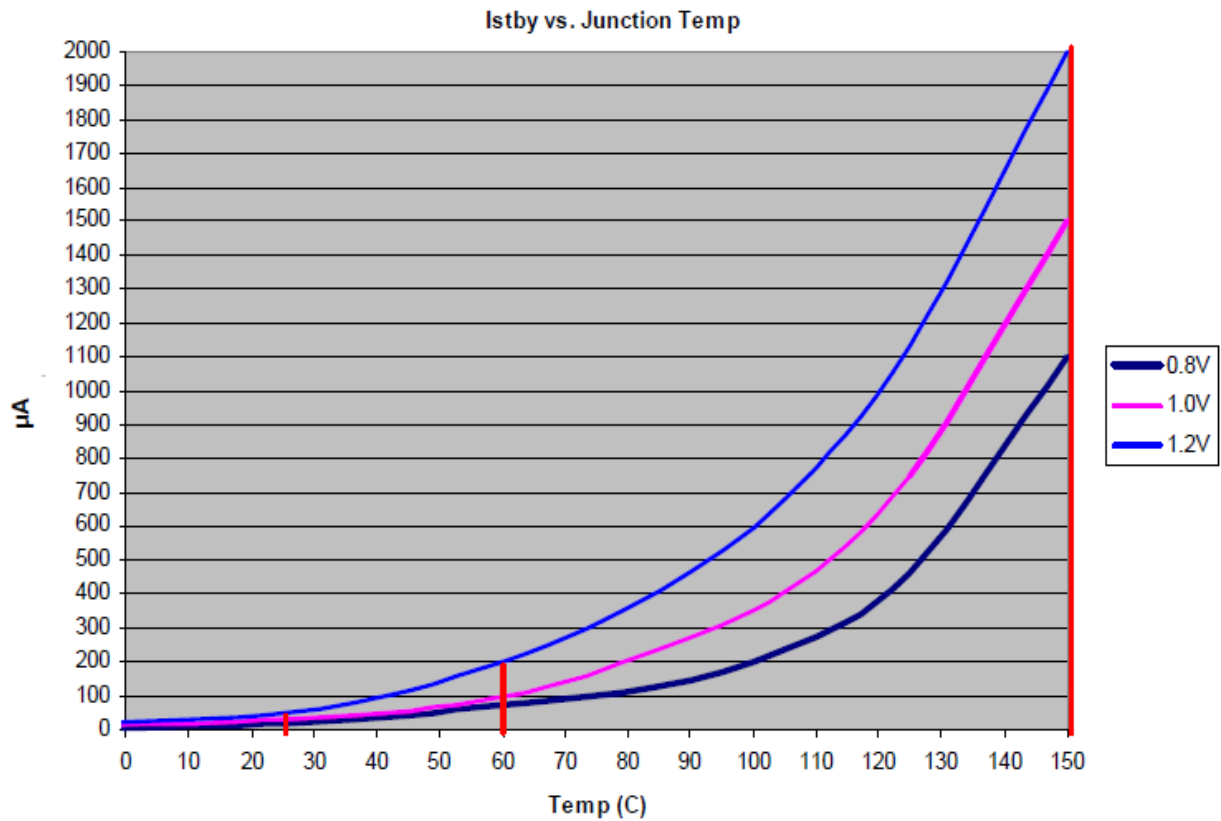
To avoid this condition, minimize the ramp time of the  $V_{DD}$  supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

During initial power ramp-up, when  $V_{stby}$  is 0.6v or above, a typical current of 1-3mA and maximum of 4mA may be seen until  $V_{DD}$  is applied. This current will not reoccur until  $V_{stby}$  is lowered below  $V_{stby}$  min. specification.



Figure 2 shows an approximate interpolation of the  $I_{STBY}$  worst-case specification to estimate values at different voltages and temperatures. The vertical lines shown at 25 °C, 60 °C, and 150 °C in Figure 2 are the actual  $I_{DD\_STBY}$  specifications (27d) listed in Table 9.

Figure 2. fISTBY Worst-case Specifications



### 3.7.1 Input Value of Pins During POR Dependent on $V_{DD33}$

When powering up the device,  $V_{DD33}$  must not lag the latest  $V_{DDSYN}$  or  $\overline{RESET}$  power pin ( $V_{DDEH6}$ ) by more than the  $V_{DD33}$  lag specification listed in Table 6, spec 8. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and  $\overline{RSTCFG}$  are not powered and therefore cannot read the default state when POR negates.  $V_{DD33}$  can lag  $V_{DDSYN}$  or the  $\overline{RESET}$  power pin ( $V_{DDEH6}$ ), but cannot lag both by more than the  $V_{DD33}$  lag specification. This  $V_{DD33}$  lag specification applies during power up only.  $V_{DD33}$  has no lead or lag requirements when powering down.

### 3.7.2 Power-Up Sequence ( $V_{RC33}$ Grounded)

The 1.5 V  $V_{DD}$  power supply must rise to 1.35 V before the 3.3 V  $V_{DDSYN}$  power supply and the  $\overline{RESET}$  power supply rises above 2.0 V. This ensures that digital logic in the PLL for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. Because the internal 1.5 V POR is disabled, the internal 3.3 V POR or the  $\overline{RESET}$  power POR must hold the device in reset. Since they can negate as low as 2.0 V,  $V_{DD}$  must be within specification before the 3.3 V POR and the  $\overline{RESET}$  POR negate.

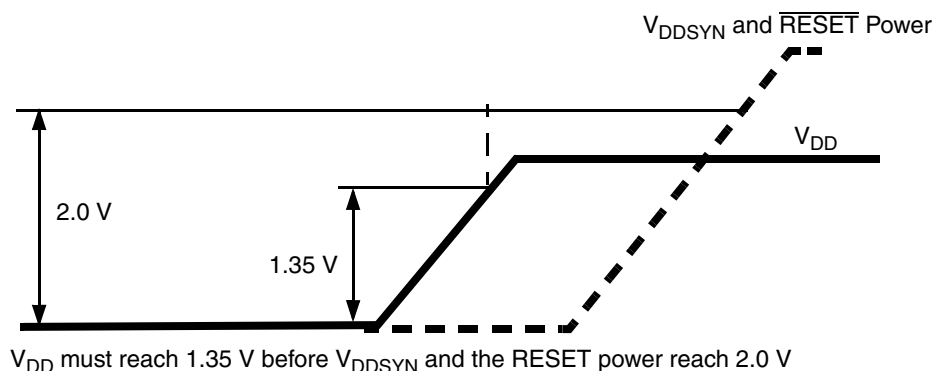


Figure 3. Power-Up Sequence ( $V_{RC33}$  Grounded)

### 3.7.3 Power-Down Sequence ( $V_{RC33}$ Grounded)

The only requirement for the power-down sequence with  $V_{RC33}$  grounded is if  $V_{DD}$  decreases to less than its operating range,  $V_{DDSYN}$  or the  $\overline{RESET}$  power must decrease to less than 2.0 V before the  $V_{DD}$  power increases to its operating range. This ensures that the digital 1.5 V logic, which is reset only by an ORed POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly. See Table 6, footnote 1.

## 3.8 DC Electrical Specifications

Table 9. DC Electrical Specifications ( $T_A = T_L$  to  $T_H$ )

Spec	Characteristic	Symbol	Min	Max.	Unit
1	Core supply voltage (average DC RMS voltage)	$V_{DD}$	1.35	1.65	V
2	Input/output supply voltage (fast input/output) <sup>1</sup>	$V_{DDE}$	1.62	3.6	V
3	Input/output supply voltage (slow and medium input/output)	$V_{DDEH}$	3.0	5.25	V
4	3.3 V input/output buffer voltage	$V_{DD33}$	3.0	3.6	V
5	Voltage regulator control input voltage	$V_{RC33}$	3.0	3.6	V
6	Analog supply voltage <sup>2</sup>	$V_{DDA}$	4.5	5.25	V
8	Flash programming voltage <sup>3</sup>	$V_{PP}$	4.5	5.25	V
9	Flash read voltage	$V_{FLASH}$	3.0	3.6	V
10	SRAM standby voltage <sup>4</sup>	$V_{STBY}$	0.8	1.2	V
11	Clock synthesizer operating voltage	$V_{DDSYN}$	3.0	3.6	V
12	Fast I/O input high voltage	$V_{IH\_F}$	$0.65 \times V_{DDE}$	$V_{DDE} + 0.3$	V
13	Fast I/O input low voltage	$V_{IL\_F}$	$V_{SS} - 0.3$	$0.35 \times V_{DDE}$	V
14	Medium and slow I/O input high voltage	$V_{IH\_S}$	$0.65 \times V_{DDEH}$	$V_{DDEH} + 0.3$	V
15	Medium and slow I/O input low voltage	$V_{IL\_S}$	$V_{SS} - 0.3$	$0.35 \times V_{DDEH}$	V
16	Fast input hysteresis	$V_{HYS\_F}$	$0.1 \times V_{DDE}$		V
17	Medium and slow I/O input hysteresis	$V_{HYS\_S}$	$0.1 \times V_{DDEH}$		V
18	Analog input voltage	$V_{INDC}$	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$	V
19	Fast output high voltage ( $I_{OH\_F} = -2.0$ mA)	$V_{OH\_F}$	$0.8 \times V_{DDE}$	—	V
20	Slow and medium output high voltage $I_{OH\_S} = -2.0$ mA $I_{OH\_S} = -1.0$ mA	$V_{OH\_S}$	$0.80 \times V_{DDEH}$ $0.85 \times V_{DDEH}$	—	V
21	Fast output low voltage ( $I_{OL\_F} = 2.0$ mA)	$V_{OL\_F}$	—	$0.2 \times V_{DDE}$	V
22	Slow and medium output low voltage $I_{OL\_S} = 2.0$ mA $I_{OL\_S} = 1.0$ mA	$V_{OL\_S}$	—	$0.20 \times V_{DDEH}$ $0.15 \times V_{DDEH}$	V
23	Load capacitance (fast I/O) <sup>5</sup> DSC (SIU_PCR[8:9]) = 0b00 = 0b01 = 0b10 = 0b11	$C_L$	— — — —	10 20 30 50	pF pF pF pF
24	Input capacitance (digital pins)	$C_{IN}$	—	7	pF
25	Input capacitance (analog pins)	$C_{IN\_A}$	—	10	pF
26	Input capacitance: (Shared digital and analog pins AN[12]_MA[0]_SDS, AN[13]_MA[1]_SDO, AN[14]_MA[2]_SDI, and AN[15]_FCK)	$C_{IN\_M}$	—	12	pF

**Table 9. DC Electrical Specifications ( $T_A = T_L$  to  $T_H$ ) (continued)**

Spec	Characteristic	Symbol	Min	Max.	Unit
27a	Operating current 1.5 V supplies @ 132 MHz: <sup>6</sup>				
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.65 V typical use <sup>7, 8</sup>	$I_{DD}$	—	460	mA
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.35 V typical use <sup>7, 8</sup>	$I_{DD}$	—	360	mA
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.65 V high use <sup>8, 9</sup>	$I_{DD}$	—	510	mA
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.35 V high use <sup>8, 9</sup>	$I_{DD}$	—	410	mA
27b	Operating current 1.5 V supplies @ 114 MHz: <sup>6</sup>				
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.65 V typical use <sup>7, 8</sup>	$I_{DD}$	—	410	mA
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.35 V typical use <sup>7, 8</sup>	$I_{DD}$	—	310	mA
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.65 V high use <sup>8, 9</sup>	$I_{DD}$	—	460	mA
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.35 V high use <sup>8, 9</sup>	$I_{DD}$	—	370	mA
27c	Operating current 1.5 V supplies @ 82 MHz: <sup>6</sup>				
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.65 V typical use <sup>7, 8</sup>	$I_{DD}$	—	330	mA
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.35 V typical use <sup>7, 8</sup>	$I_{DD}$	—	225	mA
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.65 V high use <sup>8, 9</sup>	$I_{DD}$	—	385	mA
	$V_{DD}$ (including $V_{DDF}$ max current) @ 1.35 V high use <sup>8, 9</sup>	$I_{DD}$	—	290	mA
27d	RAM standby current. <sup>10</sup>				
	$I_{DD\_STBY}$ @ 25° C	$I_{DD\_STBY}$	—	20	μA
	$V_{STBY}$ @ 0.8 V	$I_{DD\_STBY}$	—	30	μA
	$V_{STBY}$ @ 1.0 V	$I_{DD\_STBY}$	—	50	μA
	$V_{STBY}$ @ 1.2 V	$I_{DD\_STBY}$	—		
	$I_{DD\_STBY}$ @ 60° C	$I_{DD\_STBY}$	—	70	μA
	$V_{STBY}$ @ 0.8 V	$I_{DD\_STBY}$	—	100	μA
	$V_{STBY}$ @ 1.0 V	$I_{DD\_STBY}$	—	200	μA
	$V_{STBY}$ @ 1.2 V	$I_{DD\_STBY}$	—		
	$I_{DD\_STBY}$ @ 150° C (Tj)	$I_{DD\_STBY}$	—	1200	μA
	$V_{STBY}$ @ 0.8 V	$I_{DD\_STBY}$	—	1500	μA
	$V_{STBY}$ @ 1.0 V	$I_{DD\_STBY}$	—	2000	μA
	$V_{STBY}$ @ 1.2 V	$I_{DD\_STBY}$	—		
28	Operating current 3.3 V supplies @ $f_{MAX}$ MHz				
	$V_{DD33}$ <sup>11</sup>	$I_{DD\_33}$	—	2 + (values derived from procedure of footnote <sup>11</sup> )	mA
	$V_{FLASH}$	$I_{VFLASH}$	—	10	mA
	$V_{DDSYN}$	$I_{DDSYN}$	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK):				
	$V_{DDA}$ ( $V_{DDA0} + V_{DDA1}$ )	$I_{DD\_A}$	—	20.0	mA
	Analog reference supply current ( $V_{RH}$ , $V_{RL}$ )	$I_{REF}$	—	1.0	mA
	$V_{PP}$	$I_{PP}$	—	25.0	mA

Table 9. DC Electrical Specifications ( $T_A = T_L$  to  $T_H$ ) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
30	Operating current $V_{DDE}$ supplies: <sup>12</sup> $V_{DDEH1}$ $V_{DDE2}$ $V_{DDE3}$ $V_{DDEH4}$ $V_{DDE5}$ $V_{DDEH6}$ $V_{DDE7}$ $V_{DDEH8}$ $V_{DDEH9}$	$I_{DD1}$ $I_{DD2}$ $I_{DD3}$ $I_{DD4}$ $I_{DD5}$ $I_{DD6}$ $I_{DD7}$ $I_{DD8}$ $I_{DD9}$	— — — — — — — —	Refer to footnote <sup>12</sup>	mA mA mA mA mA mA mA mA mA
31	Fast I/O weak pullup current <sup>13</sup> 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V	$I_{ACT\_F}$	10 20 20	110 130 170	$\mu$ A $\mu$ A $\mu$ A
	Fast I/O weak pulldown current <sup>13</sup> 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V		10 20 20	100 130 170	$\mu$ A $\mu$ A $\mu$ A
32	Slow and medium I/O weak pullup/down current <sup>13</sup> 3.0–3.6 V 4.5–5.5 V	$I_{ACT\_S}$	10 20	150 170	$\mu$ A $\mu$ A
33	I/O input leakage current <sup>14</sup>	$I_{INACT\_D}$	–2.5	2.5	$\mu$ A
34	DC injection current (per pin)	$I_{IC}$	–2.0	2.0	mA
35	Analog input current, channel off <sup>15</sup>	$I_{INACT\_A}$	–150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	$I_{INACT\_AD}$	–2.5	2.5	$\mu$ A
36	$V_{SS}$ to $V_{SSA}$ differential voltage <sup>16</sup>	$V_{SS} - V_{SSA}$	–100	100	mV
37	Analog reference low voltage	$V_{RL}$	$V_{SSA} - 0.1$	$V_{SSA} + 0.1$	V
38	$V_{RL}$ differential voltage	$V_{RL} - V_{SSA}$	–100	100	mV
39	Analog reference high voltage	$V_{RH}$	$V_{DDA} - 0.1$	$V_{DDA} + 0.1$	V
40	$V_{REF}$ differential voltage	$V_{RH} - V_{RL}$	4.5	5.25	V
41	$V_{SSSYN}$ to $V_{SS}$ differential voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
42	$V_{RCVSS}$ to $V_{SS}$ differential voltage	$V_{RCVSS} - V_{SS}$	–50	50	mV
43	$V_{DDF}$ to $V_{DD}$ differential voltage	$V_{DDF} - V_{DD}$	–100	100	mV
43a	$V_{RC33}$ to $V_{DDSYN}$ differential voltage	$V_{RC33} - V_{DDSYN}$	–0.1	0.1 <sup>17</sup>	V
44	Analog input differential signal range (with common mode 2.5 V)	$V_{IDIFF}$	–2.5	2.5	V
45	Operating temperature range, ambient (packaged)	$T_A = (T_L \text{ to } T_H)$	$T_L$	$T_H$	°C
46	Slew rate on power-supply pins	—	—	50	V/ms

<sup>1</sup>  $V_{DDE2}$  and  $V_{DDE3}$  are limited to 2.25–3.6 V only if SIU\_ECCR[EBTS] = 0;  $V_{DDE2}$  and  $V_{DDE3}$  have a range of 1.6–3.6 V if SIU\_ECCR[EBTS] = 1.



## Electrical Characteristics

- <sup>2</sup>  $|V_{DDA0} - V_{DDA1}|$  must be  $< 0.1$  V.
- <sup>3</sup>  $V_{PP}$  can drop to 3.0 V during read operations.
- <sup>4</sup> If standby operation is not required, connect  $V_{STBY}$  to ground.
- <sup>5</sup> Applies to CLKOUT, external bus pins, and Nexus pins.
- <sup>6</sup> Maximum average RMS DC current.
- <sup>7</sup> Average current measured on Automotive benchmark.
- <sup>8</sup> Peak currents can be higher on specialized code.
- <sup>9</sup> High use current measured while running optimized SPE assembly code with all code and data 100% locked in cache (0% miss rate) with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM. Higher currents are possible if an idle loop that crosses cache lines is run from cache. Design and write code to avoid this condition.
- <sup>10</sup> The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see [Section 3.7, "Power-Up/Down Sequencing"](#), [Figure 2](#).
- <sup>11</sup> Power requirements for the  $V_{DD33}$  supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to [Table 11](#) for values to calculate the power dissipation for a specific operation.
- <sup>12</sup> Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to [Table 10](#) for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
- <sup>13</sup> Absolute value of current, measured at  $V_{IL}$  and  $V_{IH}$ .
- <sup>14</sup> Weak pullup/down inactive. Measured at  $V_{DDE} = 3.6$  V and  $V_{DDEH} = 5.25$  V. Applies to pad types: pad\_fc, pad\_sh, and pad\_mh.
- <sup>15</sup> Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 °C to 12 °C, in the ambient temperature range of 50 °C to 125 °C. Applies to pad types: pad\_a and pad\_ae.
- <sup>16</sup>  $V_{SSA}$  refers to both  $V_{SSA0}$  and  $V_{SSA1}$ .  $|V_{SSA0} - V_{SSA1}|$  must be  $< 0.1$  V.
- <sup>17</sup> Up to 0.6 V during power up and power down.

### 3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

**Table 10. I/O Pad Average DC Current ( $T_A = T_L$  to  $T_H$ )<sup>1</sup>**

Spec	Pad Type	Symbol	Frequency (MHz)	Load <sup>2</sup> (pF)	Voltage (V)	Drive Select / Slew Rate Control Setting	Current (mA)
1	Slow	$I_{DRV\_SH}$	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	$I_{DRV\_MH}$	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9
9	Fast	$I_{DRV\_FC}$	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

<sup>1</sup> These values are estimates from simulation and are not tested. Currents apply to output pins only.

<sup>2</sup> All loads are lumped.

### 3.8.2 I/O Pad $V_{DD33}$ Current Specifications

The power consumption of the  $V_{DD33}$  supply depends on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin  $V_{DD33}$  currents for all I/O segments. The output pin  $V_{DD33}$  current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad\_fc) pins. The input pin  $V_{DD33}$  current can be calculated from Table 11 based on the voltage, frequency, and load on all pad\_sh and pad\_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

**Table 11.  $V_{DD33}$  Pad Average DC Current ( $T_A = T_L$  to  $T_H$ )<sup>1</sup>**

Spec	Pad Type	Symbol	Frequency (MHz)	Load <sup>2</sup> (pF)	$V_{DD33}$ (V)	$V_{DDE}$ (V)	Drive Select	Current (mA)
<b>Inputs</b>								
1	Slow	$I_{33\_SH}$	66	0.5	3.6	5.5	NA	0.003
2	Medium	$I_{33\_MH}$	66	0.5	3.6	5.5	NA	0.003
<b>Outputs</b>								
3	Fast	$I_{33\_FC}$	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

<sup>1</sup> These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

<sup>2</sup> All loads are lumped.

### 3.9 Oscillator and FMPLL Electrical Characteristics

Table 12. FMPLL Electrical Specifications

( $V_{DDSYN} = 3.0\text{--}3.6\text{ V}$ ;  $V_{SS} = V_{SSSYN} = 0.0\text{ V}$ ;  $T_A = T_L$  to  $T_H$ )

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL reference frequency range: <sup>1</sup> Crystal reference External reference Dual controller (1:1 mode)	$f_{ref\_crystal}$ $f_{ref\_ext}$ $f_{ref\_1:1}$	8 8 24	20 20 $f_{sys} \div 2$	MHz
2	System frequency <sup>2</sup>	$f_{sys}$	$f_{ICO(MIN)} \div 2^{RFD}$	$f_{MAX}$ <sup>3</sup>	MHz
3	System clock period	$t_{CYC}$	—	$1 \div f_{sys}$	ns
4	Loss of reference frequency <sup>4</sup>	$f_{LOR}$	100	1000	kHz
5	Self-clocked mode (SCM) frequency <sup>5</sup>	$f_{SCM}$	7.4	17.5	MHz
6	EXTAL input high voltage crystal mode <sup>6</sup>  All other modes [dual controller (1:1), bypass, external reference]	$V_{IHEXT}$	$V_{XTAL} + 0.4\text{ V}$	—	V
		$V_{IHEXT}$	$(V_{DDE5} \div 2) + 0.4\text{ V}$	—	V
7	EXTAL input low voltage crystal mode <sup>7</sup>  All other modes [dual controller (1:1), bypass, external reference]	$V_{ILEXT}$	—	$V_{XTAL} - 0.4\text{ V}$	V
		$V_{ILEXT}$	—	$(V_{DDE5} \div 2) - 0.4\text{ V}$	V
8	XTAL current <sup>8</sup>	$I_{XTAL}$	0.8	3	mA
9	Total on-chip stray capacitance on XTAL	$C_{S\_XTAL}$	—	1.5	pF
10	Total on-chip stray capacitance on EXTAL	$C_{S\_EXTAL}$	—	1.5	pF
11	Crystal manufacturer's recommended capacitive load	$C_L$	Refer to crystal specification	Refer to crystal specification	pF
12	Discrete load capacitance to connect to EXTAL	$C_{L\_EXTAL}$	—	$(2 \times C_L) - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ <sup>9</sup>	pF
13	Discrete load capacitance to connect to XTAL	$C_{L\_XTAL}$	—	$(2 \times C_L) - C_{S\_XTAL} - C_{PCB\_XTAL}$ <sup>9</sup>	pF
14	PLL lock time <sup>10</sup>	$t_{lpll}$	—	750	μs
15	Dual controller (1:1) clock skew (between CLKOUT and EXTAL) <sup>11, 12</sup>	$t_{skew}$	−2	2	ns
16	Duty cycle of reference	$t_{DC}$	40	60	%
17	Frequency unLOCK range	$f_{UL}$	−4.0	4.0	% $f_{sys}$
18	Frequency LOCK range	$f_{LCK}$	−2.0	2.0	% $f_{sys}$

## Table 12. FMPLL Electrical Specifications (continued)

( $V_{DDSYN} = 3.0\text{--}3.6\text{ V}$ ;  $V_{SS} = V_{SSSYN} = 0.0\text{ V}$ ;  $T_A = T_L$  to  $T_H$ )

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
19	CLKOUT period jitter, measured at $f_{SYS}$ max: <sup>13, 14</sup> Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over a 2 ms interval)	$C_{JITTER}$	— —	5.0 0.01	% $f_{CLKOUT}$
20	Frequency modulation range limit <sup>15</sup> (do not exceed $f_{SYS}$ maximum)	$C_{MOD}$	0.8	2.4	% $f_{SYS}$
21	ICO frequency $f_{ICO} = [f_{ref\_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ <sup>16</sup> $f_{ICO} = [f_{ref\_ext} \times (MFD + 4)] \div (PREDIV + 1)$	$f_{ICO}$	48	$f_{MAX}$	MHz
22	Predivider output frequency (to PLL)	$f_{PREDIV}$	4	20 <sup>17</sup>	MHz

<sup>1</sup> Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within  $\pm 5\%$  of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.

<sup>2</sup> All internal registers retain data at 0 Hz.

<sup>3</sup> Up to the maximum frequency rating of the device (refer to Table 1).

<sup>4</sup> Loss of reference frequency is defined as the reference frequency detected internally, which transitions the PLL into self-clocked mode.

<sup>5</sup> The PLL operates at self-clocked mode (SCM) frequency when the reference frequency falls below  $f_{LOR}$ . SCM frequency is measured on the CLKOUT ball with the divider set to divide-by-two of the system clock.  
NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

<sup>6</sup> Use the EXTAL input high voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ( $V_{extal} - V_{xtal}$ ) must be  $\geq 400\text{ mV}$  for the oscillator's comparator to produce the output clock.

<sup>7</sup> Use the EXTAL input low voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ( $V_{xtal} - V_{extal}$ ) must be  $\geq 400\text{ mV}$  for the oscillator's comparator to produce the output clock.

<sup>8</sup>  $I_{xtal}$  is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

<sup>9</sup>  $C_{PCB\_EXTAL}$  and  $C_{PCB\_XTAL}$  are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

<sup>10</sup> This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time also includes the crystal startup time.

<sup>11</sup> PLL is operating in 1:1 PLL mode.

<sup>12</sup>  $V_{DDE} = 3.0\text{--}3.6\text{ V}$ .

<sup>13</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{SYS}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via  $V_{DDSYN}$  and  $V_{SSSYN}$  and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider is set to divide-by-two.

<sup>14</sup> Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of (jitter + Cmod).

<sup>15</sup> Modulation depth selected must not result in  $f_{SYS}$  value greater than the  $f_{SYS}$  maximum specified value.

<sup>16</sup>  $f_{SYS} = f_{ICO} \div (2^{RFD})$ .

<sup>17</sup> Maximum value for dual controller (1:1) mode is ( $f_{MAX} \div 2$ ) with the predivider set to 1 (FMPLL\_SYNCR[PREDIV] = 0b001).



### 3.10 eQADC Electrical Characteristics

Table 13. eQADC Conversion Specifications ( $T_A = T_L$  to  $T_H$ )

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	ADC clock (ADCLK) frequency <sup>1</sup>	$F_{ADCLK}$	1	12	MHz
2	Conversion cycles Differential Single ended	CC	13 + 2 (15) 14 + 2 (16)	13 + 128 (141) 14 + 128 (142)	ADCLK cycles
3	Stop mode recovery time <sup>2</sup>	$T_{SR}$	10	—	$\mu$ s
4	Resolution <sup>3</sup>	—	1.25	—	mV
5	INL: 6 MHz ADC clock	INL6	−4	4	Counts <sup>3</sup>
6	INL: 12 MHz ADC clock	INL12	−8	8	Counts
7	DNL: 6 MHz ADC clock	DNL6	−3 <sup>4</sup>	3 <sup>4</sup>	Counts
8	DNL: 12 MHz ADC clock	DNL12	−6 <sup>4</sup>	6 <sup>4</sup>	Counts
9	Offset error with calibration	OFFWC	−4 <sup>5</sup>	4 <sup>5</sup>	Counts
10	Full-scale gain error with calibration	GAINWC	−8 <sup>6</sup>	8 <sup>6</sup>	Counts
11	Disruptive input injection current <sup>7, 8, 9, 10</sup>	$I_{INJ}$	−1	1	mA
12	Incremental error due to injection current. All channels are 10 k $\Omega$ < $R_s$ < 100 k $\Omega$ Channel under test has $R_s = 10$ k $\Omega$ , $I_{INJ} = I_{INJMAX}, I_{INJMIN}$	$E_{INJ}$	−4	4	Counts
13	Total unadjusted error (TUE) for single ended conversions with calibration <sup>11, 12, 13, 14, 15</sup>	TUE	−4	4	Counts

<sup>1</sup> Conversion characteristics vary with  $F_{ADCLK}$  rate. Reduced conversion accuracy occurs at maximum  $F_{ADCLK}$  rate. The maximum value is based on 800 KS/s and the minimum value is based on 20 MHz oscillator clock frequency divided by a maximum 16 factor.

<sup>2</sup> Stop mode recovery time begins when the ADC control register enable bits are set until the ADC is ready to perform conversions.

<sup>3</sup> At  $V_{RH} - V_{RL} = 5.12$  V, one least significant bit (LSB) = 1.25, mV = one count.

<sup>4</sup> Guaranteed 10-bit mono tonicity.

<sup>5</sup> The absolute value of the offset error without calibration  $\leq 100$  counts.

<sup>6</sup> The absolute value of the full scale gain error without calibration  $\leq 120$  counts.

<sup>7</sup> Below disruptive current conditions, the channel being stressed has conversion values of: 0x3FF for analog inputs greater than  $V_{RH}$ , and 0x000 for values less than  $V_{RL}$ . This assumes that  $V_{RH} \leq V_{DDA}$  and  $V_{RL} \geq V_{SSA}$  due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

<sup>8</sup> Exceeding the limit can cause a conversion error on both stressed and unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

<sup>9</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using  $V_{POSCLAMP} = V_{DDA} + 0.5$  V and  $V_{NEGCLAMP} = -0.3$  V, then use the larger of the calculated values.

<sup>10</sup> This condition applies to two adjacent pads on the internal pad.

<sup>11</sup> The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

<sup>12</sup> TUE does not apply to differential conversions.

<sup>13</sup> Measured at 6 MHz ADC clock. TUE with a 12 MHz ADC clock is: −16 counts < TUE < 16 counts.

<sup>14</sup> TUE includes all internal device errors such as internal reference variation (75% Ref, 25% Ref).

<sup>15</sup> Depending on the input impedance, the analog input leakage current (Table 9. DC Electrical Specifications, spec 35a) can affect the actual TUE measured on analog channels AN[12], AN[13], AN[14], AN[15].

## 3.11 H7Fa Flash Memory Electrical Characteristics

Table 14. Flash Program and Erase Specifications ( $T_A = T_L$  to  $T_H$ )

Spec	Flash Program Characteristic	Symbol	Min.	Typical <sup>1</sup>	Initial Max. <sup>2</sup>	Max. <sup>3</sup>	Unit
3	Doubleword (64 bits) program time <sup>4</sup>	$T_{dwprogram}$	—	10	—	500	$\mu s$
4	Page program time <sup>4</sup>	$T_{pprogram}$	—	22	44 <sup>5</sup>	500	$\mu s$
7	16 KB block pre-program and erase time	$T_{16kpperase}$	—	265	400	5000	ms
9	48 KB block pre-program and erase time	$T_{48kpperase}$	—	345	400	5000	ms
10	64 KB block pre-program and erase time	$T_{64kpperase}$	—	415	500	5000	ms
8	128 KB block pre-program and erase time	$T_{128kpperase}$	—	500	1250	7500	ms
11	Minimum operating frequency for program and erase operations <sup>6</sup>	—	25	—	—	—	MHz

<sup>1</sup> Typical program and erase times are calculated at 25 °C operating temperature using nominal supply values.

<sup>2</sup> Initial factory condition:  $\leq 100$  program/erase cycles, 25 °C, using a typical supply voltage measured at a minimum system frequency of 80 MHz.

<sup>3</sup> The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

<sup>4</sup> Actual hardware programming times. This does not include software overhead.

<sup>5</sup> Page size is 256 bits (8 words).

<sup>6</sup> The read frequency of the flash can range up to the maximum operating frequency. There is no minimum read frequency condition.

Table 15. Flash EEPROM Module Life ( $T_A = T_L$  to  $T_H$ )

Spec	Characteristic	Symbol	Min.	Typical <sup>1</sup>	Unit
1a	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range ( $T_J$ )	P/E	100,000	—	cycles
1b	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range ( $T_J$ )	P/E	1000	100,000	cycles
2	Data retention Blocks with 0–1,000 P/E cycles Blocks with 1,001–100,000 P/E cycles	Retention	20 5	— —	years

<sup>1</sup> Typical endurance is evaluated at 25° C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of typical endurance, refer to engineering bulletin EB619 Typical Endurance for Nonvolatile Memory.

Table 16 shows the FLASH\_BIU settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

**Table 16. FLASH\_BIU Settings vs. Frequency of Operation <sup>1</sup>**

Maximum Frequency (MHz)	APC	RWSC	WWSC	DPFEN <sup>2</sup>	IPFEN <sup>2</sup>	PFLIM <sup>3</sup>	BFEN <sup>4</sup>
Up to and including 82 MHz <sup>5</sup>	0b001	0b001	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Up to and including 102 MHz <sup>6</sup>	0b001	0b010	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Up to and including 132 MHz <sup>7</sup>	0b010	0b011	0b01	0b00 0b01 0b11	0b00 0b01 0b11	0b000 to 0b110	0b0 0b1
Default setting after reset	0b111	0b111	0b11	0b00	0b00	0b000	0b0

<sup>1</sup> Illegal combinations exist. Use entries from the same row in this table.

<sup>2</sup> For maximum flash performance, set to 0b11.

<sup>3</sup> For maximum flash performance, set to 0b110.

<sup>4</sup> For maximum flash performance, set to 0b1.

<sup>5</sup> 82 MHz parts allow for 80 MHz system clock + 2% frequency modulation (FM).

<sup>6</sup> 102 MHz parts allow for 100 MHz system clock + 2% FM.

<sup>7</sup> 132 MHz parts allow for 128 MHz system clock + 2% FM.

## 3.12 AC Specifications

### 3.12.1 Pad AC Specifications

**Table 17. Pad AC Specifications ( $V_{DDEH} = 5.0\text{ V}$ ,  $V_{DDE} = 1.8\text{ V}$ ) <sup>1</sup>**

Spec	Pad	SRC / DSC (binary)	Out Delay (ns) <sup>2, 3, 4</sup>	Rise / Fall (ns) <sup>4, 5</sup>	Load Drive (pF)
1	Slow high voltage (SH)	11	26	15	50
			82	60	200
		01	75	40	50
			137	80	200
		00	377	200	50
			476	260	200
2	Medium high voltage (MH)	11	16	8	50
			43	30	200
		01	34	15	50
			61	35	200
		00	192	100	50
			239	125	200