



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# MPC555 / MPC556

## USER'S MANUAL

Revised 15 October 2000



# MPC555 / MPC556

## USER'S MANUAL

Revised 15 October 2000



**PREFACE**

**Section 1  
OVERVIEW**

1.1	Block Diagram . . . . .	1-1
1.2	MPC555 / MPC556 Features . . . . .	1-2
1.2.1	RISC MCU Central Processing Unit (RCPU) . . . . .	1-2
1.2.2	Four-Bank Memory Controller . . . . .	1-3
1.2.3	U-Bus System Interface Unit (USIU) . . . . .	1-3
1.2.4	Flexible Memory Protection Unit . . . . .	1-3
1.2.5	448 Kbytes of CDR MoneT Flash EEPROM Memory (CMF) . . . . .	1-3
1.2.6	26 Kbytes of Static RAM . . . . .	1-3
1.2.7	General-Purpose I/O Support . . . . .	1-4
1.2.8	Two Time Processor Units (TPU3) . . . . .	1-4
1.2.9	18-Channel Modular I/O System (MIOS1) . . . . .	1-4
1.2.10	Two Queued Analog-to-Digital Converter Modules (QADC) . . . . .	1-4
1.2.11	Two CAN 2.0B Controller Modules (TouCANs) . . . . .	1-5
1.2.12	Queued Serial Multi-Channel Module (QSMCM) . . . . .	1-5
1.3	MPC555 / MPC556 Address Map . . . . .	1-5

**Section 2  
SIGNAL DESCRIPTIONS**

2.1	Packaging and Pinout Descriptions . . . . .	2-1
2.2	Pin Functionality . . . . .	2-6
2.3	Signal Descriptions . . . . .	2-12
2.3.1	USIU Pads . . . . .	2-12
2.3.1.1	ADDR[8:31]/SGPIOA[8:31] . . . . .	2-12
2.3.1.2	DATA[0:31]/SGPIOD[0:31] . . . . .	2-13
2.3.1.3	$\overline{\text{IRQ}}[0]/\text{SGPIOC}[0]$ . . . . .	2-13
2.3.1.4	$\overline{\text{IRQ}}[1]/\overline{\text{RSV}}/\text{SGPIOC}[1]$ . . . . .	2-13
2.3.1.5	$\overline{\text{IRQ}}[2]/\overline{\text{CR}}/\text{SGPIOC}[2]/\overline{\text{MTS}}$ . . . . .	2-13
2.3.1.6	$\overline{\text{IRQ}}[3]/\overline{\text{KR}}/\overline{\text{RETRY}}/\text{SGPIOC}[3]$ . . . . .	2-13
2.3.1.7	$\overline{\text{IRQ}}[4]/\text{AT}[2]/\text{SGPIOC}[4]$ . . . . .	2-14
2.3.1.8	$\overline{\text{IRQ}}[5]/\text{SGPIOC}[5]/\text{MODCK}[1]$ . . . . .	2-14
2.3.1.9	$\overline{\text{IRQ}}[6:7]/\text{MODCK}[2:3]$ . . . . .	2-14
2.3.1.10	TSIZ[0:1] . . . . .	2-14
2.3.1.11	$\text{RD}/\overline{\text{WR}}$ . . . . .	2-15
2.3.1.12	$\overline{\text{BURST}}$ . . . . .	2-15
2.3.1.13	$\overline{\text{BDIP}}$ . . . . .	2-15
2.3.1.14	$\overline{\text{TS}}$ . . . . .	2-15
2.3.1.15	$\overline{\text{TA}}$ . . . . .	2-15

Paragraph Number	Page Number
2.3.1.16 $\overline{TEA}$ .....	2-15
2.3.1.17 $\overline{RSTCONF}/\overline{TEXP}$ .....	2-16
2.3.1.18 $\overline{OE}$ .....	2-16
2.3.1.19 $\overline{BI}/\overline{STS}$ .....	2-16
2.3.1.20 $\overline{CS}[0:3]$ .....	2-16
2.3.1.21 $\overline{WE}[0:3]/\overline{BE}[0:3]/\overline{AT}[0:3]$ .....	2-16
2.3.1.22 $\overline{PORESET}$ .....	2-17
2.3.1.23 $\overline{HRESET}$ .....	2-17
2.3.1.24 $\overline{SRESET}$ .....	2-17
2.3.1.25 $\overline{SGPIOC}[6]/\overline{FRZ}/\overline{PTR}$ .....	2-17
2.3.1.26 $\overline{SGPIOC}[7]/\overline{IRQOUT}/\overline{LWP}[0]$ .....	2-18
2.3.1.27 $\overline{BG}/\overline{VF}[0]/\overline{LWP}[1]$ .....	2-18
2.3.1.28 $\overline{BR}/\overline{VF}[1]/\overline{IWP}[2]$ .....	2-18
2.3.1.29 $\overline{BB}/\overline{VF}[2]/\overline{IWP}[3]$ .....	2-18
2.3.1.30 $\overline{IWP}[0:1]/\overline{VFLS}[0:1]$ .....	2-19
2.3.1.31 TMS .....	2-19
2.3.1.32 TDI/DSDI .....	2-19
2.3.1.33 TCK/DSCK .....	2-19
2.3.1.34 TDO/DSDO .....	2-19
2.3.1.35 $\overline{TRST}$ .....	2-20
2.3.1.36 XTAL .....	2-20
2.3.1.37 EXTAL .....	2-20
2.3.1.38 XFC .....	2-20
2.3.1.39 CLKOUT .....	2-20
2.3.1.40 EXTCLK .....	2-20
2.3.1.41 VDDSYN .....	2-20
2.3.1.42 VSSSYN .....	2-20
2.3.1.43 ENGCLK/BUCLK .....	2-21
2.3.2 QSMCM PADS .....	2-21
2.3.2.1 $\overline{PCS0}/\overline{SS}/\overline{QGPIO}[0]$ .....	2-21
2.3.2.2 $\overline{PCS}(1:3)/\overline{QGPIO}[1:3]$ .....	2-21
2.3.2.3 $\overline{MISO}/\overline{QGPIO}[4]$ .....	2-21
2.3.2.4 $\overline{MOSI}/\overline{QGPIO}[5]$ .....	2-21
2.3.2.5 $\overline{SCK}/\overline{QGPIO}[6]$ .....	2-22
2.3.2.6 $\overline{TXD}[1:2]/\overline{QGPO}[1:2]$ .....	2-22
2.3.2.7 $\overline{RXD}[1:2]/\overline{QGPI}[1:2]$ .....	2-22
2.3.2.8 ECK .....	2-22
2.3.3 MIOS PADS .....	2-22
2.3.3.1 MDA[11], [13] .....	2-22
2.3.3.2 MDA[12], [14] .....	2-23
2.3.3.3 MDA[15], [27:31] .....	2-23
2.3.3.4 $\overline{MPWM}[0:3]$ , [16:19] .....	2-23
2.3.3.5 $\overline{VF}[0:2]/\overline{MPIO32B}[0:2]$ .....	2-23

<b>Paragraph Number</b>	<b>Page Number</b>
2.3.3.6 VFLS[0:1]/MPIO32B[3:4]	2-23
2.3.3.7 MPIO32B[5:15]	2-24
2.3.4 TPU_A/TPU_B PADS	2-24
2.3.4.1 TPUCH[0:15]_[A:B]	2-24
2.3.4.2 T2CLK	2-24
2.3.5 QADC_A/QADC_B PADS	2-24
2.3.5.1 ETRIG[1:2]	2-24
2.3.5.2 AN[0]/ANW/PQB[0]_[A:B]	2-24
2.3.5.3 AN[1]/ANX/PQB[1]_[A:B]	2-24
2.3.5.4 AN[2]/ANY/PQB[2]_[A:B]	2-25
2.3.5.5 AN[3]/ANZ/PQB[3]_[A:B]	2-25
2.3.5.6 AN[48:51]/PQB[4:7]_[A:B]	2-25
2.3.5.7 AN[52:54]/MA[0:2]/PQA[0:2]_[A:B]	2-25
2.3.5.8 AN[55:59]/PQA[3:7]_[A:B]	2-26
2.3.5.9 VRH	2-26
2.3.5.10 VRL	2-26
2.3.5.11 VDDA	2-26
2.3.5.12 VSSA	2-26
2.3.6 TOUCAN_A/TOUCAN_B PADS	2-26
2.3.6.1 CNTX0_[A:B]	2-26
2.3.6.2 CNRX0_[A:B]	2-26
2.3.7 CMF PADS	2-27
2.3.7.1 EPEE	2-27
2.3.7.2 VPP	2-27
2.3.7.3 VDDF	2-27
2.3.7.4 VSSF	2-27
2.3.8 GLOBAL POWER SUPPLIES	2-27
2.3.8.1 VDDL	2-27
2.3.8.2 VDDH	2-27
2.3.8.3 VDDI	2-27
2.3.8.4 VSSI	2-27
2.3.8.5 KAPWR	2-28
2.3.8.6 VDDSRAM	2-28
2.3.8.7 VSS	2-28
2.4 Reset State	2-28
2.4.1 Pin Functionality Out of Reset	2-28
2.4.2 Pad Module Configuration Register (PDMCR)	2-28
2.4.3 Pin State During Reset	2-29
2.4.4 Power-On Reset and Hard Reset	2-30
2.4.5 Pull-Up and Pull-Down Enable and Disable for 5-V Only Pins	2-30
2.4.6 Pull-Up and Pull-Down Enable and Disable for 3-V / 5-V Multiplexed Pins	2-30
2.4.6.1 PRDS Signal	2-30
2.4.6.2 Encoded 3-V / 5-V Select	2-31

<b>Paragraph Number</b>	<b>Page Number</b>
2.4.6.3 Examples .....	2-31
2.4.7 Special Pull Resistor Disable Control (SPRDS) .....	2-31
2.4.8 Pin Reset States .....	2-32
2.5 Pad Types .....	2-37
2.5.1 Pad Interface Signals .....	2-37
2.5.2 Three-Volt Output Pad .....	2-38
2.5.2.1 Type A Interface .....	2-38
2.5.2.2 Type B Interface (Clock Pad) .....	2-39
2.5.3 Three-Volt Input Pad .....	2-39
2.5.3.1 Type C Interface .....	2-40
2.5.3.2 Type CH Interface .....	2-40
2.5.3.3 Type CNH Interface .....	2-41
2.5.3.4 Type D Interface .....	2-41
2.5.4 Three-Volt Input/Output Pad .....	2-41
2.5.4.1 Type E Interface .....	2-42
2.5.4.2 Type EOH Interface .....	2-42
2.5.4.3 Type F Interface .....	2-43
2.5.4.4 Type G Interface .....	2-44
2.5.5 Five-Volt Input/Output Pad .....	2-45
2.5.5.1 Type H Interface .....	2-45
2.5.5.2 Type I Interface .....	2-46
2.5.5.3 Type IH Interface .....	2-48
2.5.5.4 Type J Interface .....	2-49
2.5.5.5 Type JD Interface .....	2-49
2.5.6 Type K Interface (EPEE Pad) .....	2-50
2.5.7 Analog Pads .....	2-51
2.5.7.1 Type L Interface (QADC Port A) .....	2-51
2.5.7.2 Type M Interface (QADC Port B) .....	2-52
2.5.7.3 Type N Interface (ETRIG) .....	2-53
2.5.8 Pads with Fast Mode .....	2-53
2.5.8.1 Type O Interface (QSMCM Pads) .....	2-53
2.5.8.2 Type P Interface (TPU and MIOS Pads) .....	2-54
2.5.9 5V Input, 5V Output Pads .....	2-55
2.5.9.1 5V Output (Type Q) .....	2-55
2.5.9.2 Type R Interface .....	2-56
2.5.9.3 5V Output for Clock Pad .....	2-57
2.6 Pad Groups .....	2-57
2.7 Pin Names and Abbreviations .....	2-58

## Section 3 CENTRAL PROCESSING UNIT

3.1 RCPU Features .....	3-1
3.2 RCPU Block Diagram .....	3-2

<b>Paragraph Number</b>	<b>Page Number</b>
3.3 Instruction Sequencer . . . . .	3-3
3.4 Independent Execution Units . . . . .	3-4
3.4.1 Branch Processing Unit (BPU) . . . . .	3-5
3.4.2 Integer Unit (IU) . . . . .	3-5
3.4.3 Load/Store Unit (LSU) . . . . .	3-6
3.4.4 Floating-Point Unit (FPU) . . . . .	3-6
3.5 Levels of the PowerPC Architecture . . . . .	3-7
3.6 RCPU Programming Model . . . . .	3-7
3.7 PowerPC UISA Register Set . . . . .	3-11
3.7.1 General-Purpose Registers (GPRs) . . . . .	3-12
3.7.2 Floating-Point Registers (FPRs) . . . . .	3-12
3.7.3 Floating-Point Status and Control Register (FPSCR) . . . . .	3-12
3.7.4 Condition Register (CR) . . . . .	3-15
3.7.4.1 Condition Register CR0 Field Definition . . . . .	3-16
3.7.4.2 Condition Register CR1 Field Definition . . . . .	3-16
3.7.4.3 Condition Register CR $n$ Field — Compare Instruction . . . . .	3-17
3.7.5 Integer Exception Register (XER) . . . . .	3-17
3.7.6 Link Register (LR) . . . . .	3-18
3.7.7 Count Register (CTR) . . . . .	3-19
3.8 PowerPC VEA Register Set — Time Base . . . . .	3-19
3.9 PowerPC OEA Register Set . . . . .	3-20
3.9.1 Machine State Register (MSR) . . . . .	3-20
3.9.2 DAE/Source Instruction Service Register (DSISR) . . . . .	3-22
3.9.3 Data Address Register (DAR) . . . . .	3-22
3.9.4 Time Base Facility (TB) — OEA . . . . .	3-23
3.9.5 Decrementer Register (DEC) . . . . .	3-23
3.9.6 Machine Status Save/Restore Register 0 (SRR0) . . . . .	3-24
3.9.7 Machine Status Save/Restore Register 1 (SRR1) . . . . .	3-24
3.9.8 General SPRs (SPRG0–SPRG3) . . . . .	3-25
3.9.9 Processor Version Register (PVR) . . . . .	3-25
3.9.10 Implementation-Specific SPRs . . . . .	3-26
3.9.10.1 EIE, EID, and NRI Special-Purpose Registers . . . . .	3-26
3.9.10.2 Floating-Point Exception Cause Register (FPECR) . . . . .	3-26
3.9.10.3 Additional Implementation-Specific Registers . . . . .	3-27
3.10 Instruction Set . . . . .	3-28
3.10.1 Instruction Set Summary . . . . .	3-29
3.10.2 Recommended Simplified Mnemonics . . . . .	3-33
3.10.3 Calculating Effective Addresses . . . . .	3-33
3.11 Exception Model . . . . .	3-34
3.11.1 Exception Classes . . . . .	3-34
3.11.2 Ordered Exceptions . . . . .	3-34
3.11.3 Unordered Exceptions . . . . .	3-34
3.11.4 Precise Exceptions . . . . .	3-35



<b>Paragraph Number</b>	<b>Page Number</b>
3.11.5 Exception Vector Table . . . . .	3-35
3.12 Instruction Timing . . . . .	3-36
3.13 PowerPC User Instruction Set Architecture (UISA) . . . . .	3-38
3.13.1 Computation Modes . . . . .	3-38
3.13.2 Reserved Fields . . . . .	3-38
3.13.3 Classes of Instructions . . . . .	3-38
3.13.4 Exceptions . . . . .	3-39
3.13.5 The Branch Processor . . . . .	3-39
3.13.6 Instruction Fetching . . . . .	3-39
3.13.7 Branch Instructions . . . . .	3-39
3.13.7.1 Invalid Branch Instruction Forms . . . . .	3-39
3.13.7.2 Branch Prediction . . . . .	3-39
3.13.8 The Fixed-Point Processor . . . . .	3-39
3.13.8.1 Fixed-Point Instructions . . . . .	3-39
3.13.9 Floating-Point Processor . . . . .	3-40
3.13.9.1 General . . . . .	3-40
3.13.9.2 Optional instructions . . . . .	3-40
3.13.10 Load/Store Processor . . . . .	3-40
3.13.10.1 Fixed-Point Load With Update and Store With Update Instructions . . . . .	3-41
3.13.10.2 Fixed-Point Load and Store Multiple Instructions . . . . .	3-41
3.13.10.3 Fixed-Point Load String Instructions . . . . .	3-41
3.13.10.4 Storage Synchronization Instructions . . . . .	3-41
3.13.10.5 Floating-Point Load and Store With Update Instructions . . . . .	3-41
3.13.10.6 Floating-Point Load Single Instructions . . . . .	3-41
3.13.10.7 Floating-Point Store Single Instructions . . . . .	3-41
3.13.10.8 Optional Instructions . . . . .	3-42
3.13.10.9 Little-Endian Byte Ordering . . . . .	3-42
3.14 PowerPC Virtual Environment Architecture (VEA) . . . . .	3-42
3.14.1 Atomic Update Primitives . . . . .	3-42
3.14.2 Effect of Operand Placement on Performance . . . . .	3-42
3.14.3 Storage Control Instructions . . . . .	3-42
3.14.4 Instruction Synchronize (isync) Instruction . . . . .	3-42
3.14.4.1 Enforce In-Order Execution of I/O (eieio) Instruction . . . . .	3-43
3.14.5 Timebase . . . . .	3-43
3.15 POWERPC Operating Environment Architecture (OEA) . . . . .	3-43
3.15.1 Branch Processor Registers . . . . .	3-43
3.15.1.1 Machine State Register (MSR) . . . . .	3-43
3.15.1.2 Branch Processors Instructions . . . . .	3-43
3.15.2 Fixed-Point Processor . . . . .	3-43
3.15.2.1 Special Purpose Registers . . . . .	3-43
3.15.3 Storage Control Instructions . . . . .	3-44
3.15.4 Interrupts . . . . .	3-44
3.15.4.1 System Reset Interrupt . . . . .	3-44

<b>Paragraph Number</b>	<b>Page Number</b>
3.15.4.2 Machine Check Interrupt .....	3-45
3.15.4.3 Data Storage Interrupt .....	3-45
3.15.4.4 Instruction Storage Interrupt.....	3-46
3.15.4.5 Alignment Interrupt .....	3-46
3.15.4.6 Floating-Point Enabled Exception Type Program Interrupt .....	3-46
3.15.4.7 Illegal Instruction Type Program Interrupt .....	3-46
3.15.4.8 Privileged Instruction Type Program interrupt .....	3-46
3.15.4.9 Floating-Point Unavailable Interrupt .....	3-47
3.15.4.10 Trace Interrupt .....	3-47
3.15.4.11 Floating-Point Assist Interrupt .....	3-47
3.15.4.12 Implementation-Dependent Software Emulation Interrupt .....	3-48
3.15.4.13 Implementation-Specific Instruction Storage Protection Error Interrupt .....	3-49
3.15.4.14 Implementation-Specific Data Storage Protection Error Interrupt .....	3-50
3.15.4.15 Implementation-Specific Debug Interrupts .....	3-51
3.15.4.16 Partially Executed Instructions .....	3-52
3.15.5 Timer Facilities .....	3-53
3.15.6 Optional Facilities and Instructions.....	3-53

## **Section 4 BURST BUFFER**

4.1 Burst Buffer Block Diagram .....	4-1
4.2 Burst Buffer Features .....	4-2
4.3 Instruction VocabularyBased Compression Model Main Principles .....	4-3
4.3.1 Compression Model Features .....	4-3
4.3.2 Model Limitations .....	4-4
4.3.3 Vocabulary Based Instruction Compression Algorithm .....	4-4
4.3.4 Memory Organization .....	4-6
4.3.5 Compressed Code Address Format.....	4-8
4.3.6 Compressed Address Format – Direct Branches.....	4-9
4.3.7 Compressed Address Format – Indirect Branches.....	4-11
4.3.8 Compression Process .....	4-11
4.3.9 Decompression.....	4-13
4.3.10 Compression Environment Initialization .....	4-14
4.4 Modes Of Operation.....	4-14
4.4.1 Normal Operation.....	4-15
4.4.2 Slave Operation.....	4-15
4.4.3 Reset Operation .....	4-15
4.4.4 Debug Mode Operation .....	4-15
4.4.5 Standby Mode Operation .....	4-15
4.4.6 Burst Operation .....	4-15
4.4.7 Error Detection .....	4-16
4.5 Exception Table Relocation .....	4-16
4.5.1 Exception Table Relocation Operation.....	4-17

<b>Paragraph Number</b>	<b>Page Number</b>
4.6 Burst Buffer Programming Model . . . . .	4-20
4.6.1 Region Base Address Registers . . . . .	4-21
4.6.2 Region Attribute Registers MI_RA[0:3] Description . . . . .	4-21
4.6.3 Global Region Attribute Register Description (MI_GRA) . . . . .	4-23
4.6.4 BBC Module Configuration Register (BBCMCR) . . . . .	4-24

**Section 5  
UNIFIED SYSTEM INTERFACE UNIT**

5.1 Module Overview . . . . .	5-1
5.2 SIU Architecture . . . . .	5-2
5.3 USIU Address Map . . . . .	5-2
5.4 USIU PowerPC Memory Map . . . . .	5-5

**Section 6  
SYSTEM CONFIGURATION AND PROTECTION**

6.1 System Configuration . . . . .	6-3
6.1.1 USIU Pins Multiplexing . . . . .	6-3
6.1.2 Memory Mapping . . . . .	6-3
6.1.3 Arbitration Support . . . . .	6-4
6.2 External Master Modes . . . . .	6-5
6.2.1 Operation of External Master Modes . . . . .	6-5
6.2.2 Address Decoding for External Accesses . . . . .	6-6
6.3 USIU General-Purpose I/O . . . . .	6-6
6.4 Interrupt Controller . . . . .	6-8
6.4.1 SIU Interrupt Sources Priority . . . . .	6-11
6.5 Hardware Bus Monitor . . . . .	6-12
6.6 MPC555 / MPC556 Decrementer . . . . .	6-12
6.7 MPC555 / MPC556 Time Base (TB) . . . . .	6-13
6.8 Real-Time Clock (RTC) . . . . .	6-14
6.9 Periodic Interrupt Timer (PIT) . . . . .	6-15
6.10 Software Watchdog Timer (SWT) . . . . .	6-16
6.11 Freeze Operation . . . . .	6-17
6.12 Low Power Stop Operation . . . . .	6-17
6.13 System Configuration and Protection Registers . . . . .	6-18
6.13.1 System Configuration Registers . . . . .	6-18
6.13.1.1 SIU Module Configuration Register . . . . .	6-18
6.13.1.2 Internal Memory Map Register . . . . .	6-21
6.13.1.3 External Master Control Register (EMCR) . . . . .	6-22
6.13.2 SIU Interrupt Registers . . . . .	6-23
6.13.2.1 SIPEND Register . . . . .	6-23
6.13.2.2 SIU Interrupt Mask Register (SIMASK) . . . . .	6-24
6.13.2.3 SIU Interrupt Edge Level Register (SIEL) . . . . .	6-25
6.13.2.4 SIU Interrupt Vector Register . . . . .	6-25
6.13.3 System Protection Registers . . . . .	6-26

<b>Paragraph Number</b>	<b>Page Number</b>
6.13.3.1 System Protection Control Register (SYPCR) .....	6-26
6.13.3.2 Software Service Register (SWSR) .....	6-26
6.13.3.3 Transfer Error Status Register (TESR) .....	6-27
6.13.4 System Timer Registers .....	6-28
6.13.4.1 Decrementer Register .....	6-28
6.13.4.2 Time Base SPRs .....	6-28
6.13.4.3 Time Base Reference Registers .....	6-29
6.13.4.4 Time Base Control and Status Register .....	6-29
6.13.4.5 Real-Time Clock Status and Control Register .....	6-30
6.13.4.6 Real-Time Clock Register (RTC) .....	6-31
6.13.4.7 Real-Time Clock Alarm Register (RTCAL) .....	6-31
6.13.4.8 Periodic Interrupt Status and Control Register (PISCR) .....	6-32
6.13.4.9 Periodic Interrupt Timer Count Register (PITC) .....	6-32
6.13.4.10 Periodic Interrupt Timer Register (PITR) .....	6-33
6.13.5 General-Purpose I/O Registers .....	6-34
6.13.5.1 SGPIO Data Register 1 (SGPIODT1) .....	6-34
6.13.5.2 SGPIO Data Register 2 (SGPIODT2) .....	6-34
6.13.5.3 SGPIO Control Register (SGPIOCR) .....	6-35

## **Section 7 RESET**

7.1 Reset Operation .....	7-1
7.1.1 Power On Reset .....	7-1
7.1.2 Hard Reset .....	7-2
7.1.3 Soft Reset .....	7-2
7.1.4 Loss of Lock .....	7-3
7.1.5 On-Chip Clock Switch .....	7-3
7.1.6 Software Watchdog Reset .....	7-3
7.1.7 Checkstop Reset .....	7-3
7.1.8 Debug Port Hard Reset .....	7-3
7.1.9 Debug Port Soft Reset .....	7-3
7.1.10 JTAG Reset .....	7-3
7.2 Reset Actions Summary .....	7-3
7.3 Data Coherency During Reset .....	7-4
7.4 Reset Status Register .....	7-5
7.5 Reset Configuration .....	7-6
7.5.1 Hard Reset Configuration .....	7-6
7.5.2 Hard Reset Configuration Word .....	7-11
7.5.3 Soft Reset Configuration .....	7-12

## **Section 8 CLOCKS AND POWER CONTROL**

8.1 Overview .....	8-1
8.2 System Clock Sources .....	8-3

<b>Paragraph Number</b>	<b>Page Number</b>
8.3 System PLL . . . . .	8-3
8.3.1 Frequency Multiplication . . . . .	8-4
8.3.2 Skew Elimination . . . . .	8-4
8.3.3 Pre-Divider . . . . .	8-4
8.3.4 PLL Block Diagram . . . . .	8-4
8.3.5 PLL Pins . . . . .	8-5
8.4 System Clock During PLL Loss of Lock . . . . .	8-6
8.5 Low-Power Divider . . . . .	8-6
8.6 MPC555 / MPC556 Internal Clock Signals . . . . .	8-7
8.6.1 General System Clocks . . . . .	8-9
8.6.2 CLKOUT . . . . .	8-12
8.6.3 Engineering Clock . . . . .	8-12
8.7 Clock Source Switching . . . . .	8-13
8.8 Low-Power Modes . . . . .	8-15
8.8.1 Entering a Low-Power Mode . . . . .	8-15
8.8.2 Power Mode Descriptions . . . . .	8-16
8.8.3 Exiting from Low-Power Modes . . . . .	8-16
8.8.3.1 Exiting from Normal-Low Mode . . . . .	8-17
8.8.3.2 Exiting from Doze Mode . . . . .	8-17
8.8.3.3 Exiting from Deep-Sleep Mode . . . . .	8-17
8.8.3.4 Exiting from Power-Down Mode . . . . .	8-18
8.8.3.5 Low-Power Modes Flow . . . . .	8-18
8.9 Basic Power Structure . . . . .	8-20
8.9.1 Clock Unit Power Supply . . . . .	8-20
8.9.2 Chip Power Structure . . . . .	8-20
8.9.2.1 VDDL . . . . .	8-20
8.9.2.2 VDDI . . . . .	8-20
8.9.2.3 VDDSYN, VSSSYN . . . . .	8-21
8.9.2.4 KAPWR . . . . .	8-21
8.9.2.5 VDDA, VSSA . . . . .	8-21
8.9.2.6 VPP . . . . .	8-21
8.9.2.7 VDDF, VSSF . . . . .	8-21
8.9.2.8 VDDH . . . . .	8-21
8.9.2.9 VDDSRAM . . . . .	8-21
8.9.2.10 VSS . . . . .	8-21
8.9.3 Keep Alive Power . . . . .	8-22
8.9.3.1 Keep Alive Power Configuration . . . . .	8-22
8.9.3.2 Keep Alive Power Registers Lock Mechanism . . . . .	8-23
8.10 VDDSRAM Supply Failure Detection . . . . .	8-25
8.11 Power Up/Down Sequencing . . . . .	8-25
8.12 Clocks Unit Programming Model . . . . .	8-29
8.12.1 System Clock Control Register (SCCR) . . . . .	8-30
8.12.2 PLL, Low-Power, and Reset-Control Register (PLPRCR) . . . . .	8-33

<b>Paragraph Number</b>	<b>Page Number</b>
8.12.3 Change of Lock Interrupt Register (COLIR) . . . . .	8-35
8.12.4 VDDSRAM Control Register (VSRMCR) . . . . .	8-36

## **Section 9 EXTERNAL BUS INTERFACE**

9.1 Features . . . . .	9-1
9.2 Bus Transfer Signals . . . . .	9-1
9.3 Bus Control Signals . . . . .	9-2
9.4 Bus Interface Signal Descriptions . . . . .	9-3
9.5 Bus Operations . . . . .	9-7
9.5.1 Basic Transfer Protocol . . . . .	9-8
9.5.2 Single Beat Transfer . . . . .	9-8
9.5.2.1 Single Beat Read Flow . . . . .	9-8
9.5.2.2 Single Beat Write Flow . . . . .	9-11
9.5.2.3 Single Beat Flow with Small Port Size . . . . .	9-14
9.5.3 Burst Transfer . . . . .	9-15
9.5.4 Burst Mechanism . . . . .	9-16
9.5.5 Alignment and Packaging of Transfers . . . . .	9-28
9.5.6 Arbitration Phase . . . . .	9-30
9.5.6.1 Bus Request . . . . .	9-31
9.5.6.2 Bus Grant . . . . .	9-32
9.5.6.3 Bus Busy . . . . .	9-32
9.5.6.4 Internal Bus Arbiter . . . . .	9-33
9.5.7 Address Transfer Phase Signals . . . . .	9-35
9.5.7.1 Transfer Start . . . . .	9-36
9.5.7.2 Address Bus . . . . .	9-36
9.5.7.3 Read/Write . . . . .	9-36
9.5.7.4 Burst Indicator . . . . .	9-36
9.5.7.5 Transfer Size . . . . .	9-37
9.5.7.6 Address Types . . . . .	9-37
9.5.7.7 Burst Data in Progress . . . . .	9-38
9.5.8 Termination Signals . . . . .	9-38
9.5.8.1 Transfer Acknowledge . . . . .	9-38
9.5.8.2 Burst Inhibit . . . . .	9-39
9.5.8.3 Transfer Error Acknowledge . . . . .	9-39
9.5.8.4 Termination Signals Protocol . . . . .	9-39
9.5.9 Storage Reservation . . . . .	9-40
9.5.10 Bus Exception Control Cycles . . . . .	9-43
9.5.10.1 Retrying a Bus Cycle . . . . .	9-43
9.5.10.2 Termination Signals Protocol Summary . . . . .	9-47
9.5.11 Bus Operation in External Master Modes . . . . .	9-47
9.5.12 Contention Resolution on External Bus . . . . .	9-52
9.5.13 Show Cycle Transactions . . . . .	9-54

**Section 10  
MEMORY CONTROLLER**

10.1 Overview .....	10-1
10.2 Memory Controller Architecture .....	10-3
10.2.1 Associated Registers .....	10-4
10.2.2 Port Size Configuration .....	10-5
10.2.3 Write-Protect Configuration .....	10-5
10.2.4 Address and Address Space Checking .....	10-5
10.2.5 Burst Support .....	10-5
10.3 Chip-Select Timing .....	10-6
10.3.1 Memory Devices Interface Example .....	10-7
10.3.2 Peripheral Devices Interface Example .....	10-8
10.3.3 Relaxed Timing Examples .....	10-10
10.3.4 Extended Hold Time on Read Accesses .....	10-14
10.3.5 Summary of GPCM Timing Options .....	10-18
10.4 Global (Boot) Chip-Select Operation .....	10-20
10.5 Write and Byte Enable Signals .....	10-21
10.6 Dual Mapping of the Internal Flash EEPROM Array .....	10-21
10.7 Memory Controller External Master Support .....	10-24
10.8 Programming Model .....	10-27
10.8.1 General Memory Controller Programming Notes .....	10-27
10.8.2 Memory Controller Status Registers (MSTAT) .....	10-28
10.8.3 Memory Controller Base Registers (BR0 – BR3) .....	10-28
10.8.4 Memory Controller Option Registers (OR0 – OR3) .....	10-30
10.8.5 Dual Mapping Base Register (DMBR) .....	10-31
10.8.6 Dual-Mapping Option Register .....	10-32

**Section 11  
L-BUS TO U-BUS INTERFACE (L2U)**

11.1 General Features .....	11-1
11.2 DMPU Features .....	11-1
11.3 L2U Block Diagram .....	11-2
11.4 Modes Of Operation .....	11-2
11.4.1 Normal Mode .....	11-3
11.4.2 Reset Operation .....	11-3
11.4.3 Factory Test Mode .....	11-3
11.4.4 Peripheral Mode .....	11-3
11.5 Data Memory Protection .....	11-4
11.5.1 Functional Description .....	11-4
11.5.2 Associated Registers .....	11-5
11.5.3 L-bus Memory Access Violations .....	11-7
11.6 Reservation Support .....	11-7
11.6.1 The Reservation Protocol .....	11-7

<b>Paragraph Number</b>	<b>Page Number</b>
11.6.2 L2U Reservation Support . . . . .	11-7
11.6.3 Reserved Location (Bus) and Possible Actions . . . . .	11-8
11.7 L-Bus Show Cycle Support . . . . .	11-9
11.7.1 Programming Show Cycles . . . . .	11-9
11.7.2 Performance Impact . . . . .	11-9
11.7.3 Show Cycle Protocol . . . . .	11-10
11.7.4 L-Bus Write Show Cycle Flow . . . . .	11-10
11.7.5 L-Bus Read Show Cycle Flow . . . . .	11-11
11.7.6 Show Cycle Support Guidelines . . . . .	11-11
11.8 L2U Programming Model . . . . .	11-12
11.8.1 U-bus Access . . . . .	11-13
11.8.2 Transaction Size . . . . .	11-13
11.8.3 L2U Module Configuration Register (L2U_MCR) . . . . .	11-13
11.8.4 Region Base Address Registers (L2U_RBAX) . . . . .	11-14
11.8.5 Region Attribute Registers (L2U_RAX) . . . . .	11-15
11.8.6 Global Region Attribute Register . . . . .	11-15

## **Section 12**

### **U-BUS TO IMB3 BUS INTERFACE (UIMB)**

12.1 Features . . . . .	12-1
12.2 UIMB Block Diagram . . . . .	12-2
12.3 Clock Module . . . . .	12-2
12.4 Interrupt Operation . . . . .	12-3
12.4.1 Interrupt Sources and Levels on IMB . . . . .	12-4
12.4.2 IMB Interrupt Multiplexing . . . . .	12-4
12.4.3 ILBS Sequencing . . . . .	12-4
12.4.4 Interrupt Synchronizer . . . . .	12-6
12.5 Programming Model . . . . .	12-7
12.5.1 UIMB Module Configuration Register (UMCR) . . . . .	12-7
12.5.2 Test control register (UTSTCREG) . . . . .	12-8
12.5.3 Pending Interrupt Request Register (UIPEND) . . . . .	12-8

## **Section 13**

### **QUEUED ANALOG-TO-DIGITAL CONVERTER MODULE-64**

13.1 Overview . . . . .	13-1
13.2 Features . . . . .	13-2
13.3 QADC64 Pin Functions . . . . .	13-2
13.3.1 Port A Pin Functions . . . . .	13-3
13.3.1.1 Port A Analog Input Pins . . . . .	13-3
13.3.1.2 Port A Digital Input/Output Pins . . . . .	13-3
13.3.2 Port B Pin Functions . . . . .	13-4
13.3.2.1 Port B Analog Input Pins . . . . .	13-4
13.3.2.2 Port B Digital Input Pins . . . . .	13-4
13.3.3 External Trigger Input Pins . . . . .	13-4



<b>Paragraph Number</b>	<b>Page Number</b>
13.3.4 Multiplexed Address Output Pins . . . . .	13-4
13.3.5 Multiplexed Analog Input Pins . . . . .	13-5
13.3.6 Voltage Reference Pins . . . . .	13-5
13.3.7 Dedicated Analog Supply Pins . . . . .	13-5
13.3.8 External Digital Supply Pin . . . . .	13-5
13.3.9 Digital Supply Pins . . . . .	13-5
13.4 QADC64 Bus Interface . . . . .	13-6
13.5 Module Configuration . . . . .	13-6
13.5.1 Low-Power Stop Mode . . . . .	13-6
13.5.2 Freeze Mode . . . . .	13-6
13.5.3 Supervisor/Unrestricted Address Space . . . . .	13-7
13.6 General-Purpose I/O Port Operation . . . . .	13-7
13.6.1 Port Data Register . . . . .	13-8
13.6.2 Port Data Direction Register . . . . .	13-8
13.7 External Multiplexing Operation . . . . .	13-9
13.8 Analog Input Channels . . . . .	13-10
13.9 Analog Subsystem . . . . .	13-11
13.9.1 Conversion Cycle Times . . . . .	13-12
13.9.1.1 Amplifier Bypass Mode Conversion Timing . . . . .	13-13
13.9.2 Front-End Analog Multiplexer . . . . .	13-14
13.9.3 Digital-to-Analog Converter Array . . . . .	13-14
13.9.4 Comparator . . . . .	13-14
13.9.5 Successive Approximation Register . . . . .	13-14
13.10 Digital Control Subsystem . . . . .	13-14
13.10.1 Queue Priority . . . . .	13-15
13.10.2 Queue Boundary Conditions . . . . .	13-17
13.10.3 Scan Modes . . . . .	13-18
13.10.3.1 Disabled Mode . . . . .	13-18
13.10.3.2 Reserved Mode . . . . .	13-18
13.10.3.3 Single-Scan Modes . . . . .	13-18
13.10.3.4 Continuous-Scan Modes . . . . .	13-21
13.10.4 QADC64 Clock (QCLK) Generation . . . . .	13-24
13.10.5 Periodic/Interval Timer . . . . .	13-29
13.11 Interrupts . . . . .	13-29
13.11.1 Interrupt Sources . . . . .	13-30
13.11.2 Interrupt Register . . . . .	13-31
13.11.3 Interrupt Levels and Time Multiplexing . . . . .	13-31
13.12 Programming Model . . . . .	13-31
13.12.1 QADC64 Module Configuration Register . . . . .	13-33
13.12.2 QADC64 Test Register . . . . .	13-33
13.12.3 QADC64 Interrupt Register . . . . .	13-33
13.12.4 Port A/B Data Register . . . . .	13-34
13.12.5 Port Data Direction Register . . . . .	13-35

<b>Paragraph Number</b>	<b>Page Number</b>
13.12.6 QADC64 Control Register 0 (QACR0) .....	13-35
13.12.7 QADC64 Control Register 1 (QACR1) .....	13-36
13.12.8 QADC64 Control Register 2 (QACR2) .....	13-38
13.12.9 QADC64 Status Register 0 (QASR0) .....	13-40
13.12.10 QADC64 Status Register 1 (QASR1) .....	13-42
13.12.11 Conversion Command Word Table .....	13-43
13.12.12 Result Word Table .....	13-49

## **Section 14**

### **QUEUED SERIAL MULTI-CHANNEL MODULE**

14.1 Overview .....	14-1
14.2 Block Diagram .....	14-1
14.3 Signal Descriptions .....	14-2
14.4 Memory Map .....	14-2
14.5 QSMCM Global Registers .....	14-4
14.5.1 Low-Power Stop Operation .....	14-5
14.5.2 Freeze Operation .....	14-5
14.5.3 Access Protection .....	14-5
14.5.4 QSMCM Interrupts .....	14-6
14.5.5 QSMCM Configuration Register (QSMCMMCR) .....	14-7
14.5.6 QSMCM Test Register (QTEST) .....	14-8
14.5.7 QSMCM Interrupt Level Registers (QDSCI_IL, QSPI_IL) .....	14-8
14.6 QSMCM Pin Control Registers .....	14-9
14.6.1 Port QS Data Register (PORTQS) .....	14-10
14.6.2 PORTQS Pin Assignment Register (PQSPAR) .....	14-11
14.6.3 PORTQS Data Direction Register (DDRQS) .....	14-12
14.7 Queued Serial Peripheral Interface .....	14-13
14.7.1 QSPI Registers .....	14-15
14.7.1.1 QSPI Control Register 0 .....	14-16
14.7.1.2 QSPI Control Register 1 .....	14-18
14.7.1.3 QSPI Control Register 2 .....	14-18
14.7.1.4 QSPI Control Register 3 .....	14-19
14.7.1.5 QSPI Status Register .....	14-20
14.7.2 QSPI RAM .....	14-21
14.7.2.1 Receive RAM .....	14-22
14.7.2.2 Transmit RAM .....	14-22
14.7.2.3 Command RAM .....	14-22
14.7.3 QSPI Pins .....	14-23
14.7.4 QSPI Operation .....	14-24
14.7.4.1 Enabling, Disabling, and Halting the SPI .....	14-25
14.7.4.2 QSPI Interrupts .....	14-26
14.7.4.3 QSPI Flow .....	14-26
14.7.5 Master Mode Operation .....	14-33

<b>Paragraph Number</b>	<b>Page Number</b>
14.7.5.1 Clock Phase and Polarity .....	14-34
14.7.5.2 Baud Rate Selection .....	14-34
14.7.5.3 Delay Before Transfer .....	14-35
14.7.5.4 Delay After Transfer .....	14-35
14.7.5.5 Transfer Length .....	14-36
14.7.5.6 Peripheral Chip Selects .....	14-36
14.7.5.7 Master Wraparound Mode .....	14-37
14.7.6 Slave Mode .....	14-37
14.7.6.1 Description of Slave Operation .....	14-39
14.7.7 Slave Wraparound Mode .....	14-40
14.7.8 Mode Fault .....	14-41
14.8 Serial Communication Interface .....	14-41
14.8.1 SCI Registers .....	14-44
14.8.2 SCI Control Register 0 .....	14-45
14.8.3 SCI Control Register 1 .....	14-45
14.8.4 SCI Status Register (SCxSR) .....	14-47
14.8.5 SCI Data Register (SCxDR) .....	14-49
14.8.6 SCI Pins .....	14-50
14.8.7 SCI Operation .....	14-50
14.8.7.1 Definition of Terms .....	14-50
14.8.7.2 Serial Formats .....	14-51
14.8.7.3 Baud Clock .....	14-51
14.8.7.4 Parity Checking .....	14-52
14.8.7.5 Transmitter Operation .....	14-52
14.8.7.6 Receiver Operation .....	14-54
14.8.7.7 Receiver Functional Operation .....	14-56
14.8.7.8 Idle-Line Detection .....	14-57
14.8.7.9 Receiver Wake-Up .....	14-58
14.8.7.10 Internal Loop Mode .....	14-58
14.9 SCI Queue Operation .....	14-58
14.9.1 Queue Operation of SCI1 for Transmit and Receive .....	14-58
14.9.2 Queued SCI1 Status and Control Registers .....	14-59
14.9.2.1 QSCI1 Control Register .....	14-59
14.9.2.2 QSCI1 Status Register .....	14-61
14.9.3 QSCI1 Transmitter Block Diagram .....	14-61
14.9.4 QSCI1 Additional Transmit Operation Features .....	14-62
14.9.5 QSCI1 Transmit Flow Chart Implementing the Queue .....	14-64
14.9.6 Example QSCI1 Transmit for 17 Data Bytes .....	14-66
14.9.7 Example SCI Transmit for 25 Data Bytes .....	14-67
14.9.8 QSCI1 Receiver Block Diagram .....	14-68
14.9.9 QSCI1 Additional Receive Operation Features .....	14-68
14.9.10 QSCI1 Receive Flow Chart Implementing The Queue .....	14-71
14.9.11 QSCI1 Receive Queue Software Flow Chart .....	14-72

14.9.12 Example QSCI1 Receive Operation of 17 Data Frames ..... 14-73

**Section 15**

**MODULAR INPUT/OUTPUT SUBSYSTEM (MIOS1)**

15.1 MIOS1 Features ..... 15-1

15.2 Submodule Numbering, Naming and Addressing ..... 15-3

15.3 MIOS1 Signals ..... 15-3

15.4 Block Diagram ..... 15-4

15.5 MIOS1 Bus System ..... 15-6

    15.5.1 Read/Write and Control Bus ..... 15-6

    15.5.2 Request Bus ..... 15-6

    15.5.3 Counter Bus Set ..... 15-6

15.6 MIOS1 Programmer's Model ..... 15-6

15.7 MIOS1 I/O Ports ..... 15-8

15.8 MIOS Bus Interface Submodule (MBISM) ..... 15-8

    15.8.1 MIOS Bus Interface (MBISM) Registers ..... 15-8

        15.8.1.1 MIOS1 Test and Pin Control Register ..... 15-8

        15.8.1.2 MIOS1 Vector Register ..... 15-9

        15.8.1.3 MIOS1 Module and Version Number Register ..... 15-9

        15.8.1.4 MIOS1 Module Configuration Register ..... 15-9

    15.8.2 MBISM Interrupt Registers ..... 15-10

        15.8.2.1 MIOS1 Interrupt Level Register 0 (MIOS1LVL0) ..... 15-10

        15.8.2.2 MIOS1 Interrupt Level Register 1 (MIOS1LVL1) ..... 15-11

    15.8.3 Interrupt Control Section (ICS) ..... 15-11

15.9 MIOS Counter Prescaler Submodule (MCPSM) ..... 15-12

    15.9.1 MIOS Counter Prescaler Submodule (MCPSM) Registers ..... 15-12

        15.9.1.1 MCPSM Status/Control Register (MCPSMCSM) ..... 15-13

15.10 MIOS Modulus Counter Submodule (MMCSM) ..... 15-13

    15.10.1 MIOS Modulus Counter Submodule (MMCSM) Registers ..... 15-15

        15.10.1.1 MMCSM Up-Counter Register (MMCSM CNT) ..... 15-16

        15.10.1.2 MMCSM Modulus Latch Register (MMCSM ML) ..... 15-16

        15.10.1.3 MMCSM Status/Control Register (Duplicated) ..... 15-16

        15.10.1.4 MMCSM Status/Control Register (MMCSM SCR) ..... 15-17

15.11 MIOS Double Action Submodule (MDASM) ..... 15-18

    15.11.1 MIOS Double Action Submodule (MDASM) Registers ..... 15-19

        15.11.1.1 MDASM Data A Register ..... 15-21

        15.11.1.2 MDASM Data B Register (MDASM BR) ..... 15-21

        15.11.1.3 MDASM Status/Control Register (Duplicated) ..... 15-22

        15.11.1.4 MDASM Status/Control Register ..... 15-23

15.12 MIOS Pulse Width Modulation Submodule (MPWMSM) ..... 15-25

    15.12.1 MIOS Pulse Width Modulation Submodule (MPWMSM) Registers ..... 15-26

        15.12.1.1 MPWMSM Period Register (MPWMSM PER) ..... 15-27

        15.12.1.2 MPWMSM Pulse Width Register (MPWMSM PUL) ..... 15-27

<b>Paragraph Number</b>	<b>Page Number</b>
15.12.1.3 MPWMSM Counter Register (MPWMSMCNTR) . . . . .	15-28
15.12.1.4 MPWMSM Status/Control Register(MPWMSMCR) . . . . .	15-28
15.13 MIOS 16-bit Parallel Port I/O Submodule (MPIOISM) . . . . .	15-30
15.13.1 MIOS 16-bit Parallel Port I/O Submodule (MPIOISM) Registers. . . . .	15-30
15.13.1.1 MPIOISM Data Register (MPIOISMDR). . . . .	15-30
15.13.1.2 MPIOISM Data Direction Register (MPIOISMDDR). . . . .	15-31
15.14 MIOS1 Interrupts . . . . .	15-31
15.14.1 MIOS Interrupt Request Submodule (MIRSM) . . . . .	15-32
15.14.2 MIOS Interrupt Request Submodule 0 (MIRSM0) Registers . . . . .	15-33
15.14.2.1 MIRSM0 Interrupt Status Register (MIOS1SR0) . . . . .	15-34
15.14.2.2 MIRSM0 Interrupt Enable Register (MIOS1ER0). . . . .	15-35
15.14.2.3 MIRSM0 Request Pending Register (MIOS1RPR0) . . . . .	15-35
15.14.3 MIOS Interrupt Request Submodule 1 (MIRSM1) Registers . . . . .	15-36
15.14.3.1 MIRSM1 Interrupt Status Register (MIOS1SR1) . . . . .	15-36
15.14.3.2 MIRSM1 Interrupt Enable Register (MIOS1ER1). . . . .	15-37
15.14.3.3 MIRSM1 Request Pending Register (MIOS1RPR1) . . . . .	15-37
15.15 MIOS1 Function Examples . . . . .	15-38
15.15.1 MIOS1 Input Double Edge Pulse Width Measurement . . . . .	15-38
15.15.2 MIOS1 Input Double Edge Period Measurement . . . . .	15-40
15.15.3 MIOS1 Double Edge Single Output Pulse Generation. . . . .	15-41
15.15.4 MIOS1 Output Pulse Width Modulation With MDASM . . . . .	15-42
15.15.5 MIOS1 Input Pulse Accumulation. . . . .	15-43
15.16 MIOS1 Configuration . . . . .	15-43

## **Section 16**

### **CAN 2.0B CONTROLLER MODULE**

16.1 Features. . . . .	16-1
16.2 External Pins . . . . .	16-2
16.3 TouCAN Architecture . . . . .	16-3
16.3.1 TX/RX Message Buffer Structure . . . . .	16-3
16.3.1.1 Common Fields for Extended and Standard Format Frames. . . . .	16-4
16.3.1.2 Fields for Extended Format Frames . . . . .	16-6
16.3.1.3 Fields for Standard Format Frames . . . . .	16-6
16.3.1.4 Serial Message Buffers . . . . .	16-6
16.3.1.5 Message Buffer Activation/Deactivation Mechanism . . . . .	16-7
16.3.1.6 Message Buffer Lock/Release/Busy Mechanism . . . . .	16-7
16.3.2 Receive Mask Registers . . . . .	16-7
16.3.3 Bit Timing . . . . .	16-8
16.3.3.1 Configuring the TouCAN Bit Timing . . . . .	16-9
16.3.4 Error Counters . . . . .	16-9
16.3.5 Time Stamp . . . . .	16-10
16.4 TouCAN Operation. . . . .	16-11
16.4.1 TouCAN Reset . . . . .	16-11

<b>Paragraph Number</b>	<b>Page Number</b>
16.4.2 TouCAN Initialization .....	16-11
16.4.3 Transmit Process .....	16-12
16.4.3.1 Transmit Message Buffer Deactivation .....	16-13
16.4.3.2 Reception of Transmitted Frames .....	16-13
16.4.4 Receive Process .....	16-13
16.4.4.1 Receive Message Buffer Deactivation .....	16-14
16.4.4.2 Locking and Releasing Message Buffers .....	16-15
16.4.5 Remote Frames .....	16-15
16.4.6 Overload Frames .....	16-16
16.5 Special Operating Modes .....	16-16
16.5.1 Debug Mode .....	16-16
16.5.2 Low-Power Stop Mode .....	16-17
16.5.3 Auto Power Save Mode .....	16-18
16.6 Interrupts .....	16-19
16.7 Programmer's Model .....	16-20
16.7.1 TouCAN Module Configuration Register .....	16-22
16.7.2 TouCAN Test Configuration Register .....	16-24
16.7.3 TouCAN Interrupt Configuration Register .....	16-24
16.7.4 Control Register 0 .....	16-25
16.7.5 Control Register 1 .....	16-26
16.7.6 Prescaler Divide Register .....	16-27
16.7.7 Control Register 2 .....	16-28
16.7.8 Free Running Timer .....	16-29
16.7.9 Receive Global Mask Registers .....	16-29
16.7.10 Receive Buffer 14 Mask Registers .....	16-30
16.7.11 Receive Buffer 15 Mask Registers .....	16-30
16.7.12 Error and Status Register .....	16-30
16.7.13 Interrupt Mask Register .....	16-32
16.7.14 Interrupt Flag Register .....	16-33
16.7.15 Error Counters .....	16-33

## **Section 17**

### **TIME PROCESSOR UNIT 3**

17.1 Overview .....	17-1
17.2 TPU3 Components .....	17-2
17.2.1 Time Bases .....	17-2
17.2.2 Timer Channels .....	17-2
17.2.3 Scheduler .....	17-2
17.2.4 Microengine .....	17-2
17.2.5 Host Interface .....	17-3
17.2.6 Parameter RAM .....	17-3
17.3 TPU Operation .....	17-3
17.3.1 Event Timing .....	17-3

<b>Paragraph Number</b>	<b>Page Number</b>
17.3.2 Channel Orthogonality . . . . .	17-3
17.3.3 Interchannel Communication . . . . .	17-4
17.3.4 Programmable Channel Service Priority . . . . .	17-4
17.3.5 Coherency . . . . .	17-4
17.3.6 Emulation Support . . . . .	17-4
17.3.7 TPU3 Interrupts . . . . .	17-5
17.3.8 Prescaler Control for TCR1 . . . . .	17-5
17.3.9 Prescaler Control for TCR2 . . . . .	17-7
17.4 Programming Model. . . . .	17-8
17.4.1 TPU Module Configuration Register. . . . .	17-10
17.4.2 TPU3 Test Configuration Register . . . . .	17-12
17.4.3 Development Support Control Register . . . . .	17-12
17.4.4 Development Support Status Register . . . . .	17-14
17.4.5 TPU3 Interrupt Configuration Register . . . . .	17-14
17.4.6 Channel Interrupt Enable Register . . . . .	17-15
17.4.7 Channel Function Select Registers . . . . .	17-15
17.4.8 Host Sequence Registers . . . . .	17-16
17.4.9 Host Service Request Registers. . . . .	17-17
17.4.10 Channel Priority Registers . . . . .	17-18
17.4.11 Channel Interrupt Status Register . . . . .	17-19
17.4.12 Link Register. . . . .	17-19
17.4.13 Service Grant Latch Register . . . . .	17-19
17.4.14 Decoded Channel Number Register. . . . .	17-19
17.4.15 TPU3 Module Configuration Register 2 . . . . .	17-20
17.4.16 TPU Module Configuration Register 3 . . . . .	17-21
17.4.17 TPU3 Test Registers . . . . .	17-22
17.4.18 TPU3 Parameter RAM . . . . .	17-22
17.5 Time Functions. . . . .	17-23

## **Section 18**

### **DUAL-PORT TPU RAM (DPTRAM)**

18.1 Features. . . . .	18-1
18.2 DPTRAM Configuration and Block Diagram . . . . .	18-2
18.3 Programming Model. . . . .	18-2
18.3.1 DPTRAM Module Configuration Register (DPTMCR) . . . . .	18-3
18.3.2 DPTRAM Test Register . . . . .	18-4
18.3.3 Ram Base Address Register (RAMBAR) . . . . .	18-5
18.3.4 MISR High (MISRH) and MISR Low (MISRL) . . . . .	18-5
18.3.5 MISC Counter (MISCNT) . . . . .	18-6
18.4 Operation . . . . .	18-6
18.4.1 Normal Operation . . . . .	18-6
18.4.2 Standby Operation . . . . .	18-6
18.4.3 Reset Operation . . . . .	18-7

<b>Paragraph Number</b>	<b>Page Number</b>
18.4.4 Stop Operation .....	18-7
18.4.5 Freeze Operation .....	18-8
18.4.6 TPU3 Emulation Mode Operation.....	18-8
18.5 Multiple Input Signature Calculator (MISC) .....	18-8

## **Section 19**

### **CDR MoneT FLASH EEPROM**

19.1 Introduction .....	19-1
19.1.1 MPC555 / MPC556 CMF Features.....	19-2
19.1.2 Glossary of Terms for the CMF EEPROM .....	19-2
19.2 Programming Model.....	19-4
19.2.1 CMF EEPROM Control Registers .....	19-4
19.2.1.1 CMF EEPROM Configuration Register (CMFMCR).....	19-5
19.2.1.2 CMF EEPROM Test Register (CMFTST).....	19-7
19.2.1.3 CMF EEPROM High Voltage Control Register (CMFCTL).....	19-9
19.2.2 CMF EEPROM Array Addressing.....	19-11
19.2.2.1 Read Page Buffers .....	19-12
19.2.2.2 Program Page Buffers .....	19-13
19.2.2.3 Array Configuration for CMF Module A .....	19-14
19.2.2.4 Array Configuration for CMF Module B .....	19-15
19.3 Shadow Information.....	19-15
19.3.1 Address Range of Shadow Information .....	19-16
19.3.2 Reset Configuration Word (CMFCFIG) .....	19-16
19.4 Array Read Operation .....	19-17
19.5 Programming the CMF Array .....	19-18
19.5.1 Program Sequence.....	19-18
19.5.2 Program Margin Reads .....	19-22
19.5.3 Over-Programming.....	19-23
19.6 Erasing CMF Array Blocks.....	19-23
19.6.1 Erase Sequence.....	19-23
19.6.2 Erase Margin Reads.....	19-26
19.6.3 Erasing Shadow Information Words.....	19-26
19.7 Voltage Control for Programming and Erasing .....	19-27
19.7.1 Pulse Status .....	19-27
19.7.2 Pulse Width Timing Equation .....	19-27
19.7.3 System Clock Scaling.....	19-28
19.7.4 Exponential Clock Multiplier .....	19-29
19.7.5 Linear Clock Multiplier .....	19-29
19.7.6 A Technique to Determine SCLKR, CLKPE, and CLKPM .....	19-29
19.7.7 Starting and Ending a Program or Erase Sequence .....	19-30
19.7.8 Controlling the Program/Erase Voltage .....	19-31
19.8 Censored and Non-Censored Accesses .....	19-31
19.8.1 Uncensored Mode .....	19-31



<b>Paragraph Number</b>	<b>Page Number</b>
19.8.2 Censored Mode .....	19-31
19.8.3 Device Modes and Censorship Status .....	19-32
19.8.4 Setting and Clearing Censor .....	19-33
19.8.5 Switching the CMF EEPROM Censorship .....	19-35
19.9 Pin Descriptions .....	19-36
19.9.1 E <sub>PEE</sub> Signal .....	19-36
19.9.2 FLASH Program/Erase Voltage Conditioning .....	19-37
19.10 Reset Operation .....	19-39
19.10.1 Master Reset .....	19-39
19.10.2 Soft Reset .....	19-39
19.10.3 Emulation Operation .....	19-40
19.11 Disabling the CMF Module .....	19-40

## **Section 20 STATIC RANDOM ACCESS MEMORY (SRAM)**

20.1 Features .....	20-1
20.2 Block Diagram .....	20-1
20.3 Programming Model .....	20-2
20.3.1 SRAM Module Configuration Register (SRAMMCR) .....	20-2
20.3.2 <b>SRAM Test Register (SRAMTST)</b> .....	20-3

## **Section 21 DEVELOPMENT SUPPORT**

21.1 Overview .....	21-1
21.2 Program Flow Tracking .....	21-1
21.2.1 Program Trace Cycle .....	21-2
21.2.1.1 Instruction Queue Status Pins — VF [0:2] .....	21-3
21.2.1.2 History Buffer Flushes Status Pins— VFLS [0..1] .....	21-4
21.2.1.3 Queue Flush Information Special Case .....	21-4
21.2.2 Program Trace when in Debug Mode .....	21-4
21.2.3 Sequential Instructions Marked as Indirect Branch .....	21-5
21.2.4 The External Hardware .....	21-5
21.2.4.1 Synchronizing the Trace Window to the CPU Internal Events .....	21-5
21.2.4.2 Detecting the Trace Window Start Address .....	21-6
21.2.4.3 Detecting the Assertion/Negation of VSYNC .....	21-7
21.2.4.4 Detecting the Trace Window End Address .....	21-7
21.2.4.5 Compress .....	21-7
21.2.5 Instruction Fetch Show Cycle Control .....	21-8
21.3 Watchpoints and Breakpoints Support .....	21-8
21.3.1 Internal Watchpoints and Breakpoints .....	21-11
21.3.1.1 Restrictions .....	21-13
21.3.1.2 Byte and Half-Word Working Modes .....	21-13
21.3.1.3 Examples .....	21-14
21.3.1.4 Context Dependent Filter .....	21-15

<b>Paragraph Number</b>	<b>Page Number</b>
21.3.1.5 Ignore First Match . . . . .	21-15
21.3.1.6 Generating Six Compare Types . . . . .	21-16
21.3.2 Instruction Support . . . . .	21-16
21.3.2.1 Load/Store Support . . . . .	21-17
21.3.3 Watchpoint Counters . . . . .	21-21
21.3.3.1 Trap Enable Programming . . . . .	21-21
21.4 Development System Interface . . . . .	21-21
21.4.1 Debug Mode Support . . . . .	21-24
21.4.1.1 Debug Mode Enable vs. Debug Mode Disable . . . . .	21-26
21.4.1.2 Entering Debug Mode . . . . .	21-26
21.4.1.3 The Check Stop State and Debug Mode . . . . .	21-29
21.4.1.4 Saving Machine State upon Entering Debug Mode . . . . .	21-29
21.4.1.5 Running in Debug Mode . . . . .	21-30
21.4.1.6 Exiting Debug Mode . . . . .	21-30
21.5 Development Port . . . . .	21-31
21.5.1 Development Port Pins . . . . .	21-31
21.5.2 Development Serial Clock . . . . .	21-31
21.5.3 Development Serial Data In . . . . .	21-31
21.5.4 Development Serial Data Out . . . . .	21-32
21.5.5 Freeze Signal . . . . .	21-32
21.5.5.1 SGPIO6/FRZ/ $\overline{\text{PTR}}$ Pin . . . . .	21-32
21.5.5.2 IWP[0:1]/VFLS[0:1] Pins . . . . .	21-32
21.5.5.3 VFLS[0:1]_MPIO32B[3:4] Pins . . . . .	21-32
21.5.6 Development Port Registers . . . . .	21-32
21.5.6.1 Development Port Shift Register . . . . .	21-33
21.5.6.2 Trap Enable Control Register . . . . .	21-33
21.5.6.3 Development Port Registers Decode . . . . .	21-33
21.5.6.4 Development Port Serial Communications — Clock Mode Selection . . . . .	21-34
21.5.6.5 Development Port Serial Communications — Trap Enable Mode . . . . .	21-38
21.5.6.6 Serial Data into Development Port — Trap Enable Mode . . . . .	21-38
21.5.6.7 Serial Data Out of Development Port — Trap Enable Mode . . . . .	21-39
21.5.6.8 Development Port Serial Communications — Debug Mode . . . . .	21-39
21.5.6.9 Serial Data Into Development Port . . . . .	21-40
21.5.6.10 Serial Data Out of Development Port . . . . .	21-41
21.5.6.11 Fast Download Procedure . . . . .	21-41
21.6 Software Monitor Debugger Support . . . . .	21-43
21.6.1 Freeze Indication . . . . .	21-43
21.7 Development Support Registers . . . . .	21-43
21.7.1 Register Protection . . . . .	21-44
21.7.2 Comparator A–D Value Registers (CMPA–CMPD) . . . . .	21-45
21.7.3 Comparator E–F Value Registers . . . . .	21-46
21.7.4 Breakpoint Address Register (BAR) . . . . .	21-46
21.7.5 Comparator G–H Value Registers (CMPG–CMPH) . . . . .	21-46