

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China









Product Brief

MPC555PB/D Rev. 3, 2/2003

MPC555 Product Brief

This document provides an overview of the MPC555 microcontroller, including a block diagram showing the major modular components and sections that list the major features. The MPC555 member of the Freescale MPC500 RISC Microcontroller family.

Table 1. MPC555 Features

Device	Flash	Code Compression
MPC555	448 Kbytes	Code compression not supported

1 Introduction

The MPC555 device offers the following features:

- PowerPCTM core with floating-point unit
- 26 Kbytes fast RAM and 6 Kbytes TPU microcode RAM
- 448 Kbytes Flash EEPROM with 5-V programming
- 5-V I/O system
- Serial system: queued serial multi-channel module (QSMCM), dual CAN 2.0B controller modules (TouCANTM)
- 50-channel timer system: dual time processor units (TPU3), modular I/O system (MIOS1)
- 32 analog inputs: dual queued analog-to-digital converters (QADC64)
- Submicron HCMOS (CDR1) technology
- 272-pin plastic ball grid array (PBGA) packaging
- 40-MHz operation, -40 °C to 125 °C with dual supply (3.3 V, 5 V) (-55 °C to 125 °C for the suffix A device)
- 32-bit architecture (PowerPC ISA architecture compliant)
- Core performance measured at 52.7-Kbyte Dhrystones (v2.1) @ 40 MHz
- Fully static, low power operation
- Integrated double-precision floating-point unit
- Precise exception model





- 3lock Diagram
 - Extensive system development support
 - On-chip watchpoints and breakpoints
 - Program flow tracking
 - BDM on-chip emulation development interface

1.1 Block Diagram

Figure 1 is a block diagram of the MPC555.

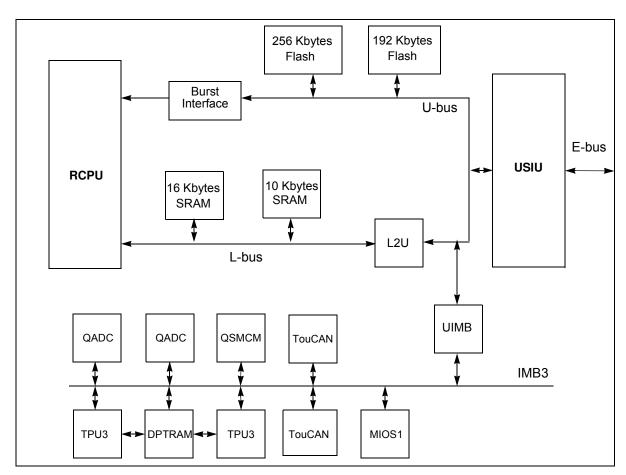


Figure 1. MPC555 Block Diagram

1.2 Key Features

The MPC555 key features are explained in the following sections.

1.2.1 Four-Bank Memory Controller

- Works with SRAM, EPROM, Flash EEPROM, and other peripherals
- Byte write enables
- 32-bit address decodes with bit masks



1.2.2 U-Bus System Interface Unit (USIU)

- Clock synthesizer
- Power management
- Reset controller
- MPC555 decrementer and time base
- Real-time clock register
- Periodic interrupt timer
- Hardware bus monitor and software watchdog timer
- Interrupt controller that supports up to eight external and eight internal interrupts
- IEEE 1149.1 JTAG test access port
- External bus interface
 - 24 address pins, 32 data pins
 - Supports multiple master designs
 - Four-beat transfer bursts, two-clock minimum bus transactions
 - Supports 5V inputs, provides 3.3-V outputs

1.2.3 Flexible Memory Protection Unit

- Four instruction regions and four data regions
- 4-Kbyte to 16-Mbyte region size support
- Default attributes available in one global entry
- Attribute support for speculative accesses

1.2.4 448-Kbyte Flash EEPROM Memory

- One 256-Kbyte and one 192-Kbyte module
- Page read mode
- Block (32-Kbyte) erasable
- External 4.75-V to 5.25-V program and erase power supply

1.2.5 26-Kbytes of Static RAM

- One 16-Kbyte and one 10-Kbyte module
- Fast (one-clock) access
- Keep-alive power
- Soft defect detection (SDD)

1.2.6 General-Purpose I/O Support

- Address (24) and data (32) pins can be used for general-purpose I/O in single-chip mode
- Nine general-purpose I/O pins in MIOS1 unit
- Many peripheral pins can be used for general-purpose I/O when not used for primary function
- 5-V tolerant inputs/outputs



1.2.7 Two Time Processor Units (TPU3)

- Each TPU3 module provides these features:
 - A dedicated micro-engine operates independently of the RCPU
 - 16 independent programmable channels and pins
 - Each channel has an event register consisting of a 16-bit capture register, a 16-bit compare register and a 16-bit comparator
 - Nine pre-programmed timer functions are available
 - Any channel can perform any time function
 - Each timer function can be assigned to more than one channel
 - Two timer count registers with programmable prescalers
 - Each channel can be synchronized to one or both counters
 - Selectable channel priority levels
 - 5-V tolerant inputs/outputs
- 6-Kbyte dual port TPU RAM (DPTRAM) is shared by the two TPU3 modules for TPU microcode

1.2.8 18-Channel Modular I/O System (MIOS1)

- Ten double action submodules (DASM)
- Eight dedicated PWM sub-modules (PWMSM)
- Two 16-bit modulus counter submodules (MCSM)
- Two parallel port I/O submodules (PIOSM)
- 5-V tolerant inputs/outputs

1.2.9 Two Queued Analog-to-Digital Converter Modules (QADC64)

Each QADC provides:

- Up to 16 analog input channels, using internal multiplexing
- Up to 41 total input channels, using internal and external multiplexing
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of 10 µs (100,000 samples per second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
 - External edge trigger/level gate
 - Software command
- 64 result registers
- Output data that is right- or left-justified, signed or unsigned
- 5-V reference and range



1.2.10 Two CAN 2.0B Controller Modules (TouCAN)

Each TouCAN provides these features:

- Full implementation of CAN protocol specification, version 2.0A and 2.0B
- Each module has 16 receive/transmit message buffers of 0 to 8 bytes data length
- Global mask register for message buffers 0 to 13
- Independent mask registers for message buffers 14 and 15
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- 16-bit free-running timer for message time-stamping
- Low power sleep mode with programmable wake-up on bus activity
- Programmable I/O modes
- Maskable interrupts
- Independent of the transmission medium (external transceiver is assumed)
- Open network architecture
- Multimaster concept
- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode with programmable wakeup on bus activity

1.2.11 Queued Serial Multi-Channel Module (QSMCM)

- Queued serial peripheral interface (QSPI)
 - Provides full-duplex communication port for peripheral expansion or interprocessor communication
 - Up to 32 preprogrammed transfers, reducing overhead
 - 160-byte queue buffer
 - Programmable transfer length: from 8 to 16 bits, inclusive
 - Synchronous interface with baud rate of up to system clock divided by 4
 - Four programmable peripheral-select pins support up to 16 devices
 - Wrap-around mode allows continuous sampling for efficient interfacing to serial peripherals (e.g., serial A/D converters, I/O latches, etc.)
- Two serial communications interfaces (SCI). Each SCI offers these features:
 - UART mode provides NRZ format and half-or full-duplex interface
 - 16 register receive buffer and 16 register transmit buffer (SCI1 only)
 - Advanced error detection and optional parity generation and detection
 - Word length programmable as 8 or 9 bits
 - Separate transmitter and receiver enable bits and double buffering of data
 - Wakeup functions allow the CPU to run uninterrupted until either a true idle line is detected or a new address byte is received
 - External source clock for baud generation
 - Multiplexing of transmit data pins with discrete outputs and receive data pins with discrete inputs, allowing realization of a low-speed serial protocol



2 MPC555 Address Map

The internal memory map is shown in Figure 2.

_		
0x00 0000	CMF Flash A	
	256 Kbytes	
0x04 0000	CME Floor D	
	CMF Flash B	
0x06 FFFF	192 Kbytes	
0x07 0000		
	Reserved for Flash	
	(2.6 Mbytes - 16 Kbytes)	
0x2F BFFF		1
0x2F C000	USIU & Flash Control	I
0x2F FFFF	16 Kbytes	
0x30 0000		+
0.30 0000	UIMB Interface &	
	IMB3 Modules	
	(32 Kbytes)	
000 7555	,	
0x30 7FFF		-
0x30 8000		
	Reserved for IMB3	
	(480 Kbytes)	
	(100 110)100)	
0x37 FFFF		
0x38 0000		1
	SRAM ControlA	
	(8 bytes)	
0x38 0008	SRAM ControlB	1
	(8 bytes)	
0x38 0010		Ī
	Reserved	
	(485.98 Kbytes)	
	•	
0x3F 9800		$\frac{1}{2}$
0X3F 8000	SRAM A	
	(10 Kbytes)	
0x3F C000	SRAM B	Ī
0x3F FFFF	(16 Kbytes)	
		_

USIU Control Registers 1 Kbyte	0x2F C000
FLASH Module A (64 bytes)	0x2F C800
FLASH Module B (64 bytes)	0x2F C840
	0x2F C880
Reserved for USIU	
IMB3 Address Space	
DPTRAM Control (12 bytes)	0x30 0000
Reserved (8180 bytes)	
DPTRAM (6 Kbytes)	0x30 2000
Reserved (2 Kbytes)	
TPU3_A (1 Kbyte)	0x30 4000
TPU3_B (1 Kbyte)	0x30 4400
QADC_A (1 Kbyte)	0x30 4800
QADC_B (1 Kbyte)	0x30 4C00
QSMCM (4 Kbytes)	0x30 5000
MIOS1 (4 Kbytes)	0x30 6000
TouCAN_A (1 Kbyte)	0x30 7080
TouCAN_B (1 Kbyte)	0x30 7480

Reserved (1920 bytes)

UIMB Registers (128 bytes) 0x30 7884

0x30 7F80

0x30 7FFF

Figure 2. MPC555 Internal Memory Map

Freescale

Semiconductor, Inc.

Freescale Semiconductor, Inc.

Fig ယ **MPC555 Pinout Diagram**

(JΩ	
	gure 3	
	S	
	S	
	ō	
	shows 1	
	Ħ	
	the	
۲	<u> </u>	
	pinout i	۰
	2	
	Ħ	
	\pm	
	jor.	
	\Box	
	for the	
	>	
	1	
	MPCSSS.)
	ن	
	Ũ	ì
	U	1

	MPC555 Ball Map																			
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Α	VDDH	A_TPUCH1	A_TPUCH4	A_TPUCH8	A_TPUCH12	A_TPUCH15	VRL	AAN0_PQB0	AAN48_PQB4	AAN52_PQA0	AAN54_PQA2	BANO_PQB0	BAN2_PQB2	BAN3_PQB3	BAN51_PQB7	VDDH	MDA11	MDA12	MDA13	VDDH
В	B_T2CLK	VDDH	A_TPUCH6	A_TPUCH10	A_TPUCH11	A_TPUCH14	VRH	AAN3_PQB3	AAN49_PQB5	AAN53_PQA1	AAN57_PQA5	BAN1_PQB1	BAN48_PQB4	BAN52_PQA0	BAN54_PQA2	ETRIG2	MDA14	MDA15	VDDH	MDA28
С	B_TPUCH15	A_T2CLK	A_TPUCH3	A_TPUCH7	A_TPUCH9	A_TPUCH13	VDDA	AAN2_PQB2	AAN51_PQB7	AAN56_PQA4	AAN59_PQA7	BAN49_PQB5	BAN53_PQA1	BAN56_PQA4	BAN57_PQA5	ETRIG1	MDA27	MDA29	MDA30	MDA31
D	B_TPUCH11	B_TPUCH13	A_TPUCH0	A_TPUCH2	A_TPUCH5	VDDI	VSSA	AAN1_PQB1	AAN50_PQB6	AAN55_PQA3	AAN58_PQA6	BAN50_PQB6	BAN55_PQA3	BAN58_PQA6	BAN59_PQA7	VDDI	VDDL	MPWM1	MPWM2	MPWM3
E	B_TPUCH7	B_TPUCH10	B_TPUCH14	VDDL													MPWM0	MPWM17	MPWM19	MPIO6
F	B_TPUCH5	B_TPUCH6	B_TPUCH8	B_TPUCH12													MPWM16	MPWM18	MPIO7	MPIO9
G	B_TPUCH2	B_TPUCH3	B_TPUCH4	B_TPUCH9													MPIO5	MPIO8	MPIO11	MPIO12
Н	B_TPUCH1	B_TPUCH0	B_CNRX0	B_CNTX0				,	,				•				MPIO10	MPIO15	MPIO14	MPIO13
J	TCK_DSCK	TDO_ DSDO	TRST_B	VDD SRAM					VSS	VSS	VSS	VSS					VF2_MPIO2	VFLS0 _MPIO3	VF0_MPIO0	VF1_MPIO1
K	TMS	TDI_DSDI	SGP_FRZ	VDDL					VSS	VSS	VSS	VSS					VDDL	VFLS1 _MPIO4	A_CNTX0	A_CNRX0
L	IWP1_VFLS	IWP0_VFLS	IRQ3B _SGP	IRQ4B _SGP					VSS	VSS	VSS	VSS					PCS1 _QGP	PCS0 _QGP	MISO_QGP4	MOSI_QGP5
М	IRQ0B_SGP	IRQ1B _SGP	IRQ2B _SGP	SGP_ IRQOUTB					VSS	VSS	VSS	VSS					PCS3 _QGP	PCS2 _QGP	ECK	SCK_QGP6
N	WEB_AT[0]	BRB_IWP2	BGB_LWP1	BBB_IWP3					Note: The pin	out is a top do	wn view of the	package.					RXD1_ QGPI	TXD1_ QGPO	RXD2_QGPI	TXD2_ QGPO
P	WEB_AT[1]	WEB_AT[2]	WEB_AT[3]	CS0B													VPP	EPEE	VSSF	VDDH
R	RD_WRB	CS3B	CS2B	CS1B													VDDL	VDDF	XFC	VDDSYN
Т	OEB	TEAB	TSIZ1	VDDL													VDDI	KAPWR	VSSSYN	EXTAL
U	TSIZ0	TAB	TSB	BDIPB	VDDI	Addr_SGP31	Addr_SGP30	Addr_SGP28	Addr_SGP29	VDDL	Data_SGP29	Data_SGP27	Data_SGP25	Data_SGP23	VDDL	Data_SGP20	RCFB_TXP	EXTCLK	ECK_BUCK	XTAL
v	BURSTB	BIB_STSB	Addr_SGP11	Addr_SGP10	Addr_SGP9	Addr_SGP8	Addr_SGP22	Addr_SGP27	Data_SGP31	Data_SGP30	Data_SGP28	Data_SGP26	Data_SGP24	Data_SGP22	Data_SGP21	Data_SGP19	Data_SGP18	CLKOUT	PORESETB	SRESETB
W	Addr_SGP12	VDDH	Addr_SGP14	Addr_SGP16	Addr_SGP18	Addr_SGP20	Addr_SGP23	Addr_SGP26	Data_SGP1	Data_SGP3	Data_SGP5	Data_SGP7	Data_SGP9	Data_SGP11	Data_SGP13	Data_SGP15	Data_SGP17	IRQ5B_SGP	VDDH	HRESETB
Y	VDDH	Addr_SGP13	Addr_SGP15	Addr_SGP17		Addr_SGP21			Data_SGP0	Data_SGP2	Data_SGP4	Data_SGP6	Data_SGP8	Data_SGP10	Data_SGP12	Data_SGP14	Data_SGP16	IRQ6B_mck2	IRQ7B _mck3	VDDH
	VDDH	=3 volt	power (I/	(O)	VDDi	=3 volt	power (in	ternal)		VSS	=ground			VDDH	=5 volt p	power			=Misc po	wer

Figure 3. MPC555 Pinout Diagram

21 November 1997

For More Information On This Product, Go to: www.freescale.com

MPC555 Product Brief



4 Supporting Documentation List

This list contains references to currently available and planned documentation.

- MPC555 User's Manual (MPC555UM/AD)
- RCPU Reference Manual (RCPURM/AD)
- Board Strategies for Ensuring Optimum Frequency Synthesizer Performance (AN1282/D)
- *Using the MIOS on the MPC555 Evaluation Board* (AN1778/D)
- Exception Table Relocation and Multi-Processor Address Mapping in the Embedded MPC5XX Family (AN1821/D)
- Non-Volatile Memory Technology Overview (AN1837/D)
- Designing Expansion Boards for the Freescale EVB555/ETAS ES200 (AN2001/D)
- *MPC555 Interrupts* (AN2109/D)
- EMC Guidelines for MPC500-Based Automotive Powertrain Systems (AN2127/D)
- Nexus Standard Specification (non-Freescale document)
- Nexus Web Site: http://www.nexus5001.org/
- IEEE 1149.1 Specification (non-Freescale document)

5 Revision History

Table 2. Revision History

Revision Number	Substantive Changes	Date of Release				
2	Existing Document.	September 2001				
2.1	Added temperature range for suffix A device.	11 December 2002				
3	Updated template and formats.	11 February 2003				



Key Features

THIS PAGE INTENTIONALLY LEFT BLANK



THIS PAGE INTENTIONALLY LEFT BLANK



How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor Technical Information Center, CH370 1300 N. Alma School Road Chandler, Arizona 85224 +1-800-521-6274 or +1-480-768-2130 support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku, Tokyo 153-0064 Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd. Technical Information Center 2 Dai King Street Tai Po Industrial Estate Tai Po, N.T., Hong Kong +800 2666 8080 support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center P.O. Box 5405 Denver, Colorado 80217 1-800-441-2447 or 303-675-2140 Fax: 303-675-2150

LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document. Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

