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MPC566EVB User's Manual

MPC566EVBUM
Rev. 1.2, 3/2003

Digital DNA from Motorola

MOTOROLA

Revision History

Version Number	Revision Date	Description of Changes
1.1	11/2002	Initial Version
1.2	3/2003	Fixed typos. Added appendix describing dBUG ethernet configuration. Added appendix for emulating the MPC53X parts.

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1. This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of EN5022 and EN 50082-1: 1998 as a **CLASS A** product.
2. This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.
3. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.
4. Anti-static precautions must be adhered to when using this product.
5. Attaching additional cables or wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

WARNING

This board generates, uses, and can radiate radio frequency energy and, if not installed properly, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for class a computing devices pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference. Operation of this product in a residential area is likely to cause interference, in which case the user, at his/her own expense, will be required to correct the interference.

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Chapter 1
MPC566 EVB Board

The MPC566EVB is an MPC566-based evaluation board that can be used for the development and test of microcontroller systems[1] (see Figure 1-1). The MPC566 is a member of the Motorola MPC500 RISC microcontroller family. It is a 32-bit processor with a 32-bit internal address bus and 32 lines of data.

The evaluation board is a development and test platform for software and hardware for the MPC566[1]. The system provides for development of target applications for the similar MPC561, MPC562, or MPC563 microcontrollers also. It can be used by software and hardware developers to test programs, tools, or circuits without having to develop a complete microcontroller system themselves. All special features of the MPC566[1] are supported.

The heart of the evaluation board is the MPC566. The MPC566EVB has 1Mbyte (256K x 32) external SRAM for development or application memory, 2Mbyte (512K x 32) external Flash memory, and numerous hardware expansion possibilities. The MPC566EVB board also provides an Ethernet interface (10/100BaseT), TouCAN, and RS232 interface in addition to the built-in I/O functions of the MPC566[1] device for programming and evaluating the attributes of the microprocessor. To support development and test, the evaluation board can be connected to debuggers and emulators produced by different manufacturers.

The MPC566EVB provides for low cost software testing with the use of a ROM resident debug monitor, dBUG, programmed into the external Flash device. Operation allows the user to load code in the on-board RAM, execute applications, set breakpoints, and display or modify registers or memory. After software is operational, the user may program the MPC566 Internal Flash EEPROM or the on-board FLASH memory for dedicated operation of new software application. No additional hardware or software is required for basic operation. For high level debug, extensive third-party tools are available for the MPC500 series. The Nexus and BDM debug ports are available to connect the tool sets.

Specifications

Clock: 56 MHz Maximum, 4Mhz reference
Operating temperature: 0°C to +70°C
Power requirement: 6 – 26V DC @ 300 ma Typical
Power output: 5.8V @ 1.5A output with 5V, 3.3V, and 2.6V regulated supplies
Board Size: 7.00 x 7.60 inches, 8 layers

[1]The MPC566EVB can be used to emulate the MPC535 and MPC536. See Appendix A and MPC566 Electrical Spec for limitations.

•**Memory Devices**:
1M Byte (256K x 32) Sync. SRAM
2M Byte (512K x 32) Sync. FLASH
1M Byte FLASH internal to MPC566 device
36K Byte SRAM internal to MPC566 device
•**POWER OAK** (PC33394 P2.6) regulated power supply for 5V, 3.3V and 2.6V supplies.
•**MAP Switch** – provides easy assignment of chip selects and memory mapping.
•**CONFIG Switch** – Basic necessary Reset Word Configuration options.
•**COM1** - SCIA1 with RS232 type DB9-S Connection
•**COM2** - SCIA2 with RS232 type DB9-S Connection, TX / RX polarity option.
•**COM3 & 4** - SCIB1 and SCIB2 with RS232 type DB9-S Connection, 10 pin IDC ribbon header connectors.
•**CAN Ports**[1] – 3 CAN transceiver interfaced ports, 1 x 4 headers.
•**10/100T Ethernet Port** – LAN91C111 based MAC+PHY, memory mapped.
•**DEVELOPMENT Ports** – Nexus 50 pin and dual voltage BDM Port.
•**LCD Port** - LCD Module Interface Connector w/ Contrast Adjust, Buffered and Memory Mapped
•**KEYPAD Port**[1] - 16 Key passive interface, applies QADC_B channels for operation.
•**BUS Port** – 32 data and 24 address lines on 60 pin header.
•**CONTROL Port** - Bus Controls with 40 pin header.
•**QSM Ports** – 2 Serial I/O ports with 16 pin socket headers.
•**MIOS Port** - MDA, PWM, and MGPIO ports with 34 pin socket header.
•**TPU Ports**[1] - 3 Timing Processor I/O ports with 20 pin socket headers.
•**QADC Ports**[1] - 2 Analog I/O ports, one 20 pin and one 24 pin socket header.
•**IRQ Port** – Interrupt or MPC566 port I/O with 10 pin socket header.
•**POWER Port** – Primary and standby power supply access port, no header.
•**I/O Connectors** in .1 grid, pin headers for bus and control provide easy ribbon cable connection for external connections. Socket headers provide easy wire connection to breadboard prototype area with 22ga solid wire.
•**Large Prototyping Area** with +5V and ground connection grids.
•Mictor Logic Probe connectors for the Address and Data bus (Not installed default)
•**Breadboard Prototyping area** (2.5 x 1.5 inch) for easy installation of test connections.
•**System Indicators** – Reset Indicator, Supply voltage indications for 5V, 3.3V, and 2.6V supplies
•**Reset Switches** – POReset, Hard, Soft reset buttons.
•**User Components** – 4 user LEDs (one with debounce), 4 user Switches, 1 user Potentiometer with socket header for I/O connection.

[1]The MPC535/6 has limited or no functionality for this module. See Appendix A

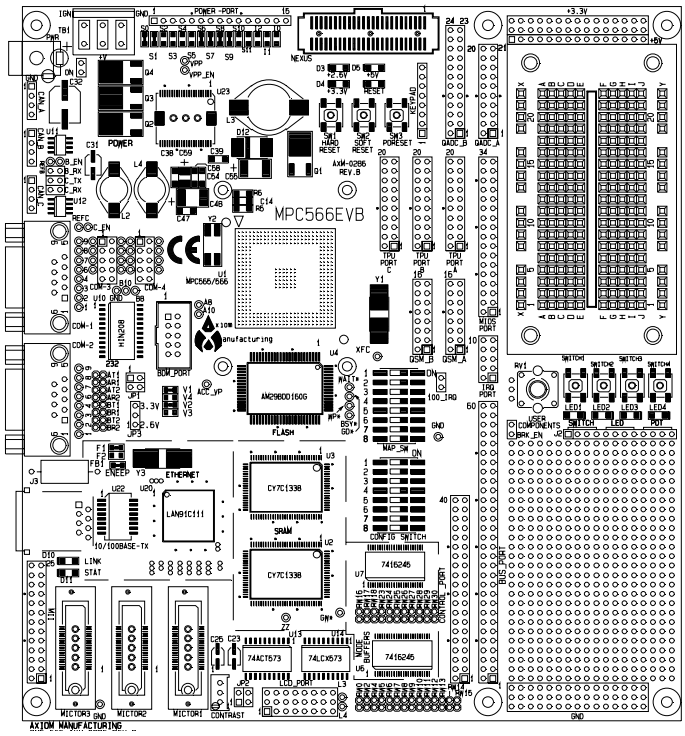


Figure 1-1. MPC566 EVB top view

1.1 Processor

The microprocessor used on the MPC566EVB is the highly integrated Motorola PowerPC MPC566 32-bit microcontroller. The MPC566 implements a PPC ISA core with 1MByte UC3F flash, four UART channels, three Timing Processor Units (TPUs)[1], 36 KBytes of SRAM plus 4KBytes DECRAM, a QSPI (Queued Serial Peripheral Interface) module, three TouCAN modules[1], 12 PWMs and 6 counter submodules in the MIOS, enhanced QADC64E, PPM module[1], a Nexus debug interface port, and 6KByte DPTRAM[1]. This processor communicates with external devices over a 32-bit wide data bus, D[0:31]. The MPC566 can address a 32 bit address range. Only 24 bits are available on the bus however. There are internally generated chip selects to allow the full 32 bit address range to be selected. There are regions that can be decoded to allow superviser, user, instruction, and data each to have the 32-bit address range. All the processor's signals are available through the expansion connector (BUS_PORT). Refer to the schematic for their pin assignments.

The MPC566 processor has the capability to support both an IEEE-ISTO 5001-1999 NEXUS port and a BDM debug port. These ports are multiplexed and can be used with third party tools to allow the user to download code to the board. The board is configured to boot up in the normal/BDM mode of operation. The BDM signals are available at the port labeled BDM_PORT. The NEXUS connector is near the reset switches on the board. It is the 2002 50 pin standard I/O connections and connector. The BDM and NEXUS ports can not be used at the same time.

[1]The MPC535/6 has limited or no functionality for this module. See Appendix A.

Figure 1-2 shows the MPC566 block diagram.

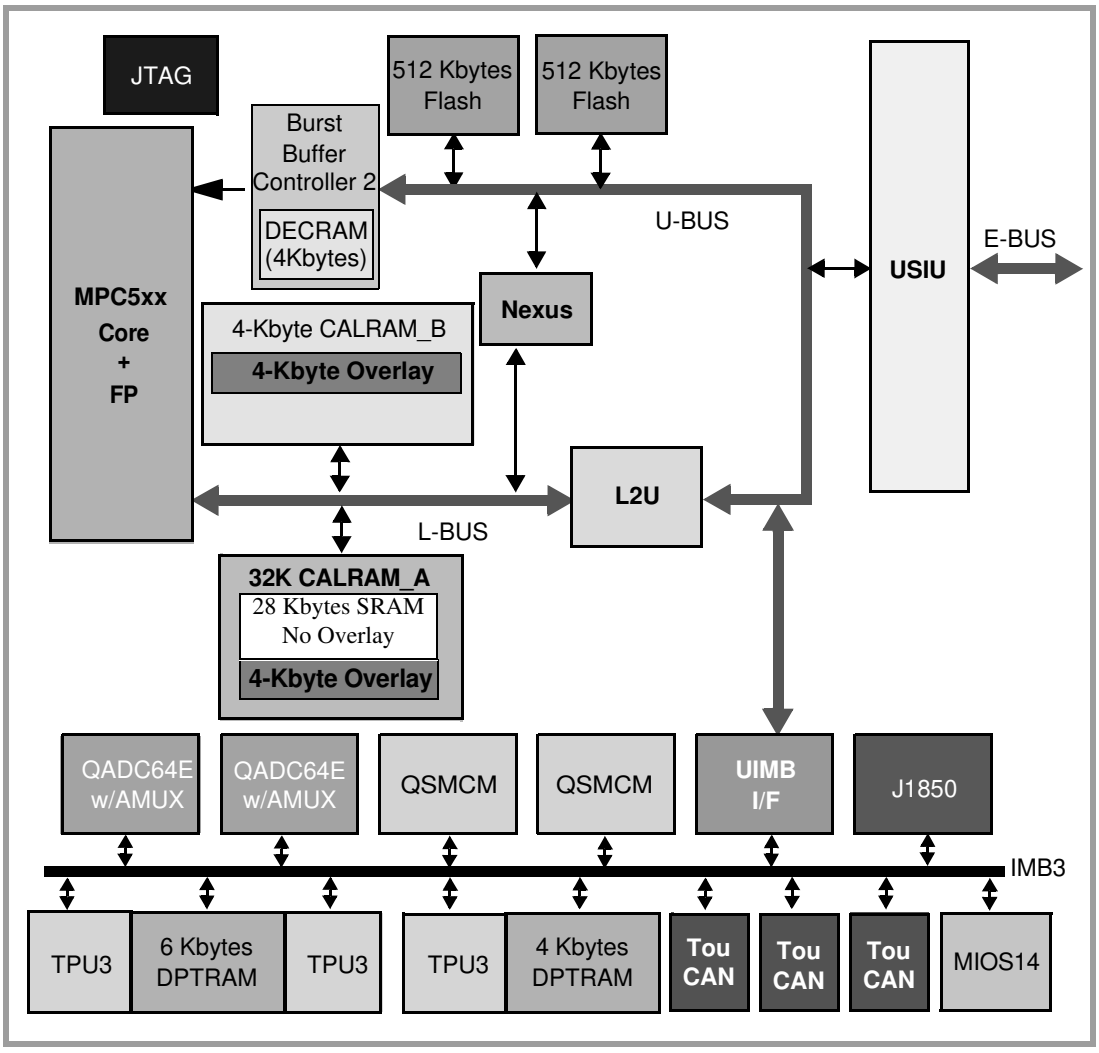


Figure 1-2. MPC566[1] Block Diagram

1.2 System Memory

1.2.1 External Flash

One on-board Flash ROM (U4) is used in the system. The Am29BDD160G device contains 16Mbits of non-volatile storage (1 M x 16-bit/512 K x 32-bit) giving a total of 2MBytes of Flash memory. This device requires a 32 bit wide port and must be written in 32 bit word size data. It may be read in bytes, half words, or words. Wait states are required to access in asynchronous mode and the same wait state delay is required during the first cycle of a burst type access. Refer to the specific device data sheet for configuring the flash memory. User should note that the debug monitor firmware is installed in this flash device. Development tools or user application programs

[1]See Appendix A for block diagram of MPC535/6

may erase or corrupt the debug monitor. If the debug monitor becomes corrupted and it's operation is desired, the firmware must be programmed into the flash by applying a development port tool such as BDM or Nexus. User should use caution to avoid this situation. The upper 1 MByte is used to store the MPC566EVB dBUG debugger/monitor firmware (0x0090_0000 to 0x009F_FFFF).

1.2.2 SRAM

The MPC566EVB has two 512 KByte device on the board (U2). It's starting address is 0xFFF0_0000.

The synchronous SRAM Memory Bank is composed of two128K x 32 memory devices. These memory devices are connected in linear order from U2 to U3 if more than one is available, so that the low order address of the memory bank will access U2 and the high order addresses of the memory bank will access U3. This memory bank must be configured as a 32 bit wide port but is byte, half word, and word accessible for read or write operations.

Also see Section 1.2.5, "MPC566EVB Memory Map".

1.2.3 Internal SRAM

The MPC566 processor has 36-KBtyes of internal memory which may be used as data or instruction memory. This memory is mapped to 0x003F_8000 and configured as data space but is not used by the dBUG monitor except during system initialization. After system initialization is complete, the internal memory is available to the user. The memory is relocatable to any 32-KByte boundary.

1.2.4 Internal Flash

The MPC566 has a U-bus CDR3 flash EEPROM module (UC3F). The primary function of the UC3F flash EEPROM module is to serve as electrically programmable and erasable non-volitle memory (NVM) to store program instructions and/or data. The MPC566 flash EEPROM array has 1 Mbytes of NVM that is divided into sixteen 64-Kbyte array blocks. If the flash array is disabled in the IMMR register (FLEN=0), then neither the UC3F array or the UC3F control registers are accessible. This feature allows the MPC566 to emulate the MPC561/562.

Please refer to the MPC566 User's Manual for more details.

1.2.5 MPC566EVB Memory Map

Interface signals to support interface to external memory and peripheral devices are generated by the memory controller. It supports four regions on four chip-select pins. The general purpose chip-selects are available on lines $\overline{CS}[0]$ through $\overline{CS}[3]$. $\overline{CS}[0]$ also functions as the global (boot) chip-select for booting out of external flash.

Since the MPC566 chip selects are fully programmable, the memory banks can be located at any location in the MPC5xx memory space.

Following is the default memory map for this board as configured by the Debug Monitor located in the external flash bank. The internal memory space of the MPC566 is detailed further in the MPC565-6 Users Manual. Chip Selects 0-3 can be changed by user software to map the external memory in different locations but the chip select configuration such as wait states and transfer acknowledge for each memory type should be maintained.

Possible Chip Select usage:

Synchronous SRAM Memory Bank	CS0 or CS1	default CS1, MAP SW. 1,2
Synchronous FLASH Memory Bank	CS0 or CS2	default CS0, MAP SW. 3,4
10/100T / LCD Port	CS3	default CS3, MAP SW. 6,7
MPC566 Internal Flash ory map of chip selects	N/A	MAP_SW. 8, may effect mem-

The MPC566EVB Default Memory Map shows the MPC566EVB memory map.

Table 1-1. The MPC566EVB Default Memory Map

Address Range	Signal and Device
0x0000_0000 - 0x0007_FFFF	1MB UC3F Flash
0x0010_0000 - 0x002F_7FFF	Reserved for Flash
0x002F_8000 - 0x002F_8FFF	BBC DECRAM 4 KBytes
0x002F_9000 - 0x002F_9FFF	Reserved for BBC
0x002F_A000 - 0x002F_BFFF	BBC Control
0x002F_C000 - 0x002F_FFFF	USIU & Flash Control
0x0030_0000 - 0x0030_7FFF	UIMB I/F & IMB Modules 32KBytes
0x0030_8000 - 0x0037_FFFF	Reserved for IMB
0x0038_0000 - 0x0038_007F	CALRAM/READI Control
0x0038_0080 - 0x0038_3FFF	Reserved (L-bus Control)
0x0038_4000 - 0x003F_6FFF	Reserved (L-bus Memory)
0x003F_7000 - 0x003F_FFFF	CALRAM (internal SRAM)
0x0080_0000 - 0x00A0_0000	External Flash 2MByte (0x0090_0000 - 0x00A0_0000 reserved for dBUG)
0x0100_0000 - 0x0108_0000	Ethernet
0xFFF0_0000 - 0xFFFF_FFFF	External SRAM 1MB

1.2.5.1 Memory Device / Bank Selection and Configuration.

The MPC566EVB board has one internal memory bank, two external memory banks and a Peripheral memory bank that provide:

- 36KByte Internal SRAM
- MPC566 512K byte Internal FLASH Memory (U1)
- 256K x 32bit (1MByte) Synchronous Static RAM (U2/3).

- 512K x 32bit (2MByte) Synchronous Flash EEPROM (U4)
- Peripherals 10/100T Ethernet and LCD Port

Each external RAM or Flash memory bank can be configured individually to operate from the MPC566 chip selects. Caution should be used not to place more than one memory bank on the CS0 chip select and to properly configure the chip select to control the memory devices provided in the memory bank correctly. **Failure to observe precautions may render the external memory bus inoperable.**

The MAP Switch (MAP_SW) connects MPC566 chip selects to the different external memory banks. If memory access problems occur, the settings of these options and the associated chip select configurations should be reviewed with some detail. Information to configure the chip selects and memory is detailed in the following section.

1.2.5.2 Memory Bank Chip Select Configuration

Application software that executes on Reset must configure each memory bank chip select properly for correct operation. Chip Select Memory Options shows the default memory settings programmed by the dBUG ROM monitor and may be applied for most user applications:

Table 1-2. Chip Select Memory Options

Memory Bank	Reg.	Default Value	Notes
CS1 = SRAM	BR1	0xFFF0_0003	Base Address = 0xFFF0_0000, Port width = 32 bit ***Default**
CS1 = SRAM, asynchronous access mode	OR1	0xFFF0_0000	Memory Range = 0xFFF0_0000 > 0xFFFF_FFFF, wait state = 0.
CS0 = FLASH	BR0	0x0080_0003	Base address 0x0080_0000, Port width = 32 bit ***Default**
CS0 = FLASH, asynchronous access mode	OR0	0xFFE0_0030	Memory range = 0x0080_0000 > 0x009F_FFFF, wait state = 3, asynchronous operation 40Mhz clock, 95ns device. Note U4 = 2M bytes and will mirror 2x with this setting. Usable range = 0x0080_0000 > 0x008F_FFFF (dBUG monitor is in upper half starting at 0x0090_0000)
CS3 = Peripheral	BR3	0x0100_0807	Base address = 0x0100_0000, Port width = 16 bit ***Default** External TA* generation provided.
CS3 = Peripheral, asynchronous	OR3	0xFFFF_80F0	Memory Range 0x0100_0000 > 0100_7FFF, wait state = External Terminate (TA*) ***Default** Note Peripheral memory map.

1.2.5.3 Reset Vector Mapping

After reset, the processor attempts to execute at physical address 0x0000_0100 if the hard reset configuration word IP bit is cleared to 0 or physical address 0xFFF0_0100 if the hard reset configuration word IP bit is set to 1. This requires the board to have a non-volatile memory device in this range with the correct information stored in it. The MPC566 processor chip-select zero ($\overline{CS0}$) responds to any accesses after reset until the OR0 is written. Since $\overline{CS0}$ (the global chip select) is connected to the Flash ROM (U6), the Flash ROM initially appears at address 0xFFF0_0000. The initialization routine then programs the chip-select logic, locates the Flash

ROM to start at 0x0080_0000 and configures the rest of the internal and external peripherals. Please refer to the MPC565 user's manual (Global (Boot) Chip-Select Operation) for more information.

1.3 Support Logic

1.3.1 Reset Logic

The reset logic provides system initialization. Reset occurs during power-on or via assertion of the signal RESET which causes the MPC566 to reset. HRESET is triggered by the reset switch (SW1) which resets the entire processor/system.

dBUG configures the MPC566 microprocessor internal resources during initialization. The contents of the exception table are copied to address 0xFFF0_0000 in the SDRAM. The Software Watchdog Timer is disabled, the Bus Monitor is enabled, and the internal timers are placed in a stop condition. A memory map for the entire board can be seen in Table 1-1., "The MPC566EVB Default Memory Map".

RW0 – 30: External Reset Configuration Word (RCW) Options

RW0, RW2, RW4 – 18, RW23 – 30 provide the user access to external Reset Configuration Word (RCW) bits not normally required for default MPC566EVB operation. The RW0 – 30 designations reflect the data bus D0 – D30 bit effected when the RCW word is enabled externally. All RW0 – 30 option bits are defaulted to the logic low value during external RCW word operation. The user may apply a wire jumper between the 2 pad positions of each RW0 – 30 option to provide a logic high level on the respective bit position during external RCW operation. Refer to the MPC566 user manual Reset chapter for the respective RCW bit definitions.

1.3.2 Clock Circuitry

The MPC566EVB board uses a 4MHz crystal (Y1 on the schematics) to provide the clock to the on-chip oscillator of the MPC566. In addition to the 4MHz crystal, there is also a 25MHz oscillator (Y3) which feeds the Ethernet chip (U20).

1.3.3 Watchdog Timer

The duration of the Watchdog is selected by the SWT[1:0] bits in the System Protection and Control Register (SYPCR), SWT[1:0] = 0b11 gives a maximum timeout period of 2^{28}/System frequency. The dBUG monitor initializes these bits with the value 0b11, which provides the maximum time-out period, but dBUG does **NOT** enable the watchdog timer via the SYPCR register SWE bit.

1.3.4 Exception Sources

The MPC500 family of processors can receive exceptions as a result of external signals, errors, interrupts, or unusual conditions arising in the execution of instructions. When the processor receives an exception, information about the state of the processor is saved and, after switching to supervisor mode, the processor begins handling the exception based on instructions in the

Exception Vector Table in memory. Exceptions are handled in program order based on PowerPC architecture requirements. When an exception occurs that was caused by an instruction, any unexecuted instructions that appear earlier in the instruction stream are required to complete before the exception is taken. Exceptions no associated with a specific instruction (asynchronous exceptions) are recognized when they occur. Exception handlers should save the information in SRR0 and SRR1 soon after the exception is taken to prevent this information from being lost due to another exception being taken.

The processor goes to an exception routine via the exception table. This table is stored in the Flash EEPROM. The address of the table location is set by the IP bit (switch 5 of MAP_SWITCH). The dBUG ROM monitor writes a copy of the exception table into the RAM starting at 0xFFF0_0000. To set an exception vector, the user places the address of the exception handler in the appropriate vector in the vector table located at 0xFFF0_0000.

The MPC566's interrupt controller supports up to 8 external interrups (0 - 7), eight levels for all internal USIU interrupt sources and 32 levels for internal peripheral modules. It has an enhanced mode of operation, which simplifies the MPC566 interrupt structure and speeds up interrupt processing.

NOTE:

No interrupt sources should have the same level and priority as another. Programming two interrupt sources with the same level and priority can result in undefined operation.

The MPC566EVB hardware uses $\overline{\text{IRQ}}$[0]/SGPIOC[0] to support the ABORT (Non Maskable Interrupt) function using the ABORT switch (SWITCH1 when BRK_EN jumper is inserted). This switch is used to force a non-maskable interrupt if the user's program execution should be aborted without issuing a RESET.

Refer to MPC566 User's Manual for more information about the interrupt controller.

1.3.5 TA Generation

The $\overline{\text{TA}}$ signal is driven by the slave device from which the current transaction was addressed. It indicates that the slave has received the data on the write cycle or returned data on the read cycle. If the transaction is a burst, $\overline{\text{TA}}$ should be asserted for each one of the transaction beats. The MPC566 drives $\overline{\text{TA}}$ when the slave device is controlled by the on-chip memory controller or when an external master initiated a transaction to an internal slave module. $\overline{\text{TA}}$ is used to indicate the completion of the bus cycle. It also allows devices with different access times to communicate with the processor properly (i.e. asynchronously) like the Ethernet controller. The internal TA generator is used for all external memories. External TA is only used for Ethernet/LCD.

1.3.6 User's Program

Switch 5 on the MAP_SW bank of switches allows users to test code from boot/PORESET without having to overwrite the ROM Monitor. The user's code will boot from internal flash (0x0000_0000) needs to contain the start of the Exception Vector Table).

When the switch is ON (IP is set), the behavior of the system is normal, dBUG boots and then runs from 0x0090_0000.

Procedure:

1. Compile and link as though the code was to be placed at the base of the internal flash, but setup so that it will download to the SRAM starting at address 0xFFF0_8000. The user should refer to their compiler documentation for this, since it will depend upon the compiler used.
2. Set IP bit (Switch 5 ON).
3. Download to SRAM (If using serial or ethernet, start the ROM Monitor first. If using BDM via a wiggler cable, download first, then start ROM Monitor by pointing the program counter (PC) to 0x0090_0100 and run.)
4. In the ROM Monitor, execute the 'upuser' command.
5. Turn off IP bit (Switch 5 OFF). User code should now be running from reset/POR.

1.3.7 Power Oak K/I/S Hardware Options

Several hardware options surround the Power Oak supply to allow the user access to many of the features. The options are sorted by leading character to indicate functionality. 'K' designated options refer to VKAM and MPC566 back-up supply options. 'I' designated options refer to Interrupt operation options. 'S' designated options refer to MPC566 Reset or I/O signal connection options. Following is the summary table (also refer to MPC566EVB schematic):

Table 1-3. K/I/S Option Table

Option Designator	Power Oak Signal	MPC566 signal	Associated Option[1]	Default Connection
K0	VKAM	KAPWR	K1	Closed, Note: REV B board has 0 ohm resistor installed
K1	2.6V	KAPWR	K0	Open
K2	VKAM	VDDSRAM1	K3	Closed
K3	2.6V	VDDSRAM1	K2	Open
K4	VKAM	VDDSRAM2	K5	Closed
K5	+2.6V	VDDSRAM2	K4	Open
K6	VKAM	VDDSRAM3	K7	Closed
K7	2.6V	VDDSRAM3	K6	Open
K8	VKAM	VDDSYN	K9	Open
K9	2.6V	VDDSYN	K8	Closed
K10	VKAM	VDDRTC	K11	Closed
K11	2.6V	VDDRTC	K10	Open
I0	WAKEUP	IRQ4		Open
I1	WAKEUP	IRQ0	I2	Open
I2	PRERESET	IRQ0	I1	Open

Option Designator	Power Oak Signal	MPC566 signal	Associated Option[1]	Default Connection
S0	PORESETB	PORESET		Closed
S1	HRESETB	HRESET		Closed
S2	SLEEP	RSTCONF_TEXP		Open
S3	REGON	MGPIO15		Open
S4	CANTXD	B_CANTX0	A_CANTX0	Open
S5	CANRXD	B_CANRX0	A_CANRX0	Open
S6	$\overline{CS}$	A_QSPI_PCS1		Closed
S7	DO	A_QSPI_MISO		Closed
S8	DI	A_QSPI_MOSI		Closed
S9	VREF3	BOEPEE	S11	Open
S10	VREF3	EPEE	S10	Open

[1] The MPC535/6 has limited or no functionality for this module. See Appendix A

1.4 Communication Ports

The MPC566EVB provides external interfaces for 4 SCI serial ports, 3 CAN ports and a 10/100T ethernet port.

1.4.1 COM1 - COM4

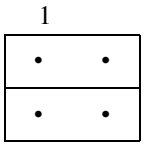
The MPC566 processor has two queued serial multi-channel modules (QSMCM_A and QSMCM_B) which provides four serial communications interfaces (SCI/UART). These submodules communicate with the CPU via a common slave bus interface unit (SBIU). The signals of COM1 and COM2 pass through external Driver/Receivers to make the channels RS-232 compatible. COM3 and COM4 serial ports with 10 pin IDC to DB9 connector headers are available for RS232 operation of MPC566 SCI B channels 1 and 2. An RS-232 serial cable with DB9 connectors is included with the board. The signals of both channels are available on the QSM_PORT connector. SCI0 (COM-1) is the “TERMINAL” channel used by dBUG for communication with an external terminal/PC. The “TERMINAL” baud rate defaults to 19200.

Notes:

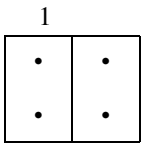
1. COM ports provide connection pads 1 – 9 behind the DB9 cable connectors so the user may modify operation of the serial connection. Each connection pad is numbered for the associated serial connector pin. Each connection pad can be isolated from the others if grouped above, by cutting the associated trace to the pad on the bottom side of the board. See the MPC566EVB schematic.
2. COM-2 has the JP1 DCE/DTE option, see below.

3. RS232 translators available to COM3 and COM4 that are not required by user application may be applied to other COM ports by isolating the MPC566 SCI signals to the RS232 transceiver and applying the associated RS232 level input or output to another COM port. User should refer to the schematic diagrams of the board to make sure correct signals and connections are isolated and reconnected for the new application.

JP1 – COM2 DCE/DTE Option:



COM-2 is optioned as a DCE type RS232 connection by default (same as COM-1). This allows direct connection to a standard 9 pin PC COM serial port.



COM-2 DTE option. This requires a NULL modem adapter to connect to a standard 9 pin PC COM serial port.

AT1/2, AR1/2, BT1/2, BR1/2 - Serial Port Configuration

The Axx and Bxx cut-away options provide a means of isolating the individual SCI RXD and TXD signals from the RS232 interface translator device (U10) and COM port operation. This allows the SCI channels to be used for other purposes, possibly on the QSM port connector. Following is a table of the SCI signals and AT/R_ positions used for enabling RS232 and COM port operation. Note: 2mm header maybe installed after cutaways are cut to allow jumper option.

Table 1-4. Serial Port Configuration

AT_ Position	SCI Channel Signal	RS232 COM Port Connection	COM_PORT Signal Direction to RS232 interface translator
AT1	SCI_A_ TXD1	COM-1	Output
AR1	SCI_A_ RXD1	COM-1	Input
AT2	SCI_A_ TXD2	COM-2	Output
AR2	SCI_A_ RXD2	COM-2	Input
BT1	SCI_B_ TXD1	COM-3	Output
BR1	SCI_B_ RXD1	COM-3	Input
BT2	SCI_B_ TXD2	COM-4	Output
BR2	SCI_B_ RXD2	COM-4	Input

1.4.2 CAN PORTs and Options[1]

The MPC566EVB board provides 3 CAN transceivers with I/O ports: CAN_A, CAN_B, and CAN_C. CAN_A is supported by the PC33394 Power Oak CAN transceiver. The CAN_B and CAN_C ports are supported by Philips PCA82C250 1M Baud CAN transceivers. The MPC566 CAN_A port is directly interfaced to the Power Oak transceiver and can not be isolated easily. The MPC566 CAN_B and C ports are interfaced to the MPC566 TOUCAN channels B and C by option jumpers B_RX, C_TX, and C_RX.

CAN_A

The CAN_A channel transceiver is provided by the Power Oak (PC33394). This transceiver has software selectable options via the QSPI 0 channel which may communicate with the Power Oak device. See the PC33394 data sheet for details. A 4.7K ohm pull-up is provided on the CAN_A TX signal. Options S4 and S5 are provided near the Power Oak device to provide both MPC566 CAN_A and CAN_B channels for messaging on the Power Oak transceiver. If S4 and S5 are connected, the B_RX option from the CAN_B port must be open.

B_RX Option Jumper

This option jumper enables the receive connection from the CAN_B port transceiver to the MPC566 CAN B RX channel. The option allows the isolation of the CAN_B port transceiver RX signal so that the user may use a different connection or transceiver for the MPC566 CAN B port.

C_RX and C_TX Option Jumpers

These options enable the CAN_C port transceiver RX and TX signals to be placed on the MPC566 MGPIO port CAN C signals. The CAN C operation on the MPC566 MGPIO port must be enabled in software, see example source code. The MPC566 MGPIO Port bits 13 and 14 are effected along with the MPC566EVB MIOS Port pins 32 and 33 respectfully.

B_EN and C_EN Option Pads, CN1 and CN2 Option Cut-Aways

These options provide access to the output enable and slew rate control of the respective CAN transceiver. By default the transceivers are set to provide minimum slew rate (fast edge) and to be constantly enabled for output. The configuration of the transceivers maybe modified for slew rate or output control or both. Signaling CAN bus slew rate can be modified by increasing the value of R66 and R67 for CAN_B and CAN_C respectfully. Opening the CN1 and CN2 away options for CAN_B and CAN_C respectfully allows a MPC566 I/O port to be applied to the B_EN and C_EN option pads to provide output control. A high level on the B_EN or C_EN would disable the respective CAN transceiver output. See the PCA82C250 data sheet on the support CD for additional information.

CAN_A, CAN_B, and CAN_C Port Connectors

These ports provide the CAN transceiver input and output connection to the CAN bus. The bias or termination for the CAN bus is provided on the EVB board but not pupualted. If required the user must install these components in the RAx, RBx, or RCx locations near the respective CAN port.. Following are the pin connections for the ports:

Pin 1 = CAN-Hi level signal

Pin 2 = CAN-Lo level signal

Pin 3 = Ground or common (this is required for proper return path on CAN bus)

[1]The MPC535/6 has limited or no functionality for this module. See Appendix A

Pin 4 = +5V supply for remote use or bias of CAN bus.

CAN_A, CAN_B, and CAN_C Port Termination Options

The RA1-3, RB1-3, and RC1-3 option locations provide the respective CAN A, B, or C port with the ability to add bias and/or termination resistance. RA1, RB1, and RC1 locations provide low bias (to ground) on the respective CAN Port CAN Hi signal. RA3, RB3, and RC3 locations provide high bias (to +5V) on the respective CAN Port CAN Low signal. RA2, RB2, and RC2 locations provide termination between the respective CAN Port CAN Hi and CAN Low signals.

1.4.3 10/100T Ethernet Port

The MPC566EVB has an Ethernet controller (SMSC LAN91C111 U20) operating at 10M bits/sec or 100Mbits/sec (see the device data sheet on the support CD forr operation details). The dBUG ROM monitor is programmed to allow a user to download files over a network to memory in different formats. The compiler-formats currently supported are S-Record, COFF, ELF, or Image (raw binary). Refer to Appendix B, “Configuring dBUG for Network Downloads”, for details on how to configure the board for network download.

The Ethernet registers are located at chip select CS3 base address in the address range 0x0000 - 0x000F. The access is 16 bits wide or half word transfers only. The LAN91C111 device applies a register bank selection technique to provide a minimum memory space size. Users should review the device data sheet in detail for operation notes. The debug monitor applies the Ethernet for file downloads only, no high level stacks are applied in the sample source code.

RJ45 jack J3 of the Ethernet port provides a direct to HUB type connection. The Ethernet cable provided with the MPC566EVB kit is a crossover type for direct connection of the EVB to a PC host network card. If connection to a HUB is desired, a standard Ethernet cable should be applied.

Table 1-5. Ethernet Jack J3

PIN	SIGNAL
1	TX+
2	TX-
3	RX+
4	Term 1 75 ohm
5	Term 1 75 ohm
6	RX-
7	Term 2 75 ohm
8	Term 2 75 ohm

100_IRQ Option Jumper

The 100_IRQ Option jumper provides Ethernet Interrupt capability to the MPC566 processor. With the option installed and the LAN91C111 device properly configured, the MPC566 IRQ1 interrupt can be applied to service the port.

LINK and STAT Indicators

The LAN91C111 Ethernet controller provides two indication drivers under software control. The LINK indicator is driven by the LAN91C111 LEDA output and the STAT indicator is driven by the LEDB output.

MII Connector

The MII connector location is for testing and the connection of an external Ethernet PHY device. This connector is not installed or supported by the EVB application.

1.4.4 BDM and NEXUS Development Ports

Both NEXUS (MPC566 Readi Module) and standard BDM (background debug module) development ports are provided on the MPC566EVB for application of integrated software debug tool suites. In order to use the BDM, simply connect the 10-pin debug connector on the board, BDM_PORT, to the P&E BDM wiggler cable provided in the kit. No special setting is needed. Refer to the MPC566 User's Manual BDM Section for additiona instructions. The NEXUS interface provides the IEEE-ISTO 5001 50 pin standard I/O connections and connector and the BDM port provides the standard 10 pin interface (refer to MPC566EVB schematic sheet 3 for details). User should observe that both ports can not be applied at the same time. Note that the NEXUS interface applies some of the MPC566 standard I/O signals from the MIOS module as alternate development port I/O signals. Following are the I/O effected:

MGPIO 7, 8, 9, 10.

NOTE:

BDM functionality and use is supported via third party developer software tools. Details may be found on CD-ROM included in this kit

1.4.4.1 BDM Port Options

The BDM Port provides several options for flexibility of operation.

JP3 - BDM Port Interface Level

JP3 provides the option of 2.6V or 3.3V interface levels on the BDM port. This allows the use of legacy MPC555 BDM tools on the MPC566. The option is set for 3.3V interface from the factory. The following JP3 reference is with the MPC566EVB setting with the COM ports facing left.