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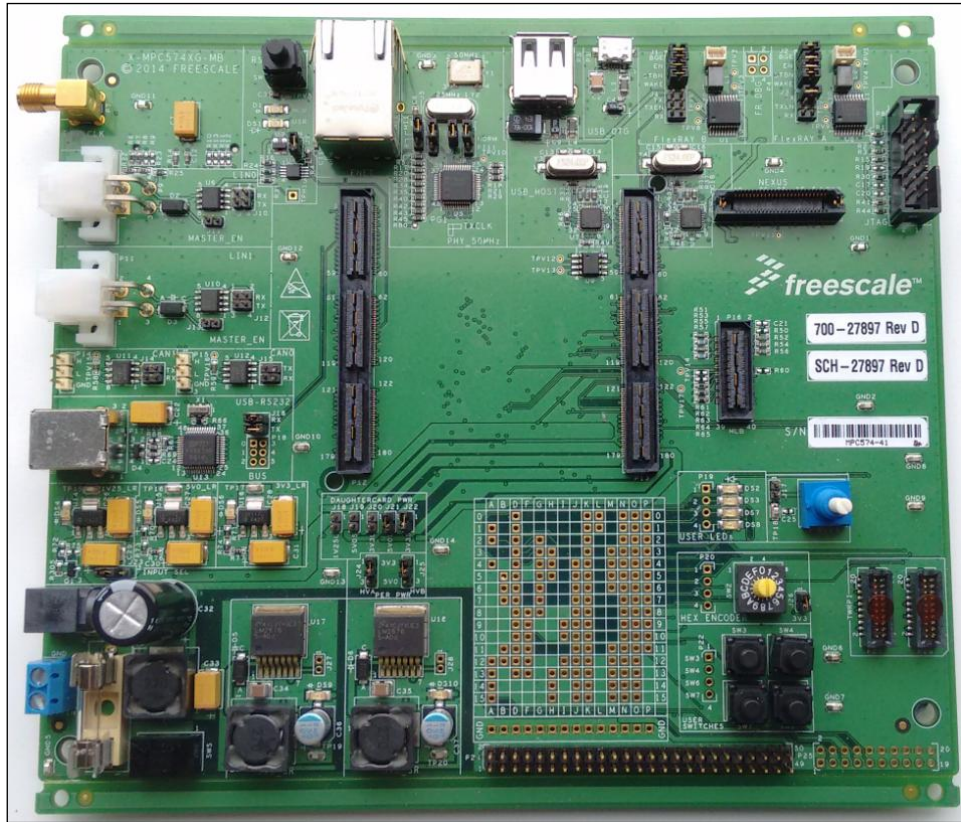
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





MPC5748G EVB User Guide

By: Alasdair Robertson

Contents

1.	INTRODUCTION	3
1.1.	Peripheral Daughtercards.....	3
2.	EVB FEATURES	3
3.	CONFIGURATION OVERVIEW	5
4.	MCU DAUGHTERCARD INFORMATION	6
4.1.	Fitting a daughtercard	6
4.2.	Removing a daughtercard.....	6
5.	INITIAL CONFIGURATION	7
5.1.	Power Supply Configuration	7
5.1.1.	Power Supply Connectors (P21, P23)	7
5.1.2.	Power Switch (SW5).....	8
5.1.3.	Regulator Power Jumper (J23)	8
5.1.4.	Power Status LED's and Fuse	8
5.1.5.	MCU Power Supply Jumpers (J18, J19, J20, J21, J22, J23).....	9
5.1.6.	Daughtercard Power Jumpers (J3 to J11)	10
5.1.7.	Peripheral Power Supply Jumpers (J24, J25)	11
5.1.8.	EVB Voltage Regulators	11
5.2.	Reset Control (J9, SW1)	13
	Note that removing jumper J9 will mean that an external reset source will not reset the MCU. This will impact most debuggers which will typically issue a reset before establishing a debug connection.	13
5.2.1.	Reset LEDs.....	13
5.3.	MCU Clock Configuration	14
5.3.1.	External Clock Input (P7).....	15
5.3.2.	MCU Clock Configuration (J1, J2 on Daughtercard)	15
5.4.	Debug Connectors (P8, P10)	16
5.4.1.	Debug Connector Pinouts.....	16
6.	COMMUNICATIONS & MEMORY INTERFACES:.....	17
6.1.	CAN Interfaces (P14, P15, J14, J15).....	17
6.2.	LIN Interfaces (P9, P11, J10, J12).....	18
6.3.	USB RS232 Serial Interface (P17, J16).....	19
6.4.	USB HOST / OTG Interfaces	20
6.5.	Ethernet (P6, J5, J6, J7, J8, R45, R80).....	20
6.6.	FlexRay (P2, P3, J1, J2, J3, J4).....	22
6.7.	SD Card Socket (P200).....	23
7.	AV INTERFACE CONNECTORS.....	23
7.1.	SAI Audio Connectors (P24, P25).....	23
7.2.	TWRPI Connectors (P26, P27).....	25
7.3.	MLB Daughtercard Connector (P16).....	25
8.	USER INTERFACE (I/O).....	26
8.1.	GPIO Matrix	26
8.2.	User Switches (SW3, SW4, SW6, SW7, P22)	27
8.3.	Hex Encoder Switch (SW2, J26, P20)	28
8.4.	User LED's (DS2, DS3, DS7, DS8, P19)	29
8.5.	ADC Input Potentiometer (J17, RV1)	29
9.	MCU PORT PIN EVB FUNCTIONS	30
10.	DEFAULT JUMPER SUMMARY TABLE	31
11.	DEFAULT JUMPER DIAGRAM	33
12.	REVISION HISTORY	33
13.	APPENDIX.....	34

1. Introduction

This user guide details the setup and configuration of the Freescale MPC5748G customer Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy evaluation of the MPC5748G family of microcontrollers, and to facilitate hardware and software development. Various daughtercards are available which connect to the EVB via two high density connectors. Please consult your Freescale representative for more details on daughtercard pricing and availability.

The EVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70°C).

This product contains components that may be damaged by electrostatic discharge. Observe precautions for handling electrostatic sensitive devices when using this EVB and associated microcontroller.

The user manual is intended to be read alongside the respective MCU documentation available at www.freescale.com and includes:

- Reference Manuals
- Product Data Sheets
- Application notes
- Chip Errata

1.1. Peripheral Daughtercards

The EVB has connectors for various peripheral daughtercards (for example MLB) that provide additional peripheral functionality. These are not supplied with the EVB and must be sourced separately. Please contact your Freescale representative for pricing and availability.

2. EVB Features

The EVB provides the following key features:

- Single 10-14 V DC external power supply input with on-board regulators to provide all of the necessary EVB and MCU voltages. Power may be supplied to the EVB via a 2.1 mm barrel style power jack or a 2-way screw type connector. 12 V operation allows in-car use if desired.
- Master power switch and regulator status LED's.
- USB Serial interface
- 2 x High Speed CAN transceiver routed to 3-way headers
- 2 x LIN interfaces routed to standard Molex headers
- Main clock supplied from on board crystal or SMA connector
- User reset switch with reset status LED's
- Ethernet PHY and RJ45 socket configurable as RMII or MII
- USB Type A Host interface
- USB Type AB (micro USB) OTG interface

- 2 x FlexRay interfaces with standard 2-pin connectors
- 14-pin JTAG and 50 pin Nexus (Trace) connectors
- 2 x High Density daughter card connectors allowing an MCU specific daughtercard to be fitted¹
- MLB daughtercard connector
- SAI Audio board connectors (2 x 0.1 inch pitch headers and 2 x TWRPI style headers)
- SD connector (mounted to the underside of the board) supporting hardware write protect and card detection
- 4 user LEDs wired to MCU ports, also available at a user header
- 4 user pushbutton switches wired to MCU ports, also available at a user header
- Hexadecimal encoded switch wired to 4 MCU ports, also available at a user header
- Simple potentiometer connected to analogue input channel

NOTE

To alleviate confusion between jumpers and connector headers, all EVB jumpers are 2 mm pitch whereas headers are 0.1 inch (2.54 mm). This prevents inadvertently fitting a jumper to a header.

¹ There is no MCU fitted to the EVB. A daughtercard must be fitted before the EVB can be used.

3. Configuration Overview

Throughout this document, all of the default jumper and switch settings are clearly marked with “(D)” and are shown in blue text. This allows a more rapid return to the default state of the EVB if required. Note that the default configuration for 3-way jumpers is a header fitted between pins 1 and 2. On the EVB, 2-way, and 3-way jumpers have been aligned such that pin1 is either to the top or to the left of the jumper. On 2-way jumpers, the source of the signal is connected to pin1.

The EVB has been designed with ease of use in mind and has been segmented into functional blocks as shown below. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

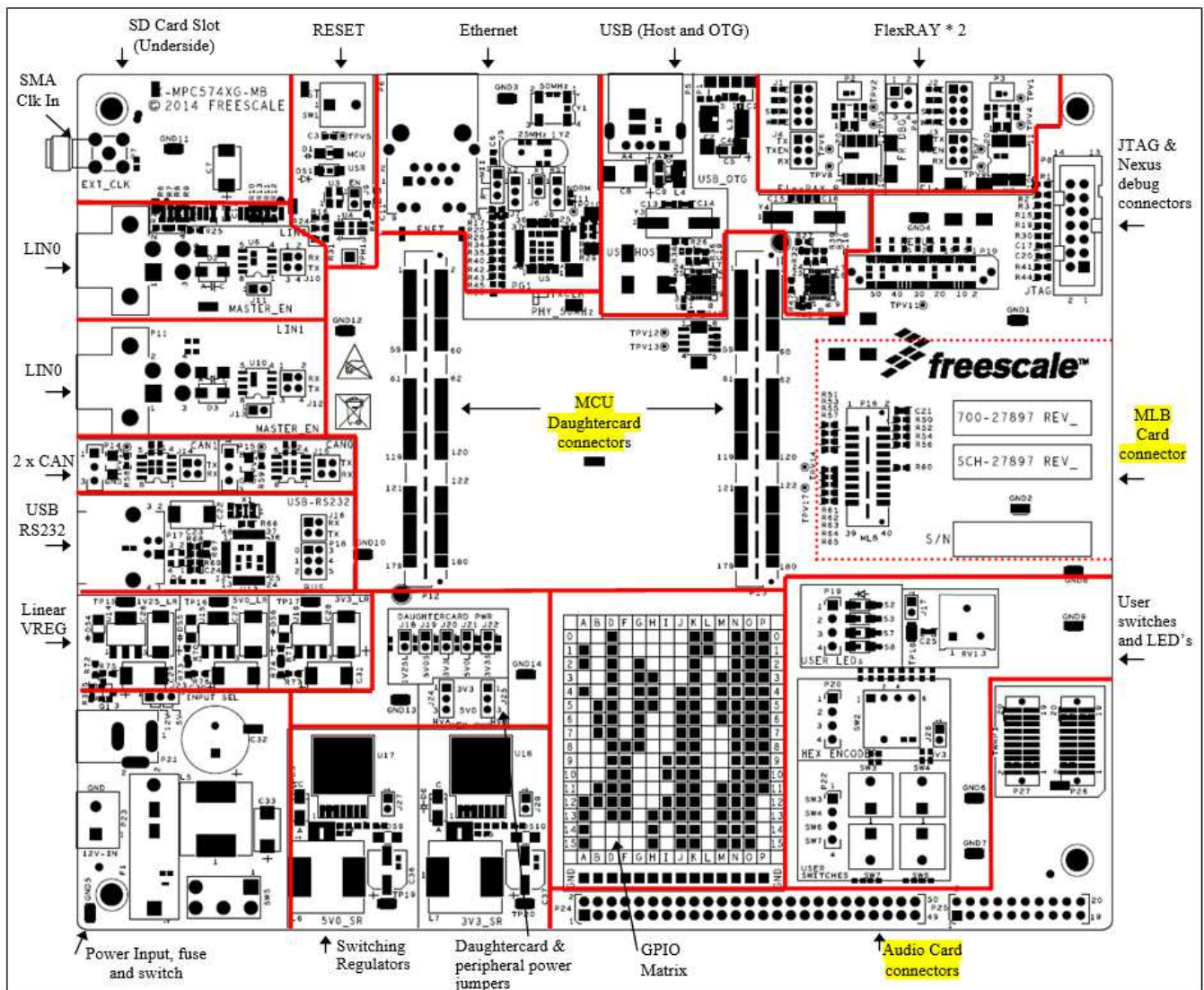


Figure 1. EVB Functional Blocks

4. MCU Daughtercard information

In order to use the EVB, an MCU daughtercard must be fitted as described in the following section. Before fitting or removing a daughtercard, ensure the EVB is powered OFF

4.1. Fitting a daughtercard

Gently place the daughtercard on the EVB connectors ensuring the correct orientation as shown in the following figure. The connectors are polarized so the daughtercard will only fit in one orientation (with the jumpers at the bottom of the daughtercard). Once the connectors have been located correctly, firmly push down all four corners of the daughter card simultaneously in order to ensure the connectors are mated. (The following picture also shows the default jumper positions for the 256BGA daughtercard)

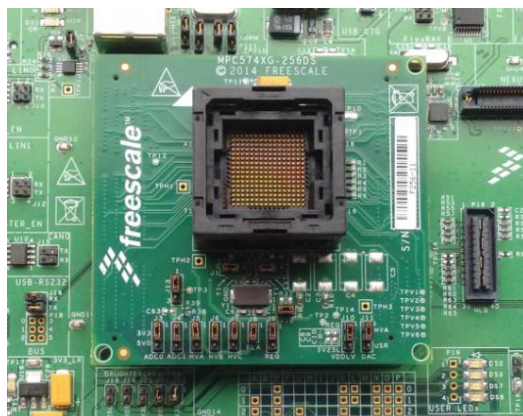


Figure 2. Daughtercard Fitted to EVB

4.2. Removing a daughtercard

In order to prevent damage to the daughtercard connectors, it is important to remove the daughtercard correctly. Carefully lift either the top or bottom edge of the daughtercard and it should easily lift off as shown in the following figure (viewed from the left side of the EVB).



Figure 3. Removing a daughtercard

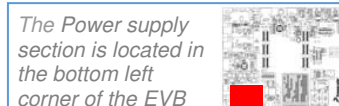
CAUTION

Do not attempt to lift the left or right edge of the daughtercard as this will result in connector damage.

5. Initial Configuration

This section details the power, reset, clocks, and debug configuration which is the minimum configuration needed in order to power ON the EVB.

5.1. Power Supply Configuration



The EVB requires an external power supply voltage of between 10 V-14 V DC (nominal 12 V), minimum 2 A. This allows the EVB to be used in a vehicle if required. The 12 V input is regulated on the EVB using two switching and three linear regulators to provide the required voltages of 5.0 V, 3.3 V (both linear and switcher) and 1.25 V (linear). For flexibility, there are two power supply input connectors on the EVB as detailed below:

5.1.1. Power Supply Connectors (P21, P23)

- **2.1 mm Barrel Connector – P21**

This connector should be used to connect the supplied wall-plug mains adapter. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1 mm plug uses the correct polarisation as shown below:

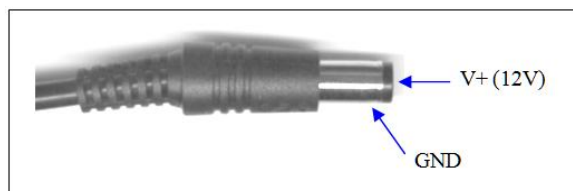


Figure 4. 2.1mm Power Connector

- **2-Way Screw Type Connector – P23**

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarisation of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

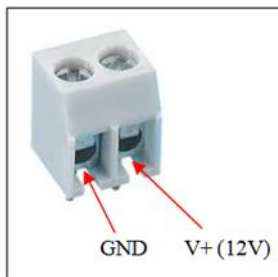


Figure 5. 2-Lever Power Connector

5.1.2. Power Switch (SW5)

Slide switch SW5 can be used to isolate the power supply input from the EVB voltage regulators if required.

- Moving the slide switch to the right (away from the fuse) will turn the EVB OFF.
- Moving the slide switch to the left (towards the fuse) will turn the EVB ON.

5.1.3. Regulator Power Jumper (J23)

All of the regulators are permanently powered from the main 12 V supply line and active with the exception of the 1.25 V linear regulator which has a 3-way jumper to allow selection of the input voltage.

The table below details the jumper configurations for the linear 1.25 V regulator source voltage. By default, the regulator is powered from the 12 V supply line.

Table 1. 1.25 V Linear Regulator Source Select (J23)

Jumper	Position	PCB Legend	Description
J23 (INPUT SEL)	1-2 (D)	12V	1.25V Linear regulator is powered from main 12V
	2-3	5V	1.25V Linear regulator is powered from 5V switching regulator output
	Removed		1.25V Linear regulator is not powered (disabled)

5.1.4. Power Status LED's and Fuse

When power is applied to the EVB, five green LED's adjacent to the voltage regulators show the presence of the supply voltages as follows:

- LED DS4 – Indicates that the 1.25V linear regulator is enabled and working correctly
- LED DS5 – Indicates that the 5.0V linear regulator is enabled and working correctly
- LED DS6 – Indicates that the 3.3V linear regulator is enabled and working correctly
- LED DS9 – Indicates that the 5.0V switching regulator is enabled and working correctly
- LED DS10 – Indicates that the 3.3V switching regulator is enabled and working correctly


If no LED's are illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power switch SW5 is in the "OFF" position or that the fuse F1 has blown. The fuse is provided to protect the external power supply and for EVB circuitry reverse-bias protection. If the fuse has blown, check the polarity of your power supply and replace the fuse with a 20 mm 1.5 A fast blow fuse.

Note that the fuse will not protect against one of the EVB regulators being shorted. If this happens, damage is likely to occur to the EVB and / or components.

CAUTION

In the event of a short in the regulator output, the regulator and/or the shorted component may be hot

5.1.5.MCU Power Supply Jumpers (J18, J19, J20, J21, J22, J23)

The MCU Daughtercard power jumpers are in the bottom left quarter of the EVB, above the power 

All of the regulated power supplies are routed to the MCU daughtercard via jumpers. This allows each power supply to be individually isolated and facilitates current measurement at the respective jumper.

Note that only the daughtercard is connected to the power lines after the jumpers so MCU current measurements are accurate. There are an additional two jumpers that control the voltages used by EVB peripherals connected to the VDD_HV_A and VDD_HV_B domains as described in section 5.1.7.

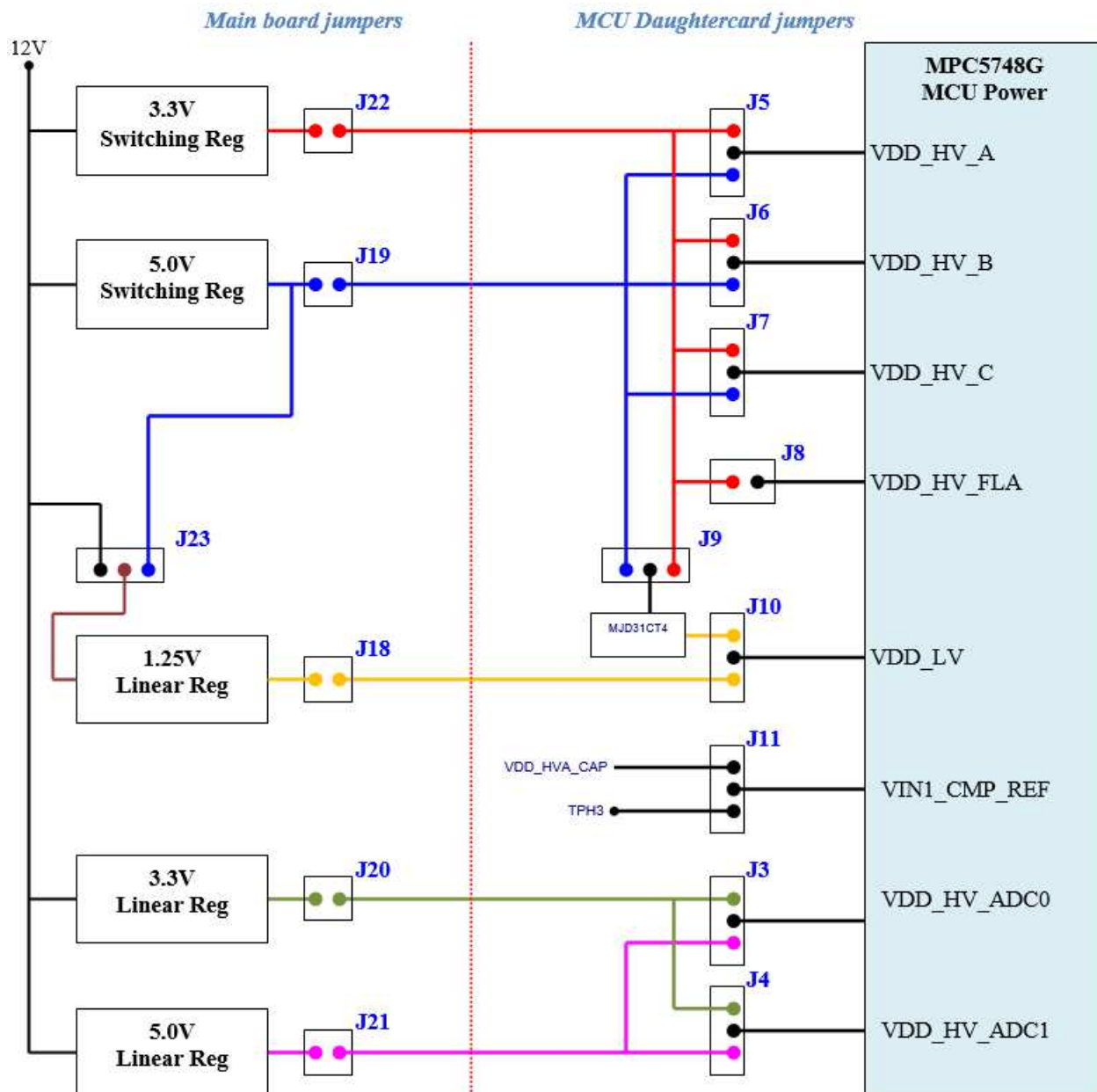


Figure 6. Power Supply Jumper Schematic

The power supply jumper description table is shown in the following table:

Table 2. Daughter Card Power Supply Jumpers (on main board)

Jumper	Position	PCB Legend	Description
J18 1V25L	Fitted (D)		1.25V Linear regulator output is routed to daughter card
	Removed		1.25V Linear regulator output is disconnected from daughtercard
J19 5V0S	Fitted (D)		5.0V Switching regulator output is routed to daughter card
	Removed		5.0V Switching regulator output is disconnected from daughtercard
J20 3V3L	Fitted (D)		3.3V Linear regulator output is routed to daughter card
	Removed		3.3V Linear regulator output is disconnected from daughtercard
J21 5V0L	Fitted (D)		5.0V Linear regulator output is routed to daughter card
	Removed		5.0V Linear regulator output is disconnected from daughtercard
J22 3V3S	Fitted (D)		3.3V Switching regulator output is routed to daughter card
	Removed		3.3V Switching regulator output is disconnected from daughtercard
J23 INPUT SEL (Above Power Jack)	1-2 (D)	12V	1.25v Linear regulator is powered by main 12V input
	2-3	5V	1.25v Linear regulator is powered by output from 5.0V switching reg
	Removed		1.25v Linear regulator is not powered (disabled)

5.1.6. Daughtercard Power Jumpers (J3 to J11)

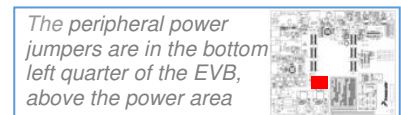
The following power control jumpers are located on the MCU daughtercard. Note that not all of the jumpers will be on each daughtercard variant.

Table 3. MCU Power Supply Jumpers (on daughtercard)

Jumper	Position	PCB Legend	Description
J3 ADC0	1-2 (D)	3V3	MCU ADC0 pin is connected to 3.3V (Linear)
	2-3	5V0	MCU ADC0 pin is connected to 5.0V (Linear)
	Removed		MCU ADC0 pin is not connected to power
J4 ADC1	1-2 (D)	3V3	MCU ADC1 pin is connected to 3.3V (Linear)
	2-3	5V0	MCU ADC1 pin is connected to 5.0V (Linear)
	Removed		MCU ADC1 pin is not connected to power
J5 HVA	1-2 (D)	3V3	MCU VDD_HV_A domain is connected to 3.3V (Switching Regulator)
	2-3	5V0	MCU VDD_HV_A domain is connected to 5.0V (Switching Regulator)
	Removed		MCU VDD_HV_A domain is not connected to power
J6 HVB	1-2 (D)	3V3	MCU VDD_HV_B domain is connected to 3.3V (Switching Regulator)
	2-3	5V0	MCU VDD_HV_B domain is connected to 5.0V (Switching Regulator)
	Removed		MCU VDD_HV_B domain is not connected to power
J7 HVC	1-2 (D)	3V3	MCU VDD_HV_C domain is connected to 3.3V (Switching Regulator)
	2-3	5V0	MCU VDD_HV_C domain is connected to 5.0V (Switching Regulator)
	Removed		MCU VDD_HV_C domain is not connected to power

Jumper	Position	PCB Legend	Description
J8² FLA	Fitted (D) Removed		MCU VDD_HV_FL A pin is connected to 3.3v (Switching Regulator) MCU VDD_HV_C domain is connected to 5.0V (Switching Regulator)
J9 REG	1-2 (D) 2-3 Removed	3V3 5V0	MCU ballast transistor collector is connected to 3.3V (Switching) MCU ballast transistor collector is connected to 5.0V(Switching) MCU ballast transistor collector is not connected to power
J10 VDDL V	1-2 (D) 2-3 Removed	REG 1V25L	MCU VDD_LV domain is powered from ballast transistor MCU VDD_LV domain is powered from 1.25V Linear regulator MCU VDD_LV domain is not powered
J11 DAC	1-2 (D) 2-3 Removed	HVA USR	MCU VIN1_CMP_REF is powered from VDD_HV_A MCU VIN1_CMP_REF is powered from user testpoint (TPH3) MCU VIN1_CMP_REF is not powered

5.1.7. Peripheral Power Supply Jumpers (J24, J25)



There are two additional power supply jumpers controlling the I/O voltage for the peripherals on the EVB in the HVA and HVB voltage domains.

The settings on these jumpers must match the VDD_HV_A and VDD_HV_B jumper voltage setting on the MCU daughtercard.

The default configuration matches the MCU daughtercard default configuration with both jumpers set to 3.3V.

Table 4. Peripheral Power Control (J24, J25)

Jumper	Position	PCB Legend	Description
J24 HVA	1-2 (D) 2-3 Removed	3V3 5V0	EVB peripherals in HVA domain are set to use I/O voltage of 3.3V EVB peripherals in HVA domain are set to use I/O voltage of 5.0V Invalid Configuration, avoid!
J25 HVB	1-2 (D) 2-3 Removed	3V3 5V0	EVB peripherals in HVB domain are set to use I/O voltage of 3.3V EVB peripherals in HVB domain are set to use I/O voltage of 5.0V Invalid Configuration, avoid!

5.1.8. EVB Voltage Regulators

The following table shows the usage of each EVB voltage regulator. This provides a useful cross reference point should any regulator be disabled. In addition, the distribution of the peripheral voltages HVA (J24) and HVB (J25) are shown.

² Note that jumper J8 (FLA) jumper must only be fitted when VDD_HV_A (J5) is connected to 3.3V.

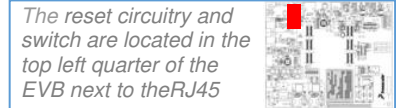
Table 5. Power Supply Distribution

Regulator	Used On
12V (Unregulated) P12V	All voltage regulators (switching and Linear, jumper selectable on 1.25V linear) 1.25V linear regulator LED supply via FET MCU Daughtercard connector MLB Daughtercard connector FlexRay transceiver VBAT pin
5.0V Switcher 5V0_SR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link) Peripheral power control jumpers (position 2-3) CAN transceivers VCC (main power) USB RS232 (FTDI) transceiver (main power and protection diode) USB Host / OTG transceiver power (VBAT) pin FlexRay Transceiver power pins (VCC / VBUF) SAI Audio connector Input to 1.25V linear regulator (in alternate jumper configuration)
3.3V Switcher 3V3_SR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link) Peripheral power control jumpers (position 1-2) Reset LED's (user and target) USB HOST / OTG transceiver I/O voltage (USB operation is fixed at 3.3V) ³ Ethernet Transceiver supply and I/O (Ethernet operation is fixed at 3.3V) ³ SAI Audio connector MLB Daughtercard connector SD Card power supply / pullup resistors (SD Card operation is fixed at 3.3V) ³ User LED's supply voltage Hex encoder switch supply voltage User pushbutton switches supply voltage
5.0V Linear 5V0_LR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link)
3.3V Linear 3V3_LR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link) MLB Daughtercard connector ADC Input Pot (user variable resistor)
1.25V Linear 1V25_LR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link)
J24 PER_HVA	Reset control circuitry (including reset pullup) JTAG Pullup resistors & reference voltage CAN Transceiver I/O Voltage select LIN Transceiver Enable (and I/O voltage select) USB RS232 (FTDI) transceiver I/O voltage select FlexRay Transceiver I/O Voltage select (and pullups)
J25 PER_HVB	Nexus Connector reference voltage and Pullups

³ These voltages are fixed due to device specifications and cannot be changed.

Note that the JTAG pins are in domain VDD_HV_A whereas the Nexus pins are VDD_HV_B. Normally this would mean that for trace, the HVA and HVB domains should be at the same voltage however some development tools can automatically adapt to the voltages on the trace signals. Please consult your tools vendor for further details.

5.2. Reset Control (J9, SW1)



The MCU has a single bi-directional open drain Reset pin. Rather than connect multiple devices to the reset pin directly, a reset-in and reset-out buffering scheme has been implemented on the EVB as shown in Figure 7 below. The reset “in” from the reset switch (SW1) and the debug connectors are logically OR’d together using an AND gate and then connected to the buffer to provide an open-drain output.

The “reset-out” circuitry provides a buffered reset signal that can be used to drive any circuitry requiring a reset control from the MCU.

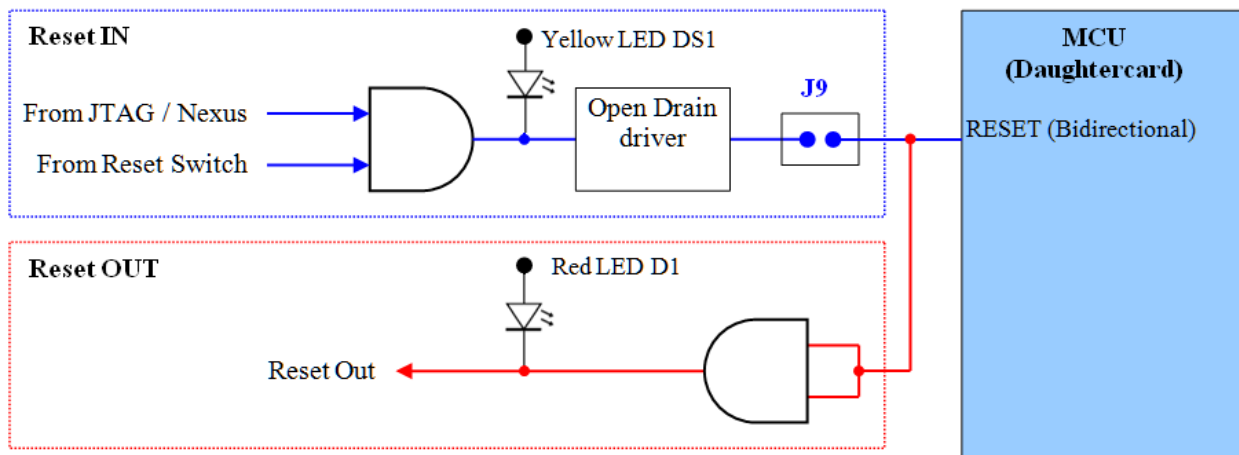


Figure 7. EVB Reset Control

Jumper J9 is used to disconnect the reset signal from the external reset sources if required.

Table 6. Reset Control (J9)

Jumper	Position	PCB Legend	Description
J9 (EN)	Fitted (D)		Reset from reset switch and debug connectors is active
	Removed		Reset from reset switch and debug connectors is inactive

Note that removing jumper J9 will mean that an external reset source will not reset the MCU. This will impact most debuggers which will typically issue a reset before establishing a debug connection.

5.2.1. Reset LEDs

As can be seen in Figure 7 above, there are two reset LED’s that can be used to identify the source / cause of a reset:

RED LED D1 (titled “MCU”) will illuminate if:

- The MCU issues a reset (in this condition ONLY this LED will be illuminated and LED DS1 will be off)
- There is a target reset (ie from the reset switch or from the debugger in which case LED DS1 will be ON)

YELLOW LED DS1 (titled “USR”) will illuminate when an external hardware device issues a reset to the MCU:

- The reset switch is pressed
- There is a reset being driven from one of the debug connectors

Table 7. Reset LED Decoding

LED DS1 (Yellow)	LED D1 (Red)	Description
OFF	OFF	No Reset being issued from MCU or external logic
OFF	ON	MCU has issued a reset
ON	OFF	External reset issued from switch or debug BUT not being issued to MCU (check J9 is fitted on the EVB)
ON	ON	External reset issued from reset switch or debug and has been issued to MCU.

5.3. MCU Clock Configuration

There are 2 clock configuration jumpers on the daughtercard and an external clock input connector on the main board to allow an externally generated clock to be supplied if desired. See Figure 8 below.

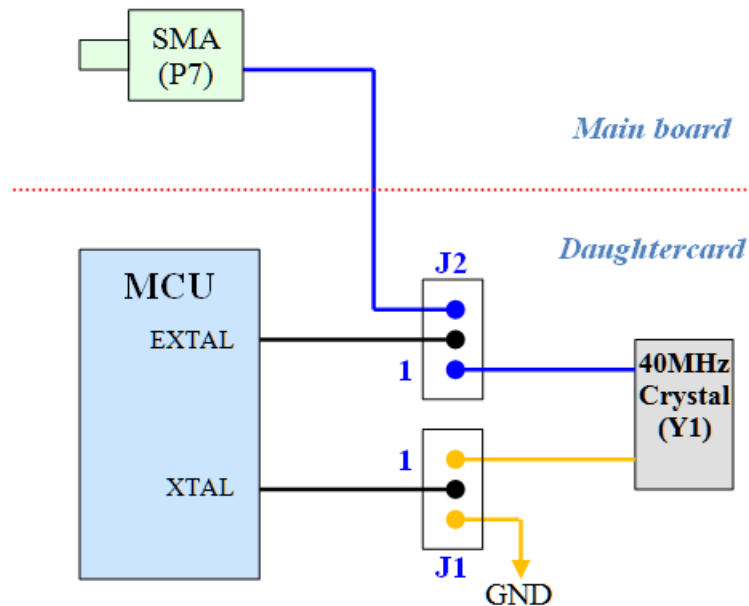
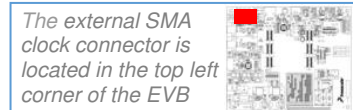


Figure 8. EVB Clock Selection

5.3.1. External Clock Input (P7)



The external clock input on the EVB is applied via SMA connector P7. When driving an external clock into the SMA connector, the jumpers on the daughtercard must be reconfigured to route the external clock to the MCU.

Note that the following conditions must be met when supplying an external clock:

- The clock frequency must be between 8MHz and 40MHz
- The amplitude of the clock input should not exceed the voltage being driven into the VDD_HV_A pins. This is selectable between 3.3V and 5.0V on the daughtercard.

5.3.2. MCU Clock Configuration (J1, J2 on Daughtercard)

There are two external clock crystals on the MPC5748G daughtercards:

- 40MHz fast external crystal for clocking the main system clock
- 32KHz slow external crystal for accurate time of day keeping

The 40MHz crystal is connected to the MCU XTAL and EXTAL pins via 3-way jumper headers as shown in the diagram above. These jumpers allow an external clock to be routed from the SMA connector (P7) on the main board if desired. The default configuration is with both daughtercard jumpers (J1 and J2) set to position 1-2 which routes the external 40MHz crystal to the MCU pins. If you wish to supply a clock via the SMA connector on the main EVB, move the daughtercard jumpers J1 and J2 to position 2-3.

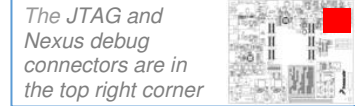
The 32 KHz external crystal is permanently connected to the MCU EXTAL32 and XTAL32 pins and has no configuration options.

Table 8. EXTAL Clock Source Selection (J1, J2 Daughtercard)

Jumper	Position	PCB Legend	Description
J1 (XTAL)	1-2 (D)	Y1	MCU XTAL signal is routed to crystal Y1
	2-3	GND	MCU XTAL signal is Grounded (for ext clock mode) ⁴
J2 (EXTAL)	1-2 (D)	Y1	MCU EXTAL signal is routed to crystal Y1
	2-3	EXT	MCU EXTAL signal is routed from EVB SMA P7

⁴ Note that the XTAL pin is left open by default with J1 in position 2-3. Resistor R34 must be populated with a zero ohm resistor in order to ground the XTAL pin.

5.4. Debug Connectors (P8, P10)



The EVB provides two debug connectors:

- Standard 14 pin JTAG
- 50 Pin Nexus connector (Samtec ASP-148422-01, Nexus Standard HP50 connector)

There is no user configuration required to use the connectors however the following points should be noted:

- The JTAG connector is routed to the JTAG signals in the default position which are powered from the MCU VDD_HV_A power domain. The Nexus signals are located in the VDD_HV_B power domain. If you are using Nexus, you may have to ensure that the VDD_HV_A and VDD_HV_B domains are at the same voltage. Consult your tools vendor for specific information
- The Nexus signals are not bonded out in every MCU package. Before using Nexus, please ensure the MCU fitted to the EVB (via the daughtercard) supports the Nexus signals.

5.4.1. Debug Connector Pinouts

The following tables list the pinouts for each of the debug connectors used on the EVB

Table 9. 14-Pin JTAG Debug Connector Pinout

Pin No	Function	Connection	Pin No	Function	Connection
1	TDI	PC0	2	GND	GND
3	TDO	PC1	4	GND	GND
5	TCLK	PH9	6	GND	GND
7	EVTI	PL8	8	N/C	---
9	RESET	JTAG-RSTx	10	TMS	PH10
11	VREF	PER_HVA	12	GND	GND
13	RDY	---	14	JCOMP	10K Pulldown

Table 10. 50-pin Samtec (Nexus) Debug Connector Pinout

Pin No	Function	Connection	Pin No	Function	Connection
1	MSEO_0	PL9	2	VREF	PER_HVB
3	MSEO_1	PL11	4	TCK	PH9
5	GND	GND	6	TMS	PH10
7	MDO0	PL2	8	TDI	PC0
9	MDO1	PL3	10	TDO	PC1
11	GND	GND	12	JCOMP	10K Pulldown
13	MDO2	PL4	14	RDY	---
15	MDO3	PL5	16	EVTI	PL8
17	GND	GND	18	EVTO	PL12
19	MCKO	PL10	20	RESET	DEBUG_RST
21	MDO4	PL6	22	RST_OUT	MCU_RST
23	GND	GND	24	GND	GND
25	MDO5	PL7	26	CLKOUT	Test Point
27	MDO6	PL13	28	TD/WT	---
29	GND	GND	30	GND	GND

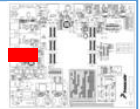
Pin No	Function	Connection	Pin No	Function	Connection
31	MDO7	PL14	32	DAI1	---
33	MDO8	PL15	34	DAI2	---
35	GND	GND	36	GND	GND
37	MDO9	PM0	38	ARBREQ	---
39	MDO10	PM1	40	ARBGRT	---
41	GND	GND	42	GND	GND
43	MD011	PM2	44	MDO13	PM8
45	MDO12	PM7	46	MDO14	PM9
47	GND	GND	48	GND	GND
49	MDO15	PM10	50	N/C	---

6. Communications & Memory Interfaces:

This section details the communication interface and storage peripherals that are implemented on the EVB.

6.1. CAN Interfaces (P14, P15, J14, J15)

The CAN Physical interface circuits are located on the left edge of the EVB



The EVB incorporates two identical CAN interface circuits connected to MCU CAN0 and CAN1 using MC33901 transceivers. Both transceivers are configured for high speed operation by pulling pin 8 to GND via a 4.7K Ohm resistor. There are test points to allow the Select pin to be driven high if desired. The MC33901 is pin compatible with other CAN transceivers supporting full CAN FD data rates.

For flexibility, the CAN transceiver I/O is connected to a standard 0.1" connector (P14 for CAN1 / P15 for CAN0) rather than using non standard DB9 connectors. The pinout of these headers is shown below and is also detailed on the PCB silkscreen

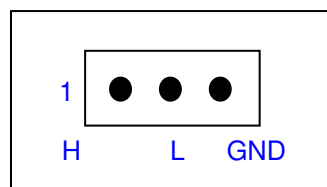


Figure 9. CAN Physical Interface Connectors

The CAN0 and CAN1 MCU TX/RX signals are jumpered as shown in the table below to allow the transceivers to be isolated from the respective MCU pin if desired. The default configuration is with all jumper headers fitted routing the TX and RX signals to the MCU.

Table 11. CAN Control Jumpers (J51, J53)

Jumper	Position	PCB Legend	Description
J15 (CAN0) Posn 1-2	FITTED (D) Removed	TX	MCU CAN0_TX signal (PB0) is routed to CAN interface MCU CAN0_TX signal (PB0) is not routed to CAN interface
J15 (CAN0) Posn 3-4	FITTED (D) Removed	RX	MCU CAN0_RX signal (PB1) is routed to CAN interface MCU CAN0_RX signal (PB1) is not routed to CAN interface
J14 (CAN1) Posn 1-2	FITTED (D) Removed	TX	MCU CAN1_TX signal (PC10) is routed to CAN interface MCU CAN1_TX signal (PC10) is not routed to CAN interface
J14 (CAN1) Posn 3-4	FITTED (D) Removed	RX	MCU CAN1_RX signal (PC11) is routed to CAN interface MCU CAN1_RX signal (PC11) is not routed to CAN interface


NOTE

Care should be taken when fitting the jumper headers to the 2x2 jumper blocks J14 and J15 as they can easily be fitted in the incorrect orientation. Jumper headers should be fitted **horizontally**.

The CAN TX / RX MCU pins are powered from the VDD_HV_A domain, which is configured between 3.3V and 5.0V on the daughtercard using jumper J5. The CAN transceivers I/O voltage is connected to the PER_HVA net configured with jumper J24 on the main EVB. Care must be taken to ensure that the MCU VDD_HV_A and PER_HVA supplies are the same when using the CAN transceiver.

6.2. LIN Interfaces (P9, P11, J10, J12)

The LIN Physical interface circuits are located on the left edge of the EVB



The EVB incorporates two identical LIN transceiver circuits connected to MCU LIN0 and LIN1 using a Freescale MC33662LEF transceiver supporting both master and slave mode (jumper selectable)

The output from the LIN transceiver is connected to a standard 4-pin Molex connector as used on most other Freescale EVB's supporting LIN as shown in the following figure:

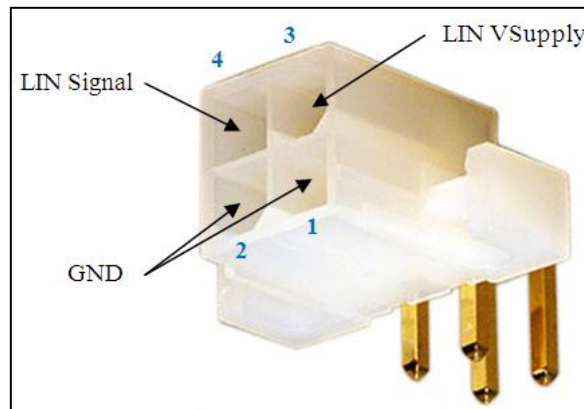


Figure 10. LIN Molex Physical Interface Connector

The LIN0 and LIN1 MCU TX/RX signals are jumpered as shown in the following to allow the transceivers to be isolated from the respective MCU pin if desired. The default configuration is with all jumper headers fitted routing the TX and RX signals to the MCU.

Each transceiver also has a master mode enable jumper which is fitted by default to configure the transceiver for Master mode. To configure the transceiver for slave mode, remove the respective “Master_EN” jumper.

Table 12. LIN Control Jumpers (J10, J11, J12, J13)

Jumper	Position	PCB Legend	Description
J10 (LIN0) Posn 1-2	FITTED (D) Removed	RX	MCU LIN0_RX signal (PB3) is routed to LIN0 interface MCU LIN0_RX signal (PB3) is not routed to LIN0 interface
J10 (LIN0) Posn 3-4	FITTED (D) Removed	TX	MCU LIN0_TX signal (PB2) is routed to LIN0 interface MCU LIN0_TX signal (PB2) is not routed to LIN0 interface
J11 (Master_EN)	FITTED (D) Removed		LIN0 is configured in Master Mode LIN0 is configured in Slave Mode
J12 (LIN1) Posn 1-2	FITTED (D) Removed	RX	MCU LIN1_TX signal (PC7) is routed to LIN1 interface MCU LIN1_TX signal (PC7) is not routed to LIN1 interface
J12 (LIN1) Posn 3-4	FITTED (D) Removed	TX	MCU LIN1_RX signal (PC6) is routed to LIN interface MCU LIN1_RX signal (PC6) is not routed to LIN interface
J13 (Master_EN)	FITTED (D) Removed		LIN1 is configured in Master Mode LIN1 is configured in Slave Mode

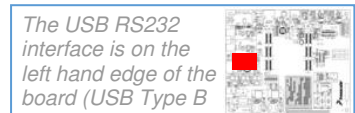
NOTE

Care should be taken when fitting the jumper headers to the 2x2 jumper blocks J10 and J12 as they can easily be fitted in the incorrect orientation. Jumper headers should be fitted **horizontally**

The LIN TX / RX MCU pins are powered from the VDD_HV_A domain, which is configured between 3.3V and 5.0V on the daughtercard using jumper J5. The LIN transceivers enable pin is connected to the PER_HVA net configured with jumper J24 on the main EVB. Care must be taken to ensure that the MCU VDD_HV_A and PER_HVA supplies are the same when using the LIN transceiver.

Note that in order for the LIN transceiver to function, external power must be supplied via pin 3 of the molex connector as detailed in Figure 10.

6.3. USB RS232 Serial Interface (P17, J16)



The EVB incorporates a USB RS232 serial interface providing RS232 connectivity via a direct USB connection between the PC and the EVB. The circuit contains an FTDI FT2232D USB to Serial interface which should automatically install the drivers for two additional COM ports on your PC. Note that only one of these is used so you will need to try both (usually the higher numbered COM port is the active one). For more information on the USB drivers and general fault finding, consult the FTDI website at <http://www.ftdichip.com/>

The MCU LIN2 signals are routed to the FTDI transceiver via a 2-way jumper header (J16) allowing the transceiver to be isolated from the MCU pin if desired. The default configuration is with the jumper

header fitted, routing the TX and RX signals from the MCU to the FTDI transceiver. No other configuration is required.

Table 13. USB RS232 Control Jumpers

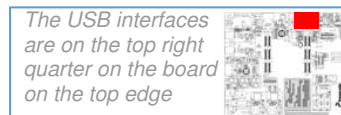
Jumper	Position	PCB Legend	Description
J16 Posn 1-2	FITTED (D) Removed	RX	MCU LIN2_RX signal (PC9) is routed to the FTDI interface MCU LIN2_RX signal (PC9) is not routed to the FTDI interface
J16 Posn 3-4	FITTED (D) Removed	TX	MCU LIN2_TX signal (PC8) is routed to the FTDI interface MCU LIN2_TX signal (PC8) is not routed to the FTDI interface

NOTE

Care should be taken when fitting the jumper headers to the 2x2 jumper block J16 as they can easily be fitted in the incorrect orientation. Jumper headers should be fitted **horizontally**.

The MCU LIN2 (SCI) pins are powered from the VDD_HV_A domain, which is configured between 3.3V and 5.0V on the daughtercard using jumper J5. The FTDI transceiver I/O voltage pin is connected to the PER_HVA net configured with jumper J24 on the main EVB. Care must be taken to ensure that the MCU VDD_HV_A and PER_HVA supplies are the same when using the FTDI transceiver.

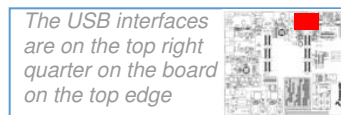
6.4. USB HOST / OTG Interfaces



The EVB includes Type A (Host) and Type AB (OTG) USB interfaces, routed to standard and micro USB sockets respectively. Each USB circuit contains a USB83340 transceiver with a shared USB power switch. There is no user configuration required on either of the USB circuits.

The USB transceivers have a 3.3V (only) interface. All of the USB0 (connected to the OTG transceiver) and USB1 (connected to the HOST transceiver) signals are in the VDD_HV_A domain and must be configured as 3.3V via daughtercard jumper J5. If VDD_HV_A is set to 5V, the USB0 and USB1 MCU signals should be left tri-stated to prevent damage to the USB transceivers.

6.5. Ethernet (P6, J5, J6, J7, J8, R45, R80)



The MPC5748G supports both MII and RMII Ethernet interfaces. The EVB incorporates a DP83848c transceiver supporting both MII and RMII modes. The transceiver is connected to a pulse J1011F21PNL RJ45 connector which includes a built-in isolation transformer.

The default configuration, with all 2-way jumpers fitted and all 3-way jumpers in position 1-2, configures the transceiver for MII mode with the reset signal to the PHY being driven from the MCU Reset out (eg any reset causing the MCU Reset line to assert will reset the PHY)

In order to configure the EVB for RMII mode, jumpers J5, J6 and J7 need to be changed as described in Table 14 below. In addition, a surface mount 0Ω resistor needs to be de-soldered and moved as shown in the figure below. This option is fitted as a resistor instead of a jumper to maintain signal integrity on the Ethernet clock signal.

For MII mode (default) R45 should have a jumper populated as shown. For RMII mode, remove R45 and fit it between R45 and R80

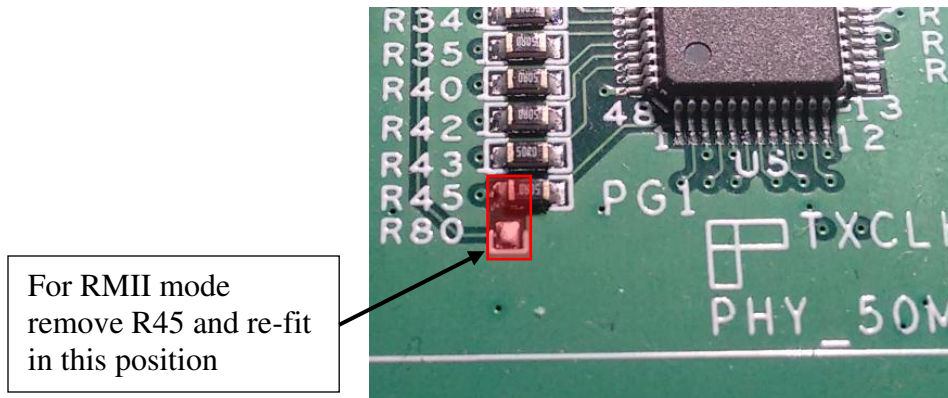


Figure 11. MII / RMII Clock Selection Resistor

To change the reset routing so that the Ethernet PHY can be reset via MCU pin PI11 (rather than being tied to the MCU reset), jumper J8 should be moved to position 2-3

Table 14. Ethernet Control jumpers (J5, J6, J7, J8, R45, R80)

Jumper	Position	PCB Legend	Description
J5	1-2 (D)	MII	Ethernet PHY is configured in MII mode
	2-3	R	Ethernet PHY is configured in RMII mode
	Removed		Invalid Configuration, avoid!
J6 (X1)	1-2 (D)		Ethernet PHY X2 clock is connected to 25MHz xtal
	2-3		Ethernet PHY X2 clock is not connected to 25MHz xtal ^{5, 6}
J7 (X2)	1-2 (D)		Ethernet PHY X1 clock is connected to 25MHz xtal
	2-3		Ethernet PHY X1 clock is driven from 50MHz xtal
	Removed		Ethernet PHY X1 clock is disconnected (invalid configuration, avoid)
J8 (RST)	1-2 (D)	NORM	The Ethernet PHY will be reset along with MCU reset
	2-3	PI11	The Ethernet PHY reset is controlled via MCU pin PI11 (Pulled high)
	Removed		Invalid Configuration, avoid!
R45 (R80)	Fitted R45		MII Mode – Clock is supplied from PHY to MCU
	R45 to R80		RMII Mode – Clock is supplied from external 50MHz oscillator to MCU

The MCU Ethernet signals are all in the VDD_HV_B domain. The Ethernet PHY will ONLY function with 3.3V I/O so VDD_HV_B must be set to 3.3V on the MCU daughtercard before the Ethernet is used. If VDD_HV_B is set to 5V, the signals routed to the Ethernet PHY (see the EVB schematics) must be left as tristate.

⁵ If jumper J7 is in position 1-2 (25MHz XTAL), J6 must be fitted and R45 must be fitted.

⁶ If jumper J7 is in position 2-3 (50MHz oscillator), J6 must be removed and R45 must be removed and placed between R45 and R80

6.6. FlexRay (P2, P3, J1, J2, J3, J4)



The EVB incorporates two FlexRay TJA1080TS/N interfaces connected to MCU FlexRay channels A and B and routed to two Molex 1.25mm pitch PicoBlade shrouded headers (standard on many Freescale EVB's). Jumpers are provided to disconnect the MCU signals from the FlexRay interface if required as well as providing general configuration.

By default, all of the jumper headers are fitted which routes the MCU signals to the FlexRay physical interface as well as configuring the controller for a default mode of operation (Transmitter enabled, Receiver enabled, not in low power mode). Please consult the FlexRay transceiver and general FlexRay specifications before changing any of the mode jumpers.

Table 15. FlexRay Configuration Jumpers (J1, J2, J3, J4)

Jumper	Position	PCB Legend	Description
FlexRay A			
J3 Posn 1-2	FITTED (D) Removed	TX	MCU PC5 is connected to FlexRay A transceiver TX MCU PC5 is not connected to FlexRay A transceiver TX
J3 Posn 3-4	FITTED (D) Removed	TXEN	MCU PE2 is connected to FlexRay A transceiver TXEN MCU PE2 is not connected to FlexRay A transceiver TXEN
J3 Posn 5-6	FITTED (D) Removed	RX	MCU PE3 is connected to FlexRay A transceiver RX MCU PE3 is not connected to FlexRay A transceiver RX
J2 Posn 1-2	FITTED (D) Removed	BGE	FlexRay A PHY Bus Guardian Enable (Transmitter is enabled) FlexRay A PHY transmitter is disabled (Receive only mode)
J2 Posn 3-4	FITTED (D) Removed	EN	FlexRay A PHY is enabled FlexRay A PHY is disabled
J2 Posn 5-6	FITTED (D) Removed	STBN	FlexRay A PHY will not enter Standby Mode FlexRay A PHY will enter Standby Mode
J2 Posn 7-8	FITTED (D) Removed	WAKE	FlexRay A PHY Wakeup signal pulled low FlexRay A PHY Wakeup signal pulled high
FlexRay B			
J4 Posn 1-2	FITTED (D) Removed	TX	MCU PE4 is connected to FlexRay B transceiver TX MCU PE4 is not connected to FlexRay B transceiver TX
J4 Posn 3-4	FITTED (D) Removed	TXEN	MCU PC4 is connected to FlexRay B transceiver TXEN MCU PC4 is not connected to FlexRay B transceiver TXEN
J4 Posn 5-6	FITTED (D) Removed	RX	MCU PE5 is connected to FlexRay B transceiver RX MCU PE5 is not connected to FlexRay B transceiver RX
J1 Posn 1-2	FITTED (D) Removed	BGE	FlexRay B PHY Bus Guardian Enable (Transmitter is enabled) FlexRay B PHY transmitter is disabled (Receive only mode)
J1 Posn 3-4	FITTED (D) Removed	EN	FlexRay B PHY is enabled FlexRay B PHY is disabled
J1 Posn 5-6	FITTED (D) Removed	STBN	FlexRay B PHY will not enter Standby Mode FlexRay B PHY will enter Standby Mode
J1 Posn 7-8	FITTED (D) Removed	WAKE	FlexRay B PHY Wakeup signal pulled low FlexRay B PHY Wakeup signal pulled high

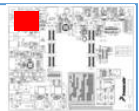
The MCU FlexRay pins are powered from the VDD_HV_A domain, which is configured between 3.3V and 5.0 V on the daughtercard using jumper J5. The FlexRay transceivers I/O voltage pin is connected to the PER_HVA net configured with jumper J24 on the main EVB. Care must be taken to ensure that the MCU VDD_HV_A and PER_HVA supplies are the same when using the FlexRay transceiver.

Important:

The EVB daughtercards are supplied with a 40 MHz crystal which is a requirement for FlexRay in order to generate the correct clock timing. If you have changed the default crystal on the daughtercard and wish to use FlexRay, you must ensure a 40 MHz crystal is fitted.

6.7. SD Card Socket (P200)

The SD socket is mounted on the underside of the board in the top left



The EVB supports a 4-bit SD interface (note that MPC5748G supports 8-bit SD data) which is routed to a full sized SD card connector on the underside of the EVB. There is no user configuration required.

The SD socket has hardware card detection (routed to PA0) and write protection (routed to PH8) status outputs which will be grounded when active.

The MCU SD card signals are all in the VDD_HV_A domain. The SD card specification is for an interface voltage of between 2.7V and 3.6V so the SD card can only be used when VDD_HV_A is set to 3.3V (PER_HVA has no impact on the voltage on the SD card)

CAUTION

If VDD_HV_A is set to 5V, damage may be caused to an SD card if an attempt is made to access it in software. If you need to leave the SD card in the socket with VDD_HV_A set to 5V, ensure all the SD card pads are left as high impedance

7. AV Interface Connectors

This section details the Audio / Video interface connectors on the EVB. Each of these connectors can be used to add additional daughtercards (not supplied) to add functionality.

7.1. SAI Audio Connectors (P24, P25)

The SAI audio connector is on the bottom edge of the EVB



The EVB includes two 0.1" headers that can be used to interface to an SAI audio board (available separately, please consult your Freescale representative). There is no EVB configuration required when using these connectors other than to ensure the EVB is switched off prior to fitting or removing the daughtercard.

The pinout of the connectors is shown below for reference and these connectors can also be used for GPIO connectivity

Table 16. 50-pin SAI Audio Daughtercard Connector P24

Pin No	Function	Connection	Pin No	Function	Connection
1	3.3V	3V3_SR	2	GND	GND
3	SAI0_DATA3	PF2	4	GND	GND
5	SAI0_DATA2	PF3	6	GND	GND
7	SAI0_DATA1	PF4	8	GND	GND
9	SAI0_DATA0	PF5	10	GND	GND
11	SAI0_BCLK	PF1	12	GND	GND
13	SAI0_SYNC	PB10	14	GND	GND
15	SAI0_MCLK	PF0	16	GND	GND
17	eMIOS1_7H	PH5	18	GND	GND
19	I2C_SCL3	PE11	20	GND	GND
21	I2C_SDA3	PE10	22	GND	GND
23	SAI1_DATA0	PJ2	24	GND	GND
25	SAI1_BCLK	PJ3	26	GND	GND
27	eMIOS1_6H	PH4	28	GND	GND
29	SAI1_SYNC	PF6	30	GND	GND
31	SAI1_MCLK	PF7	32	GND	GND
33	I2C_SCL2	PE9	34	GND	GND
35	I2C_SDA2	PE8	36	GND	GND
37	SAI2_DATA0	PI14	38	GND	GND
39	SAI2_BCLK	PJ1	40	GND	GND
41	SAI2_SYNC	PJ0	42	GND	GND
43	SAI2_MCLK	PI15	44	GND	GND
45	eMIOS1_5H	PH3	46	GND	GND
47	GPIO Control	PA5	48	GND	GND
49	5.0V	5V0_SR	50	GND	GND

Table 17. 20-pin SAI Audio Daughtercard Connector P25

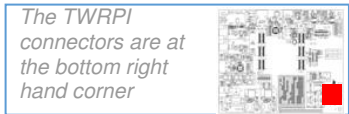
Pin No	Function	Connection	Pin No	Function	Connection
1	N/C	N/C	2	GND	GND
3	DSPI0_SIN	PA12	4	GND	GND
5	DSPI0_SOUT	PA13	6	GND	GND
7	DSPI0_SCK	PA14	8	GND	GND
9	DSPI0_SS0	PA15	10	GND	GND
11	DSPI3_SOUT	PG2	12	GND	GND
13	DSPI3_SS3	PG3	14	GND	GND
15	DSPI3_SCK	PG4	16	GND	GND
17	DSPI3_SIN	PG5	18	GND	GND
19	N/C	N/C	20	GND	GND

Note that connector P25 is not populated and must be fitted if required

CAUTION

Before the daughtercard is installed or removed, the EVB must be powered OFF to prevent potential damage to the EVB or daughter card components.

7.2. TWRPI Connectors (P26, P27)



The EVB includes two fine pitch TWRPI headers that can be used to interface to an SAI audio board (available separately, please consult your Freescale representative) along with the 0.1" headers mentioned in the section above. There is no EVB configuration required when using these connectors other than to ensure the EVB is switched off prior to fitting or removing the daughtercard. The pinout of the connectors is shown below for reference.

Table 18. TWRPI Connector P26

Pin No	Function	Connection	Pin No	Function	Connection
1	5V	5V0_SR	2	3.3V	3V3_SR
3	GND	GND	4	3.3V	3V3_LR
5	GND	GND	6	GND	GND
7	GND	GND	8	ADC0	PD5
9	ADC1	PD6	10	GND	GND
11	GND	GND	12	ADC2	PD4
13	GND	GND	14	GND	GND
15	GND	GND	16	GND	GND
17	ID0	PD7 ⁷	18	ID1 ⁷	PD8
19	GND	GND	20		

Table 19. TWRPI Connector P27

Pin No	Function	Connection	Pin No	Function	Connection
1	GND	GND	2	GND	GND
3	I2C0_SCL	PO0	4	I2C0_SDA	PO1
5	GND	GND	6	GND	GND
7	GND	GND	8	GND	GND
9	DSPIO_SIN	PA12	10	DSPIO_SOUT	PA13
11	DSPIO_SS0	PA15	12	DSPIO_SCK	PA14
13	GND	GND	14	GND	GND
15	GPIO0/IRQ	PK3	16	GPIO1	PK0
17	GPIO2	PK1	18	GPIO3	PK2
19	GPIO4	PK4	20	N/C	N/C

7.3. MLB Daughtercard Connector (P16)



There is a 40-pin interface connector on the EVB for connecting an MLB (Media Local Bus) daughtercard. There is no hardware configuration possible at EVB level for this connector.

MLB Daughtercards are available direct from SMSC

As with all daughtercards, the EVB must be powered OFF to prevent damage to the EVB or daughter card components.

⁷ ID0 and ID1 have a 10K pullup to 3V3