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**NXP Semiconductors**
Data Sheet: Technical Data

Document Number: MPC5777M
Rev. 6, 06/2016

# MPC5777M

416 TEPBGA
27mm x 27 mm

512 TEPBGA
25 mm x 25 mm

# MPC5777M Microcontroller Data Sheet

- Three main CPUs, single issue, 32-bit CPU core complexes (e200z7), one of which is a dedicated lockstep core.
  - Power Architecture® embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - 16 KB Local instruction RAM and 64 KB local data RAM
  - 16 KB I-Cache and 4 KB D-Cache
- I/O Processor, dual issue, 32-bit CPU core complex (e200z4), with
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - Lightweight Signal Processing Auxiliary Processing Unit (LSP APU) instruction support for digital signal processing (DSP)
  - 16 KB Local instruction RAM and 64 KB local data RAM
  - 8 KB I-Cache
- 8640 KB on-chip flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 404 KB on-chip general-purpose SRAM including 64 KB standby RAM (+ 192 KB data RAM included in the CPUs). Of this 404 KB, 64 KB can be powered by a separate supply so the contents of this portion can be preserved when the main MCU is powered down.
- Multichannel direct memory access controllers (eDMA): 2 x 64 channels per eDMA (128 channels total)
- Triple Interrupt controller (INTC)
  - Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Dual crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters with end-to-end ECC
- Hardware Security Module (HSM) to provide robust integrity checking of flash memory
- System Integration Unit Lite (SIUL)
- Boot Assist Module (BAM) supports factory programming using serial bootload through ‘UART Serial Boot Mode Protocol’. Physical interface (PHY) can be:
  - UART/LIN
  - CAN
- GTM104 — generic timer module
- Enhanced analog-to-digital converter system with
  - Twelve separate 12-bit SAR analog converters
  - Ten separate 16-bit Sigma-Delta analog converters
- Eight deserial serial peripheral interface (DSPI) modules
- Two Peripheral Sensor Interface (PSI5) controllers
- Three LIN and three UART communication interface (LINFlexD) modules (6 total)
  - LINFlexD_0 is a Master/Slave
  - LINFlexD_1, LINFlexD_2, LINFlexD_14, LINFlexD_15, and LINFlexD_16 are Masters
- Four modular controller area network (MCAN) modules and one time-triggered controller area network (M-TTCAN)
- External Bus Interface (EBI)
  - Dual routing of accesses to EBI
  - Access path determined by access address
  - Access path downstream of PFLASH controller
    - Allows EBI accesses to share buffer and prefetch capabilities of internal flash
    - Allows internal flash accesses to be remapped to memories connected to EBI

# Table of Contents

    - Access path via dedicated AXBS slave port
        - Avoids contention with other memory accesses
- Two Dual-channel FlexRay controllers
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- Self-test capability

# 1 Introduction

## 1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5777M series of microcontroller units (MCUs). For functional characteristics, see the *MPC5777M Microcontroller Reference Manual*.

## 1.2 Description

This family of MCUs is targeted at automotive powertrain controller and chassis control applications from single cylinder motorcycles at the very bottom end; through 4 to 8 cylinder gasoline and diesel engines; transmission control; steering and breaking applications; to high end hybrid and advanced combustion systems at the top end.

Many of the applications are considered to be functionally safe and the family is designed to achieve ISO26262 ASIL-D compliance.

## 1.3 Device feature

**Table 1. MPC5777M feature**

| Feature | | MPC5777M |
|---|---|---|
| Process | | 55 nm |
| Main processor | Core | e200z7 |
| | Number of main cores | 2 |
| | Number of checker cores | 1 |
| | Local RAM (per main core) | 16 KB Instruction<br>64 KB Data |
| | Single precision floating point | Yes |
| | LSP | No |
| | VLE | Yes |
| | Cache | 16 KB Instruction<br>4 KB Data |
| I/O processor | Core | e200z4 |
| | Local RAM | 16 KB instruction<br>64 KB Data |
| | Single precision floating point | Yes |
| | LSP | Yes |
| | VLE | Yes |
| | Cache | 8 KB instruction |
| Main processor frequency | | 300 MHz[1] |
| I/O processor frequency | | 200 MHz |
| MMU entries | | 0 |
| MPU | | Yes |
| Semaphores | | Yes |

**Table 1. MPC5777M feature (continued)**

| Feature | MPC5777M |
|---|---|
| CRC channels | 2 |
| Software watchdog timer (Task SWT/Safety SWT) | 4 (3/1) |
| Core Nexus class | 3+ |
| Sequence processing unit (SPU) | Yes |
| Debug and calibration interface (DCI) / run control module | Yes |
| System SRAM | 404 KB |
| Flash memory | 8640 KB |
| Flash memory fetch accelerator | 4 × 256 bit |
| Data flash memory (EEPROM) | 8 × 64 KB<br>+ 2 × 16 KB |
| Flash memory overlay RAM | 16 KB |
| External bus | 32 bit |
| Calibration interface | 64-bit IPS Slave |
| DMA channels | 2 × 64 |
| DMA Nexus Class | 3+ |
| LINFlex (UART/MSC) | 6 (3/3) |
| MCAN/TTCAN | 4/1 |
| DSPI (SPI/MSC/sync SCI) | 8 (4/3/1) |
| Microsecond bus downlink | Yes |
| SENT bus | 15 |
| $I^2C$ | 2 |
| PSI5 bus | 5 |
| PSI5-S UART-to-PSI5 interface | Yes |
| FlexRay | 2 × dual channel |
| Ethernet | MII / RMII |
| Zipwire® (SIPI / LFAST$^2$) Interprocessor Communication Interface | High speed |
| System timers | 8 PIT channels<br>3 AUTOSAR® (STM)<br>64-bit PIT |
| BOSCH® GTM Timer[3] | Yes |
| GTM RAM | 58 KB |
| Interrupt controller | 727 sources |
| ADC (SAR) | 12 |

**Table 1. MPC5777M feature (continued)**

| Feature | MPC5777M |
|---|---|
| ADC (SD) | 10 |
| Temperature sensor | Yes |
| Self test controller | Yes |
| PLL | Dual PLL with FM |
| Integrated linear voltage regulator | None |
| External power supplies | 5 V<br>3.3 V[7]<br>1.2 V |
| Low-power modes | Stop mode<br>Slow mode |
| Packages | • 416 TEPBGA[4]<br>• 512 TEPBGA[5] |

1 Includes four user-programmable CPU cores and one safety core. The main computational shell consists of dual e200z7 CPUs operating at 300 MHz with a third identical core running as a safety checker core in delayed lockstep mode with one of the dual e200z7 cores. The I/O subsystem includes a CPU targeted at managing the peripherals. This is an e200z4 CPU running at 200 MHz. The fifth CPU is an e200z0 running at 100 MHz and is embedded in the Hardware Security Module. All CPUs are compatible with the Power Architecture.

2 LVDS Fast Asynchronous Serial Transmission

3 BOSCH® is a registered trademark of Robert Bosch GmbH.

4 416 TEPBGA package supports development and production applications with the same package footprint.

5 512 TEPBGA package supports development and production applications with the same package footprint.

## 1.4 Block diagram

The figures below show the top-level block diagrams.

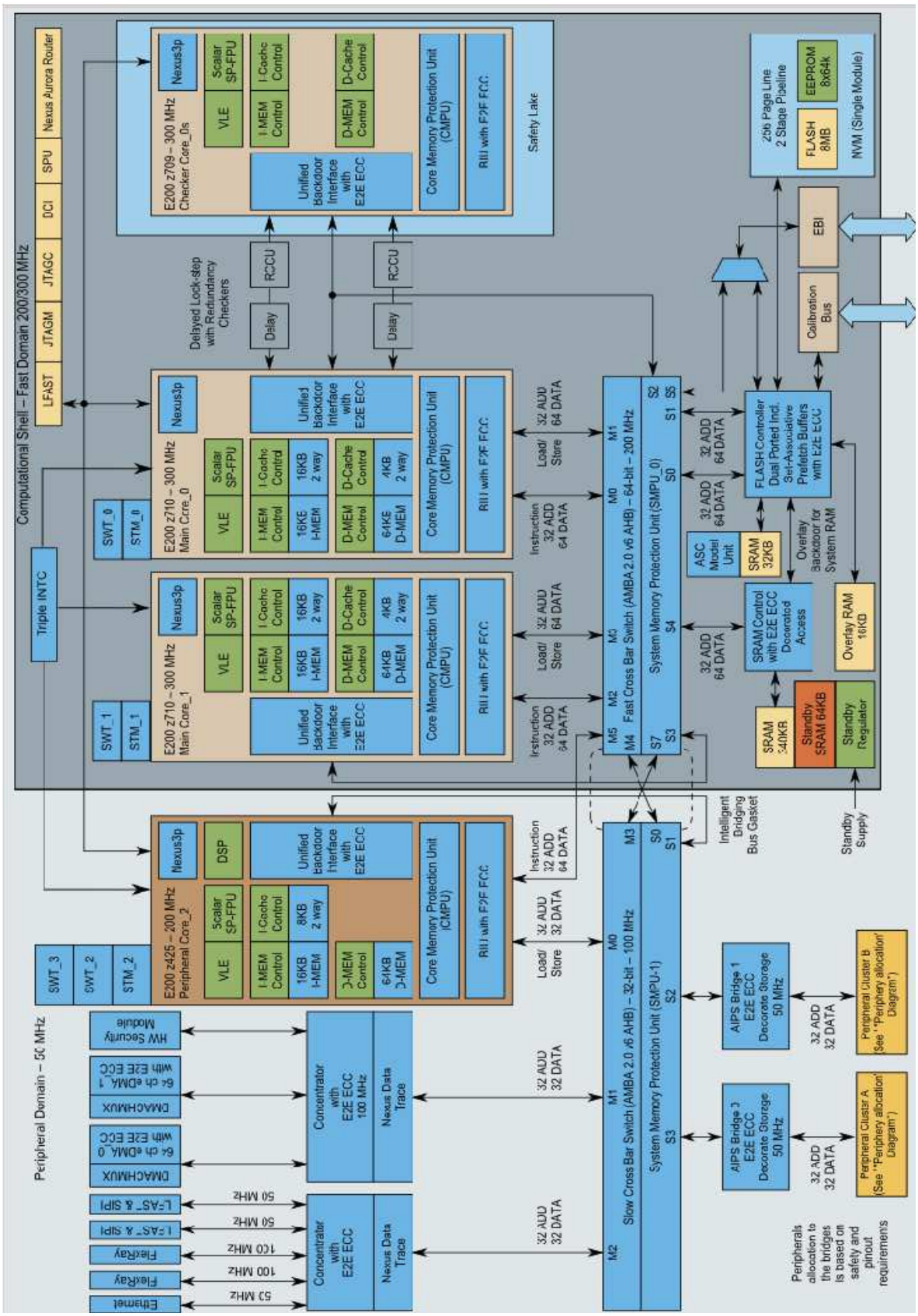


**Figure 1. Block diagram**

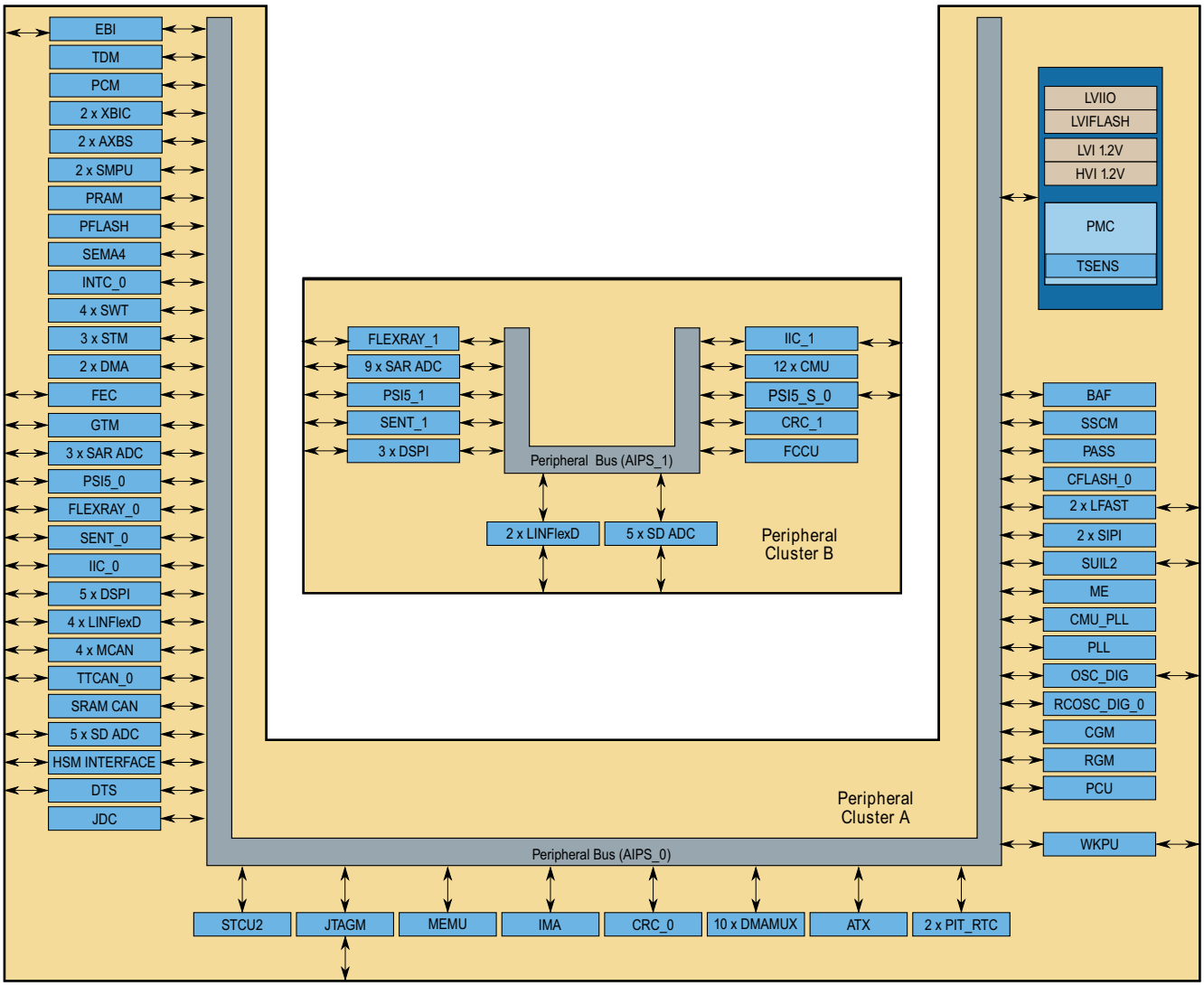


**Figure 2. Periphery allocation**

# 2 Package pinouts and signal descriptions

See the *MPC5777M Microcontroller Reference Manual* for signal information.

## 2.1 Package pinouts

The BGA ballmap package pinouts for the 416 and 512 production and emulation devices are shown in the following figures.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | PX[0] | PN[0] | PH[12] | PC[15] | PF[3] | PF[5] | PH[14] | PH[15] | PK[15] | PM[8] | PX[2] | PQ[14] | PH[9] | PQ[4] | PQ[10] | PQ[9] | VDD_HV_FLA | PQ[3] | PH[0] | PA[0] | PA[4] | ESR0 | PF[14] | VDD_HV_IO_MAIN | VSS_HV | A |
| B | PD[15] | PD[14] | PM[15] | PH[13] | PC[13] | PM[11] | PM[10] | PF[4] | PM[3] | PK[14] | PM[7] | PQ[15] | PX[1] | PQ[7] | PQ[6] | PQ[11] | PQ[8] | VDD_HV_FLA | PQ[5] | PM[9] | PA[12] | PORST | TESTMODE | VDD_HV_IO_MAIN | VSS_HV | VDD_LV | B |
| C | PC[7] | PL[2] | PM[14] | PM[12] | PC[10] | PC[14] | PM[2] | PM[0] | PM[1] | PM[6] | PM[4] | PQ[13] | PH[4] | PE[10] | PH[7] | PD[0] | PD[3] | PD[2] | PH[8] | PH[3] | PA[10] | PA[1] | VDD_HV_IO_MAIN | VSS_HV | VDD_LV | PA[14] | C |
| D | PN[2] | PN[4] | PN[1] | PC[6] | PC[12] | PC[11] | VDD_HV_IO_FLEX | VSS_HV | VDD_LV | PE[12] | PM[5] | PH[10] | PE[11] | VDD_HV_PMC | VSS_HV | PH[1] | PD[1] | PA[13] | PG[15] | PH[2] | PA[11] | VDD_HV_IO_MAIN | VSS_HV | VDD_LV | PA[9] | PD[6] | D |
| E | PN[3] | PC[9] | PL[7] | PL[1] | | | | | | | | | | | | | | | | | | | VDD_LV | PA[6] | PA[8] | VDD_HV_IO_JTAG | E |
| F | PN[5] | PC[8] | PL[6] | PL[0] | | | | | | | | | | | | | | | | | | | PA[5] | PA[7] | VSS_HV_OSC | NC | F |
| G | PN[7] | PF[2] | PL[3] | PL[5] | | | | | | | | | | | | | | | | | | | PD[7] | PI[15] | XTAL | EXTAL | G |
| H | PC[4] | PC[5] | PL[4] | VDD_LV | | | | | | | | | | | | | | | | | | | PF[13] | NC | NC | NC | H |
| J | PN[9] | PN[6] | PC[3] | VSS_HV | | | | | | | | | | | | | | | | | | | PI[14] | PF[10] | PF[11] | PF[12] | J |
| K | PN[11] | PN[10] | PN[8] | VDD_HV_IO_MAIN | | | | | | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | | | | | | PF[9] | PH[5] | PH[6] | PJ[9] | K |
| L | PN[15] | PN[14] | PN[13] | PN[12] | | | | | | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | | | | | | VSS_HV | PF[8] | PJ[3] | PJ[4] | L |
| M | PE[0] | PC[0] | PC[1] | PC[2] | | | | | | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | | | | | | VDD_HV_IO_EBI | PW[14] | PW[15] | PJ[2] | M |
| N | PG[0] | PE[4] | PE[2] | PE[1] | | | | | | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | | | | | | PW[10] | PW[11] | PW[12] | PW[13] | N |
| P | PI[9] | PI[8] | PQ[1] | PQ[2] | | | | | | NC | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | NC | | | | | | VDD_LV | PW[7] | PW[8] | PW[9] | P |
| R | NC | PQ[0] | PD[12] | NC | | | | | | NC | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | NC | | | | | | VSS_HV | PW[4] | PW[5] | PW[6] | R |
| T | PK[1] | PE[3] | PD[13] | VSS_HV | | | | | | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | VSS_LV | | | | | | VDD_HV_IO_EBI | PW[1] | PW[2] | PW[3] | T |
| U | PK[0] | PR[14] | PK[2] | PK[3] | | | | | | NC | NC | NC | NC | NC | NC | NC | NC | | | | | | PW[0] | PV[13] | PV[14] | PV[15] | U |
| V | PR[15] | PR[12] | PB[13] | PB[12] | | | | | | | | | | | | | | | | | | | VDD_LV | PV[10] | PV[11] | PV[12] | V |
| W | PR[13] | PR[10] | PI[1] | VDD_HV_ADR_D | | | | | | | | | | | | | | | | | | | VSS_HV | PV[7] | PV[8] | PV[9] | W |
| Y | PR[11] | PR[8] | PI[0] | VSS_HV_ADR_D | | | | | | | | | | | | | | | | | | | VDD_HV_IO_EBI | PV[3] | PV[4] | PV[5] | Y |
| AA | PR[9] | PI[5] | PE[13] | PR[6] | | | | | | | | | | | | | | | | | | | PV[2] | PV[1] | PY[4] | PV[0] | AA |
| AB | PI[3] | PI[4] | PR[7] | PE[14] | | | | | | | | | | | | | | | | | | | VDD_LV | PT[2] | PT[7] | PT[12] | AB |
| AC | PI[2] | PD[11] | PG[8] | PE[15] | PB[0] | VSS_HV_ADR_D2 | PG[6] | PB[6] | PL[9] | PL[10] | PI[13] | PF[1] | PL[14] | PA[15] | PD[10] | VDD_HV_IO_MAIN | PF[7] | VDD_HV_IO_FLEXE | VSS_HV | VDD_LV | NC | VDD_HV_IO_FLEXE | VSS_HV | PT[3] | PT[8] | PT[13] | AC |
| AD | PB[4] | PR[0] | PG[7] | PK[10] | PB[1] | VDD_HV_ADR_D2 | PG[5] | PB[7] | VDDSTBY | PL[12] | PI[12] | PF[0] | PL[15] | PJ[6] | PB[11] | VDD_HV_IO_MAIN | PF[6] | PS[0] | PS[3] | PS[6] | PS[9] | PS[12] | PS[14] | PT[4] | PT[9] | PT[14] | AD |
| AE | PR[1] | PI[7] | PG[12] | PB[2] | VDD_HV_ADV_D | PR[2] | PR[4] | VSS_HV_ADR_S | VDD_HV_ADV_S | PL[13] | PI[11] | PD[9] | PJ[0] | PB[9] | PD[8] | VDD_HV_IO_MAIN | PJ[7] | PS[1] | PS[4] | PS[7] | PS[10] | PS[13] | PS[15] | PT[5] | PT[10] | PT[15] | AE |
| AF | NC | PI[6] | PG[11] | PB[3] | VSS_HV_ADV_D | PR[3] | PR[5] | VDD_HV_ADR_S | VSS_HV_ADV_S | PL[11] | PI[10] | PB[10] | PJ[1] | PB[8] | PA[3] | VDD_HV_IO_MAIN | PJ[5] | PS[2] | PS[5] | PS[8] | PS[11] | PT[0] | PT[1] | PT[6] | PT[11] | NC | AF |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |

**Figure 3. 416-ball BGA production device pinout (top view)**

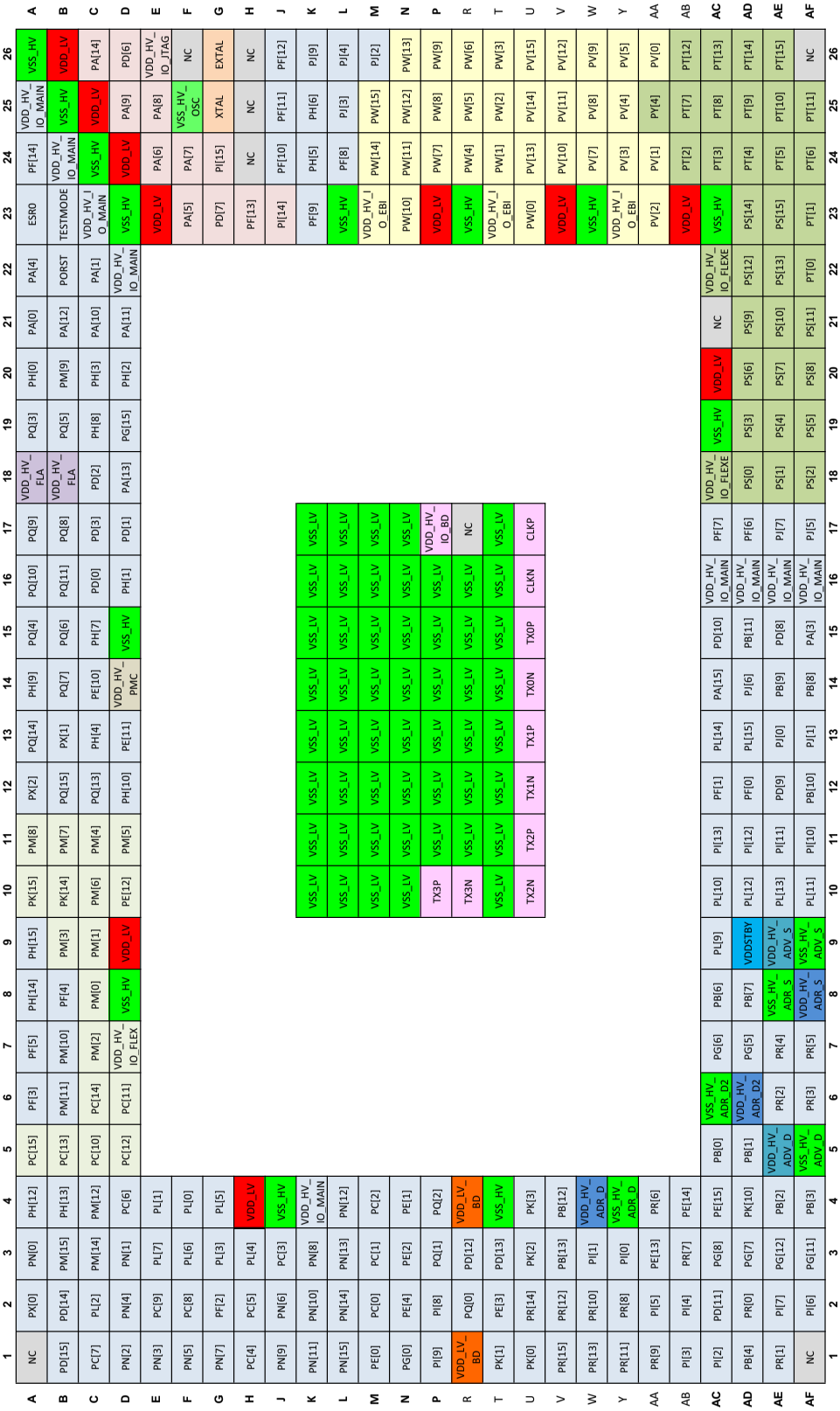

**Figure 4. 416-ball BGA emulation device pinout (top view)**


**Figure 5. 512-ball BGA production device pinout (top view)**

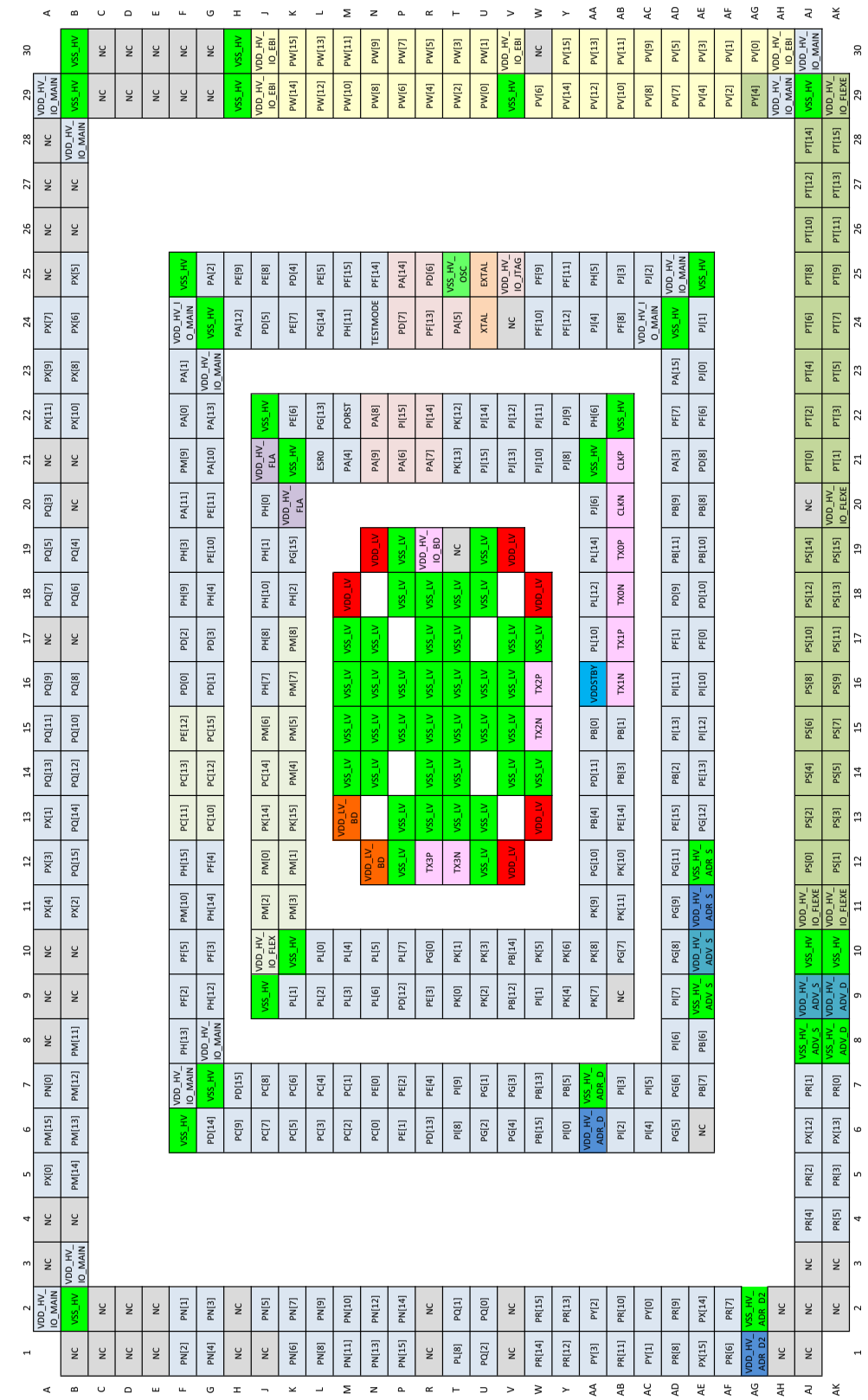

**Figure 6. 512-ball BGA emulation device pinout (top view)**

## 2.2 Pin/ball descriptions

The following sections provide signal descriptions and related information about device functionality and configuration.

### 2.2.1 Power supply and reference voltage pins/balls

Table 2 contains information on power supply and reference pin functions for the devices.

**NOTE**

All ground supplies must be tied to ground. They can NOT float.

**Table 2. Power supply and reference pins**

| Supply | | | BGA ball | | | |
|---|---|---|---|---|---|---|
| Symbol | Type | Description | 416PD | 416ED | 512PD | 512ED |
| $V_{SS\_HV}$ | Ground | High voltage ground | A26, B25, C24, D23, D15, D8, J4, L23, R23, T4, W23, AC23, AC19 | | B2, B29, B30, F6, F25, G7, G24, H29, H30, J9, J22, K10, K21,V29, AA21, AB22, AD24, AE25, AJ10, AJ29, AK10 | |
| $V_{SS\_LV}$ | Ground | Low voltage ground | K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15,N 16, N17, P11, P12, P13, P14, P15, P16, R 11, R12, R13, R14, R15, R16, T10, T11, T12, T13, T14, T15, T16, T17 | | M14, M15, M16, M17, N14, N15, N16, N17, P12, P13, P15, P16, P18, P19, R13, R14, R15, R16, R17, R18, T13,T14, T15, T16, T17, T18, U12, U13, U 15, U16, U18, U19, V14, V15 V16, V17, W14, W17 | |
| $V_{DD\_LV}$ | Power | Low voltage power supply for production device (PLL is also powered by this pin.) | B26, C25, D9, D24, E23, H4, P23, V23, AB23, AC20 | | M18, N19, V12, V19, W13, W18 | |
| $V_{DD\_LV\_BD}$ | Power | Low voltage power supply for buddy die | — | R1, R4 | — | M13, N12 |
| $V_{DD\_HV\_PMC}$ | Power | High voltage power supply for internal power management unit | D14 | | — | |
| $V_{DD\_HV\_IO\_MAIN}$ | Power | High voltage power supply for I/O | A25, B24, C23, D22, K4, AC16, AD16, AE16, AF16 | | A2, A29, B3, B28, F7, F24, G8, G23, AC24, AD25, AH29, AJ30 | |
| $V_{DD\_HV\_IO\_BD}$ | Power | High voltage power supply for buddy die I/O | — | P17 | — | R19 |
| $V_{SS\_HV\_OSC}$ | Ground | Oscillator ground supply | F25 | | T25 | |
| $V_{DD\_HV\_JTAG}$ | Power | JTAG/Oscillator power supply | E26 | | V25 | |

**Table 2. Power supply and reference pins (continued)**

| Supply | | | BGA ball | | | |
|---|---|---|---|---|---|---|
| Symbol | Type | Description | 416PD | 416ED | 512PD | 512ED |
| $V_{DD\_HV\_IO\_FLEX}$ | Power | FlexRay/Ethernet 3.3 V I/O supply | D7 | | J10 | |
| $V_{DD\_HV\_IO\_FLEXE}$ | Power | FLexRay/Ethernet/EBI I/O Segment Voltage Supply | AC18, AC22 | | AJ11, AK11, AK20, AK29 | |
| $V_{DD\_HV\_IO\_EBI}$ | Power | EBI Address/Control I/O Segment Voltage Supply | M23,T23,Y23 | | J29, J30, V30, AH30 | |
| $V_{DD\_HV\_FLA}$ | Power | Decoupling supply pin for flash | A18, B18 | | J21, K20 | |
| $V_{SS\_HV\_ADV\_S}$ | Ground | Ground supply for ADC SAR | AF9 | | AE9, AJ8 | |
| $V_{DD\_HV\_ADV\_S}$ | Power | Voltage supply for ADC SAR | AE9 | | AE10, AJ9 | |
| $V_{SS\_HV\_ADV\_D}$ | Ground | Ground supply for ADC SD | AF5 | | AK8 | |
| $V_{DD\_HV\_ADV\_D}$ | Power | Voltage supply for ADC SD | AE5 | | AK9 | |
| $V_{SS\_HV\_ADR\_S}$ | Reference | Ground reference for ADC SAR | AE8 | | AE12 | |
| $V_{DD\_HV\_ADR\_S}$ | Reference | Voltage reference for ADC SAR | AF8 | | AE11 | |
| $V_{SS\_HV\_ADR\_D}$ | Reference | Ground reference for ADC SD | Y4, AC6 | | AA7 | |
| $V_{DD\_HV\_ADR\_D}$ | Reference | Voltage reference for ADC SD | W4, AD6 | | AA6 | |
| $V_{DDSTBY}$ | Power | Standby RAM supply | AD9 | | AA16 | |

## 2.2.2 System pins/balls

Table 3 contains information on system pin functions for the devices.

**Table 3. System pins**

| Symbol | Description | Direction | BGA ball | | | |
|---|---|---|---|---|---|---|
| | | | 416PD | 416ED | 512PD | 512ED |
| PORST | Power on reset with Schmitt trigger characteristics and noise filter. PORST is active low | Bidirectional | B22 | | M22 | |
| ESR0 | External functional reset with Schmitt trigger characteristics and noise filter. ESR0 is active low | Bidirectional | A23 | | L21 | |
| TESTMODE | Pin for testing purpose only. TESTMODE pull-down is implemented to prevent the device from entering TESTMODE. It is recommended to connect the TESTMODE pin to VSS_HV_IO on the board. The value of the TESTMODE pin is latched at the negation of reset and has no affect afterward.<br>**Note:** The device will not exit reset with the TESTMODE pin asserted during power-up. | Input only | B23 | | N24 | |

**Table 3. System pins (continued)**

| Symbol | Description | Direction | BGA ball | | | |
|---|---|---|---|---|---|---|
| | | | 416PD | 416ED | 512PD | 512ED |
| XTAL | Analog output of the oscillator amplifier circuit<br>needs to be grounded if oscillator is used in bypass mode. | Output | G25 | | U24 | |
| EXTAL | Analog input of the oscillator amplifier circuit when oscillator is not in bypass mode<br>Analog input for the clock generator when oscillator is in bypass mode | Input | G26 | | U25 | |

## 2.2.3 LVDS pins/balls

The following table contains information on LVDS pin functions for the devices.

**Table 4. LVDS pin descriptions**

| Functional block | Port pin | Signal | Signal description | Direction | BGA ball (416 PD, 416 ED) | BGA ball (512 PD, 512 ED) |
|---|---|---|---|---|---|---|
| SIPI / LFAST[1] | PA[14] | SIPI_TXP | Interprocessor Bus LFAST, LVDS Transmit Positive Terminal | O | C26 | P25 |
| | PD[6] | SIPI_TXN | Interprocessor Bus LFAST, LVDS Transmit Negative Terminal | O | D26 | R25 |
| | PD[7] | SIPI_RXP | Interprocessor Bus LFAST, LVDS Receive Positive Terminal | I | G23 | P24 |
| | PF[13] | SIPI_RXN | Interprocessor Bus LFAST, LVDS Receive Negative Terminal | I | H23 | R24 |
| High-Speed Debug (HSD) / LFAST[1,2] | PA[7] | DEBUG_TXP | Debug LFAST, LVDS Transmit Positive Terminal | O | F24 | R21 |
| | PA[8] | DEBUG_TXN | Debug LFAST, LVDS Transmit Negative Terminal | O | E25 | N22 |
| | PA[9] | DEBUG_RXP | Debug LFAST, LVDS Receive Positive Terminal | I | D25 | N21 |
| | PA[5] | DEBUG_RXN | Debug LFAST, LVDS Receive Negative Terminal | I | F23 | T24 |

**Table 4. LVDS pin descriptions (continued)**

| Functional block | Port pin | Signal | Signal description | Direction | BGA ball (416 PD, 416 ED) | BGA ball (512 PD, 512 ED) |
|---|---|---|---|---|---|---|
| DSPI 4 Microsecond Bus | PD[2] | SCK_P | DSPI 4 Microsecond Bus Serial Clock, LVDS Positive Terminal | O | C18 | F17 |
| | PD[3] | SCK_N | DSPI 4 Microsecond Bus Serial Clock, LVDS Negative Terminal | O | C17 | G17 |
| | PD[0] | SOUT_P | DSPI 4 Microsecond Bus Serial Data, LVDS Positive Terminal | O | C16 | F16 |
| | PD[1] | SOUT_N | DSPI 4 Microsecond Bus Serial Data, LVDS Negative Terminal | O | D17 | G16 |
| DSPI 5 Microsecond Bus | PF[10] | SCK_P | DSPI 5 Microsecond Bus Serial Clock, LVDS Positive Terminal | O | J24 | W24 |
| | PF[9] | SCK_N | DSPI 5 Microsecond Bus Serial Clock, LVDS Negative Terminal | O | K23 | W25 |
| | PF[12] | SOUT_P | DSPI 5 Microsecond Bus Serial Data, LVDS Positive Terminal | O | J26 | Y24 |
| | PF[11] | SOUT_N | DSPI 5 Microsecond Bus Serial Data, LVDS Negative Terminal | O | J25 | Y25 |
| DSPI 6 Microsecond Bus | PQ[9] | SCK_P | DSPI 6Microsecond Bus Serial Clock, LVDS Positive Terminal | O | A17 | A16 |
| | PQ[8] | SCK_N | DSPI 6 Microsecond Bus Serial Clock, LVDS Negative Terminal | O | B17 | B16 |
| | PQ[11] | SOUT_P | DSPI 6 Microsecond Bus Serial Data, LVDS Positive Terminal | O | B16 | A15 |
| | PQ[10] | SOUT_N | DSPI 6 Microsecond Bus Serial Data, LVDS Negative Terminal | O | A16 | B15 |

**Table 4. LVDS pin descriptions (continued)**

| Functional block | Port pin | Signal | Signal description | Direction | BGA ball (416 PD, 416 ED) | BGA ball (512 PD, 512 ED) |
|---|---|---|---|---|---|---|
| Differential DSPI 2 | PD[2] | SCK_P | Differential DSPI 2 Clock, LVDS Positive Terminal | O | C18 | F17 |
| | PD[3] | SCK_N | Differential DSPI 2 Clock, LVDS Negative Terminal | O | C17 | G17 |
| | PD[0] | SOUT_P | Differential DSPI 2 Serial Output, LVDS Positive Terminal | O | C16 | F16 |
| | PD[1] | SOUT_N | Differential DSPI 2 Serial Output, LVDS Negative Terminal | O | D17 | G16 |
| | PD[7] | SIN_P | Differential DSPI 2 Serial Input, LVDS Positive Terminal | I | G23 | P24 |
| | PF[13] | SIN_N | Differential DSPI 2 Serial Input, LVDS Negative Terminal | I | H23 | R24 |
| Differential DSPI 5 | PF[10] | SCK_P | Differential DSPI 5 Clock, LVDS Positive Terminal | O | J24 | W24 |
| | PF[9] | SCK_N | Differential DSPI 5 Clock, LVDS Negative Terminal | O | K23 | W25 |
| | PF[12] | SOUT_P | Differential DSPI 5 Serial Output, LVDS Positive Terminal | O | J26 | Y24 |
| | PF[11] | SOUT_N | Differential DSPI 5 Serial Output, LVDS Negative Terminal | O | J25 | Y25 |
| | PD[7] | SIN_P | Differential DSPI 5 Serial Input, LVDS Positive Terminal | I | G23 | P24 |
| | PF[13] | SIN_N | Differential DSPI 5 Serial Input, LVDS Negative Terminal | I | H23 | R24 |
| | PI[15] | SIN_P | Differential DSPI 5 Serial Input, LVDS Positive Terminal | I | G24 | P22 |
| | PI[14] | SIN_N | Differential DSPI 5 Serial Input, LVDS Negative Terminal | I | J23 | R22 |

[1] DRCLK and TCK/DRCLK usage for SIPI LFAST and Debug LFAST are described in the *MPC5777M Microcontroller Reference Manual* SIPI LFAST and Debug LFAST chapters.

[2] Pads use special enable signal form DCI block: DCI driven enable for Debug LFAST pads is transparent to user.

**Table 5. Aurora pin descriptions**

| Functional Block | PAD | Signal | Signal Description | Direction | BGA | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | 416PD | 416ED | 512PD | 512ED |
| Nexus Aurora High Speed Trace | — | TX0P | Nexus Aurora High Speed Trace Lane 0, LVDS Positive Terminal | O | — | U15 | — | AB19 |
| | — | TX0N | Nexus Aurora High Speed Trace Lane 0, LVDS Negative Terminal | O | — | U14 | — | AB18 |
| | — | TX1P | Nexus Aurora High Speed Trace Lane 1, LVDS Positive Terminal | O | — | U13 | — | AB17 |
| | — | TX1N | Nexus Aurora High Speed Trace Lane 1, LVDS Negative Terminal | O | — | U12 | — | AB16 |
| | — | TX2P | Nexus Aurora High Speed Trace Lane 2, LVDS Positive Terminal | O | — | U11 | — | W16 |
| | — | TX2N | Nexus Aurora High Speed Trace Lane 2, LVDS Negative Terminal | O | — | U10 | — | W15 |
| | — | TX3P | Nexus Aurora High Speed Trace Lane 3, LVDS Positive Terminal | O | — | P10 | — | R12 |
| | — | TX3N | Nexus Aurora High Speed Trace Lane 3, LVDS Negative Terminal | O | — | R10 | — | T12 |
| | — | CLKP (BD-AGB TCLKP) | Nexus Aurora High Speed Trace Clock, LVDS Positive Terminal | I | — | U17 | — | AB21 |
| | — | CLKN (BD-AGB TCLKN) | Nexus Aurora High Speed Trace Clock, LVDS Negative Terminal | I | — | U16 | — | AB20 |

# 3 Electrical characteristics

## 3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

**NOTE**

Within this document, $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_FLEXE}$, $V_{DD\_HV\_IO\_EBI}$, and $V_{DD\_HV\_FLA}$. $V_{DD\_HV\_ADV}$ refers to ADC supply pins $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADR}$ refers to ADC reference pins $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$. $V_{SS\_HV\_ADV}$ refers to ADC ground pins $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$. $V_{SS\_HV\_ADR}$ refers to ADC reference pins $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$.

## 3.2 Absolute maximum ratings

Table 6 describes the maximum ratings of the device.

**Table 6. Absolute maximum ratings[1]**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Cycle | SR | Lifetime power cycles | — | — | 1000 k | — |
| $V_{DD\_LV}$ | SR | 1.2 V core supply voltage[2,3,4] | — | –0.3 | 1.5 | V |
| $V_{DD\_LV\_BD}$ | SR | Emulation module voltage[2,3,4] | — | –0.3 | 1.5 | V |
| $V_{DD\_HV\_IO}$ | SR | I/O supply voltage[5,6] | — | –0.3 | 6.0 | V |
| $V_{DD\_HV\_PMC}$ | SR | Power Management Controller supply voltage[5] | — | –0.3 | 6.0 | V |
| $V_{DD\_HV\_FLA}$ | SR | Flash core voltage[7] | — | –0.3 | 4.5 | V |
| $V_{DDSTBY}$ | SR | RAM standby supply voltage[5] | — | –0.3 | 6.0 | V |
| $V_{SS\_HV\_ADV}$[8] | SR | SAR and S/D ADC ground voltage | Reference to $V_{SS\_HV}$ | –0.3 | 0.3 | V |
| $V_{DD\_HV\_ADV}$[9] | SR | SAR and S/D ADC supply voltage | Reference to corresponding $V_{SS\_HV\_ADV}$ | –0.3 | 6.0 | V |
| $V_{SS\_HV\_ADR}$[10] | SR | SAR and S/D ADC low reference | Reference to $V_{SS\_HV}$ | –0.3 | 0.3 | V |
| $V_{DD\_HV\_ADR}$[11] | SR | SAR and S/D ADC high reference | Reference to corresponding $V_{SS\_HV\_ADR}$ | –0.3 | 6.0 | V |
| $V_{DD\_HV\_IO\_JTAG}$ | SR | Crystal oscillator, FEC MDIO/MDC, LFAST, JTAG[5] | Reference to $V_{SS\_HV}$ | –0.3 | 6.0 | V |

**Table 6. Absolute maximum ratings[1] (continued)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{DD\_HV\_IO\_EBI}$ | SR | External Bus Interface supply voltage | — | –0.3 | 6.0 | V |
| $V_{DD\_LV\_BD} – V_{DD\_LV}$ | SR | Emulation module supply differential to 1.2 V core supply | — | –0.3 | 1.5 | V |
| $V_{IN}$ | SR | I/O input voltage range[12] | — | –0.3 | 6.0 | V |
| | | | Relative to $V_{SS\_HV\_IO}$[13,14] | –0.3 | — | |
| | | | Relative to $V_{DD\_HV\_IO}$[13,14] | — | 0.3 | |
| $I_{INJD}$ | SR | Maximum DC injection current for digital pad | Per pin, applies to all digital pins | –5 | 5 | mA |
| $I_{INJA}$ | SR | Maximum DC injection current for analog pad | Per pin, applies to all analog pins | –5 | 5 | mA |
| $I_{MAXD}$ | SR | Maximum output DC current when driven | Medium | –7 | 8 | mA |
| | | | Strong | –10 | 10 | |
| | | | Very strong | –11 | 11 | |
| $I_{MAXSEG}$ | SR | Maximum current per power segment[15] | — | –90 | 90 | mA |
| $T_{STG}$ | SR | Storage temperature range and non-operating times | — | –55 | 175 | °C |
| STORAGE | SR | Maximum storage time, assembled part programmed in ECU | No supply; storage temperature in range –40 °C to 60 °C | — | 20 | years |
| $T_{SDR}$ | SR | Maximum solder temperature[16] Pb-free package | — | — | 260 | °C |
| MSL | SR | Moisture sensitivity level[17] | — | — | 3 | — |
| $t_{XRAY}$ | SR | X-ray screen time[18] | At 160 KeV at max 5 mm | — | 3 | min |

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum $T_J$ = 150 °C, remaining time as defined in note 3 and note 4

3 Allowed 1.38– 1.45 V– for 10 hours cumulative time at maximum $T_J$ = 150 °C, remaining time as defined in note 4

4 1.32 – 1.38 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.326 V at maximum $T_J$ = 150 °C.

5 Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, $T_J$ = 150 °C, remaining time at or below 5.5 V.

6 $V_{DD\_HV\_IO}$ applies to $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_FLEXE}$, $V_{DD\_HV\_IO\_JTAG}$, and $V_{DD\_HV\_IO\_EBI}$ I/O power supplies.

7 Allowed 3.6–4.5 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, $T_J$ = 150 °C, remaining time at or below 3.6 V.

8 Includes ADC grounds $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$.

[9] Includes ADC supplies $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADV\_S}$ is also the supply for the device temperature sensor, RCOSC, and bandgap reference.

[10] Includes ADC low references $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$.

[11] Includes ADC high references $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$.

[12] The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies significantly across process and temperature, but a value of 0.3V can be used for nominal calculations.

[13] $V_{DD\_HV\_IO}/V_{SS\_HV\_IO}$ refers to supply pins and corresponding grounds: $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_OSC}$, $V_{DD\_HV\_FLA}$.

[14] Relative value can be exceeded if design measures are taken to ensure injection current limitation (parameters $I_{INJD}$ and $I_{INJA}$).

[15] Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.

[16] Solder profile per IPC/JEDEC J-STD-020D

[17] Moisture sensitivity per JEDEC test method A112

[18] Three Screen done, 1 minute each. No change in device parameters during characterization of at least 10 devices at 30 minutes exposure of 150 KeV at maximum 5 mm.

## 3.3 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

**Table 7. ESD ratings[1,2]**

| Parameter | Conditions | Value | Unit |
|---|---|---|---|
| ESD for Human Body Model (HBM)[3] | All pins | 2000 | V |
| ESD for field induced Charged Device Model (CDM)[4] | All pins | 500 | V |

[1] All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”

[3] This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing

[4] This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level

## 3.4 Operating conditions

The following table describes the operating conditions for the device for which all specifications in the data sheet are valid, except where explicitly noted.

The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

**Table 8. Device operating conditions[1]**

| Symbol | | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **Frequency** | | | | | | | |
| $f_{SYS}$ | SR | Device operating frequency[2] | $T_J$ = –40 °C to 150 °C | — | — | 300 | MHz |

**Table 8. Device operating conditions[1] (continued)**

| Symbol | | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **Temperature** | | | | | | | |
| $T_J$ | SR | Operating temperature range - junction | — | –40.0 | — | 150.0 | °C |
| $T_A$ ($T_L$ to $T_H$) | SR | Ambient operating temperature range | — | –40.0 | — | 125.0 | °C |
| **Voltage** | | | | | | | |
| $V_{DD\_LV}$ | SR | External core supply voltage[3,4] | LVD/HVD enabled | 1.24 | — | 1.38[5] | V |
| | | | LVD/HVD disabled[6,7,8,9] | 1.19 | — | 1.38[5] | |
| $V_{DD\_HV\_IO\_MAIN}$[10,11] | SR | I/O supply voltage | LVD400/HVD600 enabled[18] | 4.5 | — | 5.5[12] | V |
| | | | LVD400/HVD600 disabled [6,13,14,15,18] | 4.2 | — | 5.5 | |
| | | | LVD360/HVD600 disabled [6,13,14,16,17,18] | 3.0 | — | 5.5 | |
| $V_{DD\_HV\_IO\_JTAG}$ | SR | JTAG I/O supply voltage[6,19] | 5 V range | 4.5 | — | 5.5 | V |
| | | | 3.3 V range | 3.0 | — | 3.6 | |
| $V_{DD\_HV\_IO\_FLEX}$ | SR | FlexRay I/O supply voltage | 5 V range | 4.5 | — | 5.5 | V |
| | | | 3.3 V range | 3.0 | — | 3.6 | |
| $V_{DD\_HV\_IO\_FLEXE}$ | SR | FlexRay/EBI I/O supply voltage | 5 V range | 4.5 | — | 5.5 | V |
| | | | 3.3 V range | 3.0 | — | 3.6 | |
| $V_{DD\_HV\_IO\_EBI}$ | SR | External Bus Interface supply voltage | 5 V range | 4.5 | — | 5.5 | V |
| | | | 3.3 V range | 3.0 | — | 3.6 | |
| $V_{DD\_HV\_OSC}$ | SR | Oscillator supply voltage[6,20] | 5 V range | 4.5 | — | 5.5 | V |
| | | | 3.3 V range | 3.0 | — | 3.6 | |
| $V_{DD\_HV\_PMC}$[21] | SR | Power Management Controller (PMC) supply voltage | Full functionality[22,23] | 3.5[24,25] | — | 5.5 | V |
| | | | Reduced internal regulator output capability[26] | 3.15 | — | 3.5 | |
| | | | Supply monitoring activity only (LVD/HVD) | 3.0 | — | 3.15 | |
| $V_{DDSTBY}$ | SR | RAM standby supply voltage[27,28,29] | — | 1.1 | — | 5.5 | V |
| $V_{DD\_HV\_ADV}$ | SR | SARADC, SDADC, Temperature Sensor, and Bandgap Reference supply voltage | LVD400 enabled | 4.5 | — | 5.5 | V |
| | | | LVD400 disabled[30,31,34] | 4.0 | — | 5.5[32] | |
| | | | LVD300 disabled[6,30,31,33,34] | 3.7 | — | 5.5[32] | |

**Table 8. Device operating conditions[1] (continued)**

| Symbol | | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{DD\_HV\_ADR\_D}$ | SR | SD ADC supply reference voltage | Reduced SNR | 3.0 | $V_{DD\_HV\_ADV\_D}$ | 4.5 | V |
| | | | Full SNR | 4.5 | | 5.5[32] | |
| $V_{DD\_HV\_ADR\_D} - V_{DD\_HV\_ADV\_D}$ | SR | SD ADC reference differential voltage | — | — | — | 25 | mV |
| $V_{SS\_HV\_ADR\_D}$ | SR | SD ADC ground reference voltage | — | $V_{SS\_HV\_ADV\_D}$ | | | V |
| $V_{SS\_HV\_ADR\_D} - V_{SS\_HV\_ADV\_D}$ | SR | $V_{SS\_HV\_ADR\_D}$ differential voltage | — | –25 | — | 25 | mV |
| $V_{DD\_HV\_ADR\_S}$[35] | SR | SARADC reference | — | 2.0 | $V_{DD\_HV\_ADV\_S}$ | 4.0 | V |
| | | | | 4.0 | | 5.5[32] | |
| $V_{SS\_HV\_ADR\_S}$ | SR | SAR ADC ground reference voltage | — | $V_{SS\_HV\_ADV\_S}$ | | | V |
| $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S}$ | SR | SARADC reference differential voltage | — | — | — | 25 | mV |
| $V_{SS\_HV\_ADR\_S} - V_{SS\_HV\_ADV\_S}$ | SR | $V_{SS\_HV\_ADR\_S}$ differential voltage | — | –25 | — | 25 | mV |
| $V_{SS\_HV\_ADV} - V_{SS}$ | SR | $V_{SS\_HV\_ADV}$ differential voltage | — | –25 | — | 25 | mV |
| $V_{RAMP\_LV}$ | SR | Slew rate on core power supply pins | — | — | — | 100 | V/ms |
| $V_{RAMP\_HV}$ | SR | Slew rate on HV power supply pins | — | — | — | 100 | V/ms |
| $V_{por\_rel}$ | CC | POR release trip point | -40 °C < Tj < 150 °C | 3.10 | — | 4.26 | V |
| $V_{por\_hys}$ | CC | POR hysteresis | -40 °C < Tj < 150 °C | 150 | — | 300 | mV |
| $V_{IN}$ | SR | I/O input voltage range | — | 0 | — | 5.5 | V |
| **Injection current** | | | | | | | |
| $I_{IC}$ | SR | DC injection current (per pin)[36,37,38] | Digital pins and analog pins | –3.0 | — | 3.0 | mA |
| $I_{MAXSEG}$ | SR | Maximum current per power segment[39] | — | –80 | — | 80 | mA |

1 The ranges in this table are design targets and actual data may vary in the given range.

2 Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the *MPC5777M Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.

3 Core voltage as measured on device pin to guarantee published silicon performance.

4 During power ramp, voltage measured on silicon might be lower. maximum performance is not guaranteed, but correct silicon operation is guaranteed. Refer to the Power Management and Reset Generation Module chapters in the *MPC5777M Microcontroller Reference Manual* for further information.

[5] Although the maximum $V_{DD\_LV}$ operating voltage is 1.38 V, reset is not entered at that voltage. An external voltage monitor is needed or the HVD140_C can be monitored (via an interrupt or by polling the HVD140_C flag bit). Performance above 1.38 V is not guaranteed, and allowed operation above 1.38 V is defined in Absolute maximum ratings.

[6] In the LVD/HVD disabled case, it is necessary for the system to be within a higher voltage range during destructive reset events.

[7] Maximum core voltage is not permitted for entire product life. *See Absolute maximum rating*.

[8] When internal LVD/HVDs are disabled, external monitoring is required to guarantee correct device operation.

[9] Vdd_lv should be above 1.24 V during destructive resets or POR events.

[10] VDD_HV_IO_MAIN range limited to 4.75–5.25 V when FERS = 1 to enable the fast erase time of the flash memory.

[11] During power up operation, the minimum required voltage to come out of reset state is determined by the $V_{PORUP\_HV}$ monitor, which is defined in the voltage monitor electrical characteristics table. Note that the $V_{PORUP\_HV}$ monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

[12] When the LVD/HVDs are enabled, the $V_{DD\_HV\_IO\_MAIN}$ must be less than 5.412 V to exit from a destructive reset.

[13] Maximum voltage is not permitted for entire product life. See *Absolute maximum rating*.

[14] When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.

[15] When these LVD/HVDs are disabled, the $V_{DD\_HV\_IO\_MAIN}$ supply must be between 3.182 V and 5.412 V.

[16] Reduced output capabilities below 4.2 V. See performance derating values in *I/O pad electrical characteristics.*

[17] When the LVD/HVDs are disabled, the VDD_HV_IO_MAIN must be between 3.024 V and 5.412 V.

[18] The PMC supply voltage ($V_{DD\_HV\_PMC}$) must be within the correct range (see the $V_{DD\_HV\_PMC}$ specification).

[19] When the LVD/HVDs are disabled, the HV I/O JTAG supply ($V_{DD\_HV\_IO\_JTAG}$) must be above 3.024 V.

[20] When the LVD/HVDs are disabled, the HV OSC supply ($V_{DD\_HV\_OSC}$) must be above 3.024 V.

[21] Flash read operation is supported for a minimum $V_{DD\_HV\_PMC}$ value of 3.15 V. Flash read, program, and erase operations are supported for a minimum $V_{DD\_HV\_PMC}$ value of 3.5 V.

[22] When the LVD/HVDs are disabled, the $V_{DD\_HV\_PMC}$ must be below 5.412 V during destructive reset events.

[23] A minimum of 4.5 V is required to guarantee correct user logic BIST operation.

[24] During power up operation, the minimum required voltage to come out of reset state is determined by the $V_{PORUP\_HV}$ monitor, which is defined in the voltage monitor electrical characteristics table. Note that the $V_{PORUP\_HV}$ monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

[25] Above Ta = 25°C, the minimum $V_{DD\_HV\_PMC}$ voltage is 3.6 V.

[26] With the reduced internal regulator output capability, erases and writes to the device flash cannot be guaranteed for a single event and multiple erases and writes may be necessary. User logic BIST is not supported with reduced capability.

[27] RAM data retention is guaranteed at a voltage that is always below the maximum brownout flag trip point voltage (see the DC Electrical Specification table). The minimum $V_{DDSTBY}$ voltage at the pin is larger in order to account for on-chip IR drop and noise. There is no effect on RAM operation when $V_{DDSTBY}$ is below 1.1 V, and $V_{DD\_LV}$ is above the minimum operating value.

[28] Non-regulated supplies can be used on the VDDSTBY pin if the absolute maximum and operating condition voltage limits are met. There is no static clamp to a supply rail for the VDDSTBY pin, only dynamic protection for ESD events.

[29] The VDDSTBY pin should be connected to ground in the application when the standby RAM feature is not used.

[30] $V_{DD\_HV\_ADV\_S}$ is required to be between 4.5 V and 5.5 V to read the internal Temperature Sensor and Bandgap Reference.

[31] SAR ADC only. SDADC minimum is 4.5 V.

[32] The ADC is functional up to 5.9V with no reliability issues, but performance is not guaranteed.

[33] When the LVD/HVDs are disabled, the HV ADC supply ($V_{DD\_HV\_ADV}$) must be above 3.182 V.

[34] For supply voltages between 3.0 V and 4.0 V there is no guaranteed precision of ADC (accuracy/linearity). ADCs recover to a fully functional state when the voltage rises above 4.0 V.

[35] $V_{DD\_HV\_ADR\_S}$ must be between 4.5 V and 5.5 V for accurate reading of the device Temperature Sensor.

[36] Full device lifetime without performance degradation

[37] I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the *Absolute maximum ratings* table for maximum input current for reliability requirements.