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NXP Semiconductors

Document Number: MPC5777MRM
Rev. 4.2, 08/2016

MPC5777M Reference Manual

This is the MPC5777M Reference Manual set, consisting of the following files:

- MPC5777M Reference Manual, Rev. 4.2
- MPC5777M Reference Manual, Rev.4. 1
- MPC5777M Reference Manual, Rev. 4

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MPC5777M Reference Manual

MPC5777M Reference Manual, Revision 4.2

Document Number: MPC5777MRM
Rev. 4.2, 08/2016

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RM Addendum Rev 4.2

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Chapter 1
Addenda Overview

1.1 Addenda Overview

The table below displays the updates for MPC5777M RM Rev 4.2 and RM Rev 4.1.

Table 1-1. MPC5777M RM Addenda

Location	Description
MPC5777M RM 4.2 (08/2016)	
Chapter 2, Introduction	
Page 124	• Updated the Block Diagram. See Block Diagram
Chapter 5, Memory Map	
Page 153	• Updated the "Used size" of Flash to 512 KB in the table 'Overview memory map'. See Data Flash Blocks–no overlay
Page 167	• Updated the row "0x00400104" in the table 'UTest flash memory map'. See System RAM memory maps
Chapter 7, Device Configuration	
Page 212	• Added 'IPS Clock Gating Module Enable 1 (IPS_CGM_EN1) Register'. See Clock Gating Module Enable 1 (IPS_CGM_EN1)
Page 222	• Changed the address offset of IPS Clock Gating Module Enable 0. See IPS Clock Gating Module Enable 0 (IPS_CGM_EN0)
Page 224	• Added a note in the section 'INTC implemented registers'. See INTC implemented registers
Page 224	• Removed interrupts in 'Table 7-23 Interrupt sources', which are not supported by the device. See Interrupt sources
Page 268	• Corrected the Reset value of SWT_CR0, SWT_CR1, SWT_CR2, and SWT_CR3 registers in the section 'Default configuration'.

Table continues on the next page...

Table 1-1. MPC5777M RM Addenda (continued)

Location	Description
	See Default configuration
Page 273	• Updated the FEC interface selection section and table FEC interface selection. See FEC interface selection
Page 284	• Changed the Auto configuration for linflex_1 to linflex_16 from 'no' to 'n/a'. See LINFlexD configurations
Page 285	• Updated the MREV and JPIN value in the table 'SSCM_MEMCONFIG Reset Values'. See SSCM_MEMCONFIG reset values
Page 287	• Added a new section 'Reset values on BAF exit'. See Reset values on BAF exit
Page 294	• Updated some entries in table 'LVD /HVD self test decoding' column 'LVD / HVD under test'. See LVD /HVD self test decoding
Page 308	• Updated the table 'Availability and reset values of selected FCCU registers'. See FCCU chip-specific register reset values
Page 310	• Updated the figure 'Error signal flow'. See Error signal flow
Page 311	• Updated the footnotes of 'Table 7-86. FCCU failure inputs'. See FCCU failure inputs
Chapter 12, Calibration and Debug	
Page 443	• Added sections DCI signals and DCI EVTx Pin Multiplexing Control Register (DCI_PINCR). See, DCI signals and DCI $\overline{\text{EVTx}}$ Pin Multiplexing Control Register (DCI_PINCR)
Chapter 14, Core description	
Page 532	• Updated the Reset value of DMEM Control Register 0. See DMEM Control register 0
Page 539	• Updated the Reset value of IMEM Control Register 0. See IMEM Control register 0
Chapter 15, Core description	
Page 615	• Updated the Reset value for DMEM Control Register 0. See DMEM Control register 0
Page 623	• Updated the Reset value of IMEM Control Register 0. See IMEM Control register 0

Table continues on the next page...

Table 1-1. MPC5777M RM Addenda (continued)

Location	Description
Chapter 17, Crossbar Switch	
Page 771	• Updated the reset value of XBAR Control Register. See, XBAR Control register.
Chapter 23, Interrupt Controller (INTC)	
Page 926	• Updated the section 'Examining LIFO contents'. See, Examining LIFO contents.
Chapter 24, Enhanced Direct Memory Access (eDMA)	
Page 930	• Updated the description of Memory map/register definition section. See Memory map/register definition
Chapter 26, Clocking	
Page 1086	• Updated the table 'Maximum system level clock frequencies'. See System clock frequency limitations
Page 1088	• Updated the table 'JTAG frequencies'. See JTAG frequencies
Page 1088	• Added a new section 'System clock ratio restrictions'. See System Clock ratio restrictions
Page 1097	• Updated the Clock distribution figure. See Clock distribution
Page 1102	• Added a note in the M_TTCAN/M_CAN clocking section. See, M_TTCAN/M_CAN clocking
Page 1108	• Added guideline for PCS register configuration in the 'Progressive clock switching' section. See, Progressive clock switching
Chapter 27, Dual PLL Digital Interface (PLLDIG)	
Page 1118 and Page 1123	• Added a reference to the section 'Clock configuration' in register description of PLLDIG PLL0 Divider Register and PLLDIG PLL1 Divider Register.
Page 1129	• Added equation for f_{pll1_VCO} and f_{pll1_phi} when PLLDIG_PLL1FD[FDEN] = 1b. • Updated equations f_{PLL1_PHI} and f_{pll1_VCO}. • See Clock configuration
Chapter 29, Clocking Generation Module	
Page 1204	• Updated Equation 11. See Generic clock change properties
Chapter 31, IRCOSC Digital Interface	
Page 1230	• Updated the Reset value of 'IRCOSC Control Register (IRCOSC_CTL)'.

Table continues on the next page...

Table 1-1. MPC5777M RM Addenda (continued)

Location	Description
	See IRCOSC Control register
Chapter 34, Embedded Flash Memory (c55fmc)	
Page 1303	• Changed the reset value of the Alternate Module Configuration Register, the footnote in the register diagram replaced with footnotes for Over-Program Protection 0 register, and the Footnote in the register diagram replaced with footnote in Over-Program Protection 1 register, Over-Program Protection 2 register, and Over-Program Protection 3 register. See C55FMC Memory map and register definition
Page 1346	• Updated the existing Note in the section 'Program suspend/resume'. See Program suspend/resume
Page 1352	• Paragraph added to section 'Array integrity self check'. See Array integrity self check
Chapter 37, External Bus Interface	
Page 1418 and 1458	• Removed the column 'EBI_MCR [SIZE]' from the tables 'Table 37-3. Write/ Byte Enable Signals Function', ' Table 37-9. Data Bus Requirements for Read Cycles' and 'Table 37-10. Data Bus Contents for Write Cycles'. See, External Bus Interface
Chapter 38, Analog-to-Digital Converters (ADC) Configuration	
Page 1496	• Updated the figure SAR ADC integration diagram. See SAR ADC integration diagram
Page 1500	• SARADC_B sampling time unit changed. See Self Test features
Page 1547, 1550, and 1553	• Updated the field name 'SARADCx_ICWSELR7' in the tables 'Table 38-31 SARADC_8 register definitions, Table 38-32 SARADC_9 register definitions and Table 38-33 SARADC_10 register definitions'. See SARADC register description
Chapter 39 Sigma Delta Analog-to-Digital Converter (SDADC) Digital Interface,	
Page 1572	• Added FRST and FOWEN fields in FIFO Control Register. See FIFO Control register
Chapter 40, Successive Approximation Register Analog-to- Digital Converter (SARADC) Digital Interface	
Page 1651	• Added a Note in the Test Channel Data Register (SARADC_TCDRn) description. See Test Channel Data register
Chapter 48, CAN Subsytem	
Page 1837	• CAN FD support is removed throughout the document. See, CAN Subsystem
Page 1879	• The FOS field width updated to 7 bits for the Rx FIFO 0 Configuration Register .

Table continues on the next page...

Table 1-1. MPC5777M RM Addenda (continued)

Location	Description
	See M_CAN_RXF0C[F0S]
Page 1867	• Added bit field values for the DRXE field in Interrupt Enable Register. See DRXE
Chapter 52, LVDS Fast Asynchronous Serial Transmission (LFAST) – Interprocessor Communications	
Page 2282	• Changed the instances of digrf to LFAST. See, Digrf changed to LFAST
Page 2312	• Fixed typo error, changed the fields name from CTSMN to RCTSMN, CTSMX to RCTSMX, and TISR[CTSMX] to RFCR[CTSMX] in the section CTS mode support. See CTS mode support
Chapter 59, LINFlexD	
Page 3199 and Page 3219	• Updated the field description of IOPE in the LIN Control Register2 and in the LINS field changed the bit field value description of 0001 Init mode in the LIN Status Register. See LINFlexD
Chapter 63 Power Management Controller digital interface	
Page 3407	• Added a sentence in the Reset Event Select Register description. See Reset Event Select register
Chapter 73, JTAG Master	
Page 3956	• For the field TCKSEL updated the TCK divide value. See Module Configuration register
Chapter 76, LVDS Fast Asynchronous Serial Transmission (LFAST) – High Speed debug	
Page 4004	• Changed the instances of digrf to LFAST. See, Digrf changed to LFAST
Page 4066	• Updated the description of the field LVLPEN. See LVLPEN
Chapter 86, Self-Test Control Unit	
Page 4463	• Updated the section 'Register write-access watchdog timer'. See, Register write-access watchdog timer
	• Added a chip specific topic. See STCU2 • Added a chip specific topic for AUTOLOCK_VALUE with info about DCF_COMPLETION. See AUTOLOCK_VALUE for register write access and DCF_COMPLETION value for DCF write completion
Chapter 85, Fault Collection and Control Unit (FCCU)	

Table continues on the next page...

Table 1-1. MPC5777M RM Addenda (continued)

Location	Description
Page 4423 and 4447	• Removed a note from the RFS Configuration Register and NMI Enable Register. See FCCU
MPC5777M RM 4.1 (05/2015)	

Chapter 5, Memory Map, page167	• Table 5-6,In the UTest flash memory map, made the following changes for starting address 0x00400308:
	  • Changed the name in the Description column" to "Reserved".
	  • Changed the existing note.
	  • Added an additional note.
	See, UTest flash memory map

Chapter 2
RM Addendum Rev 4.2

2.1 Overview

The updates for MPC5777M RM Rev 4.2 are described in detail below.

2.1.1 Block Diagram

- The Block Diagram is updated. The 'Concentrator with E2E ECC 50 MHz' changed to 'Concentrator with E2E ECC' and the connection arrows from the FlexRay Ethernet and LFAST & SIPI now have the frequency listed on them.

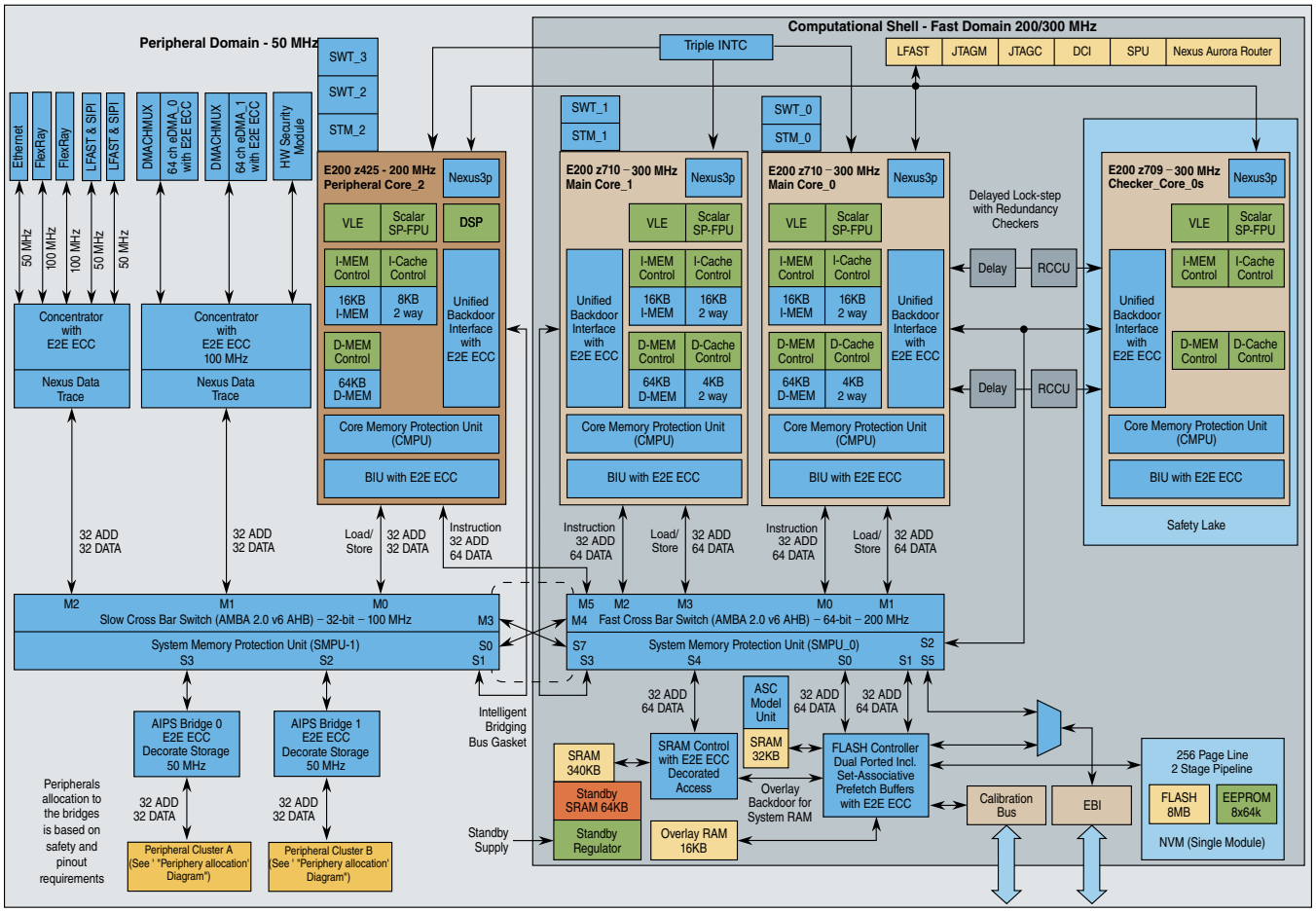


Figure 2-1. Block diagram

2.1.2 Memory Map

2.1.2.1 Data Flash Blocks–no overlay

- In Table 2-1, for the starting address 0x00800000, changed the "Used size" to 512 KB.

Table 2-1. Overview memory map

Start address	End address	Allocated size	Used size	Description
Flash (XBAR port 0—0)				
0x00800000	0x009FFFFF	2 MB	512 KB	Data Flash Blocks–no overlay

2.1.2.2 System RAM memory maps

- Updated the 0x00400104 row in table UTest flash memory map:

Table 2-2. UTest flash memory map

Start address	End address	Allocated size [bytes]	Description	Comments
0x00400104	0x0040011F	28	Fuse Bypass Password (FA flash test password)	The FA flash test password must be left erased unless the application requires an additional password for testing the flash during failure analysis. If a password is required, additional programming is necessary. See the Security Reference Manual entry for "Fuse Bypass Password" for more information.

2.1.3 Device configuration

2.1.3.1 Clock Gating Module Enable 1 (IPS_CGM_EN1)

- Clock Gating Module Enable 0 (IPS_CGM_EN0) register is added under the section Platform Configuration Module.

Offset 18h

Access: Supervisor read/write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IPS_CGM_DMA1
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 2-2. IPS Clock Gating Enable 1 (IPS_CGM_EN1) register

Table 2-3. IPS_CGM_EN1 field description

Field	Description
0–30	Reserved
31 IPS_CGM_DMA1	IPS clock gating enable for DMA1 1 Enable clock gating, one IPS clock delay is introduced between master and slave. 0 Disable clock gating.

2.1.3.2 IPS Clock Gating Module Enable 0 (IPS_CGM_EN0)

- Changed the address offset of IPS Clock Gating Module Enable 0 register to 0x14h.

Offset: 14h Access: Supervisor read/write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	IPS_CGM_DMA0	0	0	0	IPS_CGM_MPU1	0	0	0	IPS_CGM_AXBS1	0	0	0	IPS_CGM_INTC
W																
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	IPS_CGM_MPU0	0	0	0	IPS_CGM_AXBS0	0	0	0	IPS_CGM_PRAM	0	0	0	IPS_CGM_PFLASH
W																
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Figure 2-3. IPS Clock Gating Module Enable 0 register

2.1.3.3 INTC implemented registers

- The following note has been added to the section:

NOTE

There are four cores implemented on this chip, but core 3 is strictly a checker core. The INTC only supports the three functional cores 0, 1, and 2. Therefore, the registers INTC_IACKR3, INTC_CPR3, and INTC_EOIR3 are not supported, and any attempt to access these registers results in a bus error. Also, writing to the HVEN3 bit in the INTC_BCR register has no effect.

2.1.3.4 Interrupt sources

- Removed the following interrupts not supported by the device from 'Table 7-23 Interrupt sources':
  - DSPI_0_SR(TFIWF)
  - DSPI_1_SR(TFIWF)

- DSPI_2_SR(TFIWF)
- DSPI_3_SR(TFIWF)
- DSPI_4_SR(TFIWF)
- DSPI_5_SR(TFIWF)
- DSPI_6_SR(TFIWF)
- DSPI_12_SR(TFIWF)

2.1.3.5 Default configuration

- Changed the reset values of SWT_CR [0, 1, 2, 3] registers.
  For SWT[0, 1, 3], the SWT_CR register reset value of 0xFF00_010A selects:
  - All masters allowed access
  - Reset on invalid access
  - Oscillator clock selected
  - Counter stops in debug mode
  - Watchdog is disabled

  For SWT[2], the SWT_CR register reset value of 0xFF00_011B selects:
  - All masters allowed access
  - Reset on invalid access
  - Oscillator clock selected
  - Counter stops in debug mode
  - Soft locked
  - Watchdog is enabled

2.1.3.6 FEC interface selection

- On this chip, the FEC interface depends on the settings of FEC_RCR[MII_MODE] (in the FEC) and the SoC Configuration Register0 SIUL2_SCR0[FEC_MODE].

Table 2-4. FEC interface selection

FEC_RCR[MII_MODE]	SIUL2_SCR0[FEC_MODE]	Interface used by the FEC
0	0 or 1	7-wire
1	0	RMII
	1	MII

2.1.3.7 LINFlexD configurations

- The Auto synchronization for Linflex1-16 changed from 'no' to 'n/a' in LINFlexD configurations table.

Table 2-5. LINFlexD configurations

Description	linflex_0	linflex_1	linflex_2	linflex_14	linflex_15	linflex_16
Number of filters implemented	16	0	0	0	0	0
Number of Tx DMA channels	1	1	1	1	1	1
Number of Rx DMA channels	1l	1	1	1	1	1
LIN operation mode	master/ slave	master	master	master	master	master
Auto synchronization	yes	n/a	n/a	n/a	n/a	n/a

2.1.3.8 SSCM_MEMCONFIG reset values

- In the table SSCM_MEMCONFIG reset values' updated the MREV and JPIN values.

Table 2-6. SSCM_MEMCONFIG reset values

Field	Field Definition	Value
MREV	Minor Revision	0001b
JPIN	JTAG Part ID	30Fh

2.1.3.9 Reset values on BAF exit

Added the section reset values on BAF exit under the section Boot Assist Flash (BAF) configuration.

- BAF interacts with various modules during its course of execution. BAF enables and disables the reset of values of registers for these modules. The reset values of some status registers which are not restored by BAF on exit are listed in the table below.

Table 2-7. Reset Values at Serial Boot

Sl. No.	Module Name	Register	BAF Exit Reset Value
1	MC_ME	MC_ME_RUN_PC_0	0xFE
2	MC_ME	MC_ME_DRUN	0x130072
3	MC_ME	MC_ME_GS	0x130072
4	MC_CGM	MC_CGM_SC_DC2	0x80010000
5	MC_CGM	MC_CGM_AC3_SC	0x0

Table continues on the next page...

Table 2-7. Reset Values at Serial Boot (continued)

Sl. No.	Module Name	Register	BAF Exit Reset Value
6	MC_CGM	MC_CGM_AC0_SC	0x02000000
7	MC_CGM	MC_CGM_AC0_DC4	0x80000000
8	MC_CGM	MC_CGM_AC8_SC	0x01000000
9	MC_CGM	MC_CGM_AC8_DC0	0x80000000
10	PLLDIG	PLLDIG_PLL0DV	0x00061021
11	FCCU	FCCU_RF_CFG_0	0xFFFFEFFF

Table 2-8. Reset Values at Flash Boot

Sl. No.	Module Name	Register	BAF Exit Reset Value
1	MC_ME	ME_IS	0x00000001
2	MC_ME	ME_DMTS	0x30000000
3	FCCU	FCCU_RF_CFG_0	0xFFFFEFFF

2.1.3.10 LVD /HVD self test decoding

- Entries updated under column 'LVD / HVD under test' in the table LVD /HVD self test decoding:

Table 2-9. LVD /HVD self test decoding

Current Name	New Name
POR098_C	LVD096_C
LVD114_C	LVD112_C
POR098_F	LVD096_F
LVD114_F	LVD108_F
LVD114_P	LVD108_P
LVD114_H	LVD108_C
LVD280_IF2	LVD270_IF2
LVD280_IE	LVD270_IE
LVD280_C	LVD270_C
LVD280_IF	LVD270_IF
LVD280_IM	LVD270_IM
LVD280_IJ	LVD270_IJ
LVD280_O	LVD270_O
LVD300_F	LVD295_F
LVD300_A	LVD295_A

2.1.3.11 FCCU chip-specific register reset values

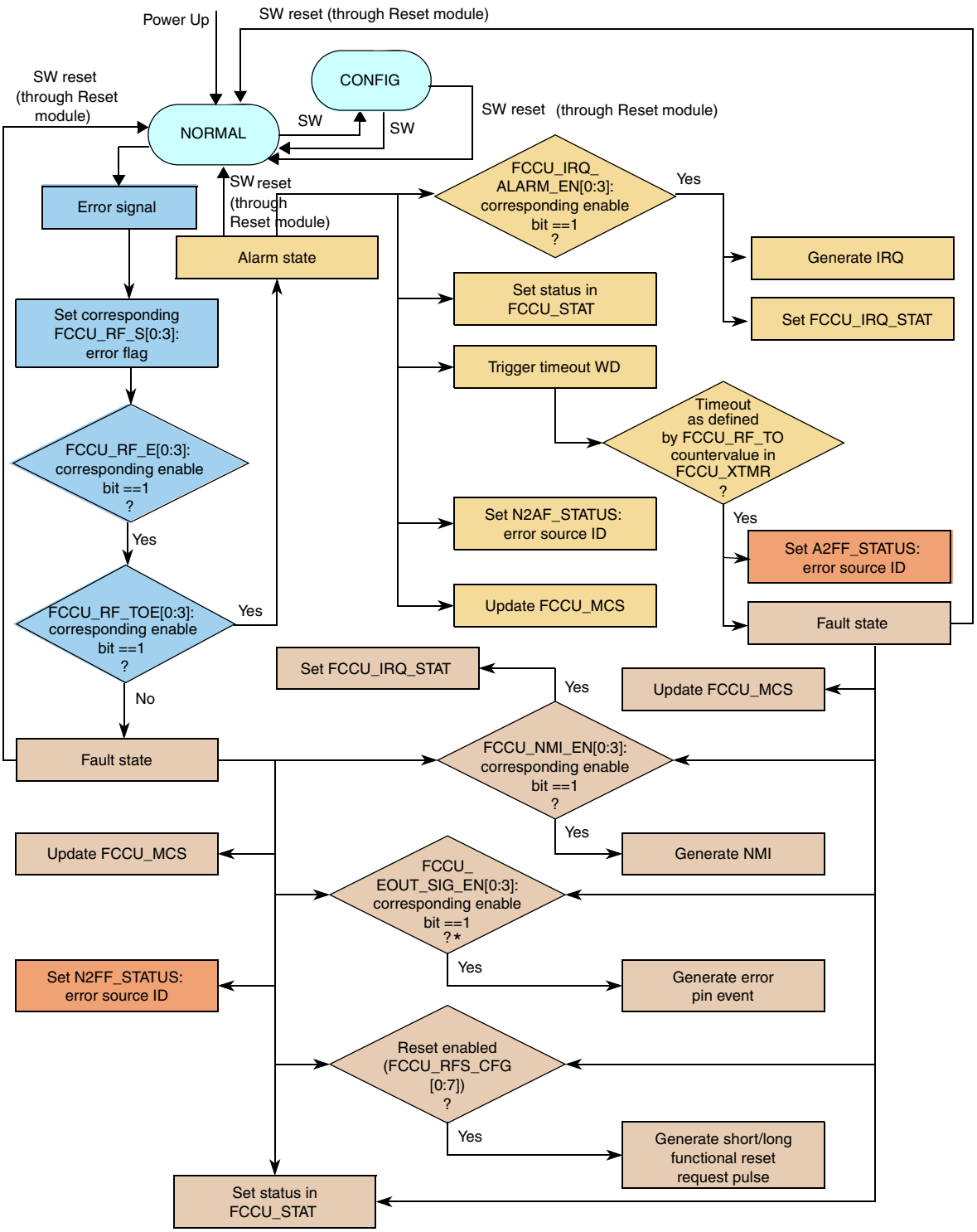
This table lists in alphabetical order by mnemonic the FCCU registers whose reset values are specific to this chip.

Table 2-10. Availability and reset values of selected FCCU registers

Register	Reset value
FCCU_CFG	0x0000_0000
FCCU_CFG_TO	0x0000_0006
FCCU_MCS	0x0000_0000
FCCU_RF_CFG0	0xFFFF_FFFF
FCCU_RF_CFG1	0xFFFF_FFFF
FCCU_RF_CFG2	0xFFFF_FFFF
FCCU_RF_CFG3	0xFFFF_FFFF
FCCU_RF_E0	0xFFFF_FFFF
FCCU_RF_E1	0xFFFF_FFFF
FCCU_RF_E2	0xFFFF_FFFF
FCCU_RF_E3	0xFFFF_FFFF
FCCU_RF_TO	0x0000_FFFF
FCCU_RF_TOE0	0xFFFF_FFFF
FCCU_RF_TOE1	0xFFFF_FFFF
FCCU_RF_TOE2	0xFFFF_FFFF
FCCU_RF_TOE3	0xFFFF_FFFF
FCCU_RFS_CFG0	0x0000_0000
FCCU_RFS_CFG1	0x0000_0000
FCCU_RFS_CFG2	0x0000_0000
FCCU_RFS_CFG3	0x0000_0000
FCCU_RFS_CFG4	0x0000_0000
FCCU_RFS_CFG5	0x0000_0000
FCCU_RFS_CFG6	0x0000_0000
FCCU_RFS_CFG7	0x0000_0000

2.1.3.12 Error signal flow

In the Figure 2-4, added a footnote 'This condition must be satisfied only when FCCU is configured for Bistable fault-output mode (FCCU_CFG[FOM])'.



* This condition must be satisfied only when FCCU is configured for Bistable fault-output mode (FCCU_CFG[FOM]).

Figure 2-4. Error signal flow

2.1.3.13 FCCU failure inputs

- Editorial updates in the footnotes of Table 7-86. FCCU failure inputs:
  - Added cross reference to Figure 26-1 and Figure 26-2 Clock generation in footnote number 12.
  - Removed the footnote number 14.
  - Changed 200z4 Core to z7 core in footnote number 18.
  - For Channel 31 updated the footnotes to Channel 31 [1,13].

2.1.4 DCI signals

The DCI sends and receives the $\overline{\text{EVTI}}$[1:0] and $\overline{\text{EVTO}}$[1:0] signals to/from the cores and other modules. The tables below summarize the source and destination of $\overline{\text{EVTI}}$, $\overline{\text{EVTO}}$, and related signals for the PD and the BD. For example, for the PD, $\overline{\text{EVTI}}$[0] are outputs of the JTAGM and SPU and inputs to the cores, HSM, GTM, and NXMC.

Table 2-11. PD DCI signals

Signal	Cores	HSM	GTM	NXMC	NAR	JTAGM	SPU	DTS
$\overline{\text{EVTI}}$[0]	I	I	I	I	—	O	I/O	—
$\overline{\text{EVTI}}$[1]	—	—	—	—	—	O	I/O	—
$\overline{\text{EVTO}}$[0]	O	O	O	O	—	I[1]	I/O	—
$\overline{\text{EVTO}}$[1]	—	—	—	—	—	I[1]	I/O	O
Core debug event	I	—	—	—	—	—	—	—
DCI cross triggering	O	—	O	—	—	—	—	—

1. The EVTO signal provided to the JTAGM is stretched by the DCI on the 16MHz IRC clock. Therefore, the incoming EVTO cannot be reliably detected by the JTAGM when the JTAGM clock is configured at less than 32MHz.

Table 2-12. BD DCI signals

Signal	RWA	NAR	NAL	JTAGM
$\overline{\text{EVTI}}$[0]	—	I	—	O
$\overline{\text{EVTI}}$[1]	—	—	—	O
$\overline{\text{EVTO}}$[0]	—	—	—	I[1]
$\overline{\text{EVTO}}$[1]	—	—	—	I[1]

1. The EVTO signal provided to the JTAGM is stretched by the DCI on the 16MHz IRC clock. Therefore, the incoming EVTO cannot be reliably detected by the JTAGM when the JTAGM clock is configured at less than 32MHz.

The DCI sends the system debug signal, ipg_debug, to the modules below. For details regarding module functionality during system debug, refer to the individual module chapter.

- AMU
- CAN
- LFAST (Interprocessor Communications instance only)
- DSPI
- eDMA
- FCCU
- GTMINT
- I2C
- NXMC
- PIT
- PSI5
- SARADC
- SDADC
- SRX
- SSCM
- STM
- SWT

2.1.4.1 DCI $\overline{\text{EVTx}}$ Pin Multiplexing Control Register (DCI_PINCR)

The DCI $\overline{\text{EVTx}}$ Pin Multiplexing Control Register (DCI_PINCR) is described below. The $\overline{\text{EVTI}}$ and $\overline{\text{EVTO}}$ functions share the same set of possible pins. If this register is written to enable both $\overline{\text{EVTI}}$ and $\overline{\text{EVTO}}$ on the same pin, the $\overline{\text{EVTI}}$ function is selected, although this type of programming should be avoided. Programming the $\overline{\text{EVTI}}$ fields to select $\overline{\text{EVTI}}$[0] or $\overline{\text{EVTI}}$[1] inputs to come from more than one pin is considered a programming error and no pin is enabled.

	31	30	29	28	27	26	25	24
R W	Reserved							EVTO0E

Table continues on the next page...

Reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
R/W	Reserved			EVTI1E	Reserved			EVTI0E
Reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
R/W	EVTO1D	EVTO1C	EVTO1B	EVTO1A	EVTO0D	EVTO0C	EVTO0B	EVTO0A
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R/W	EVTI1D	EVTI1C	EVTI1B	EVTI1A	EVTI0D	EVTI0C	EVTI0B	EVTI0A
Reset	0	0	0	0	0	0	0	0

Table 2-13. DCI_PINCR field descriptions

Field	Description
24 EVTO0E	Enables $\overline{\text{EVTO}}$[0] function on pin PA[8]
20 EVTI1E	Enables $\overline{\text{EVTI}}$[1] function on pin PA[9]
16 EVTI0E	Enables $\overline{\text{EVTI}}$[0] function on pin PA[8]
15 EVTO1D	Enables $\overline{\text{EVTO}}$[1] function on pin PA[9]
14 EVTO1C	Enables $\overline{\text{EVTO}}$[1] function on pin PM[6]
13 EVTO1B	Enables $\overline{\text{EVTO}}$[1] function on pin PK[14]
12 EVTO1A	Enables $\overline{\text{EVTO}}$[1] function on pin PH[11]
11 EVTO0D	Enables $\overline{\text{EVTO}}$[0] function on pin PM[5]
10 EVTO0C	Enables $\overline{\text{EVTO}}$[0] function on pin PM[4]
9 EVTO0B	Enables $\overline{\text{EVTO}}$[0] function on pin PF[15]
8	Enables $\overline{\text{EVTO}}$[0] function on pin PF[14]

Table continues on the next page...

Table 2-13. DCI_PINCR field descriptions (continued)

Field	Description
EVTO0A	
7 EVTI1D	Enables $\overline{\text{EVTI}}$[1] function on pin PM[7]
6 EVTI1C	Enables $\overline{\text{EVTI}}$[1] function on pin PM[6]
5 EVTI1B	Enables $\overline{\text{EVTI}}$[1] function on pin PK[14]
4 EVTI1A	Enables $\overline{\text{EVTI}}$[1] function on pin PH[11]
3 EVTI0D	Enables $\overline{\text{EVTI}}$[0] function on pin PM[5]
2 EVTI0C	Enables $\overline{\text{EVTI}}$[0] function on pin PM[4]
1 EVTI0B	Enables $\overline{\text{EVTI}}$[0] function on pin PF[15]
0 EVTI0A	Enables $\overline{\text{EVTI}}$[0] function on pin PF[14]

2.1.5 Core description

2.1.5.1 DMEM Control register 0

- The Reset value for DMEM Control Register 0 is updated to 0x0000_041C.