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Freescale Semiconductor
Technical Data

MPC7410EC
Rev. 6.1, 11/2007

MPC7410 RISC Microprocessor Hardware Specifications

The MPC7410 is a PowerPC™ reduced instruction set computing (RISC) microprocessor. This document describes pertinent electrical and physical characteristics of the MPC7410. For functional characteristics of the processor, refer to the *MPC7410 RISC Microprocessor User's Manual*.

To locate any published errata or updates for this document, refer to the web site at http://www.freescale.com.

Contents

1 Overview

The MPC7410 is the second implementation of the fourth generation (G4) microprocessors from Freescale. The MPC7410 implements the full PowerPC 32-bit architecture and is targeted at both computing and embedded systems applications.

Some comments on the MPC7410 with respect to the MPC750:

- The MPC7410 adds an implementation of the new AltiVec™ technology instruction set.
- The MPC7410 includes significant improvements in memory subsystem (MSS) bandwidth and offers an optional, high-bandwidth MPX bus interface.
- The MPC7410 adds full hardware-based multiprocessing capability, including a five-state cache coherency protocol (four MESI states plus a fifth state for shared intervention).

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- The MPC7410 is implemented in a next generation process technology for core frequency improvement.
- The MPC7410 floating-point unit has been improved to make latency equal for double- and single-precision operations involving multiplication.
- The completion queue has been extended to eight slots.
- There are no other significant changes to scalar pipelines, decode/dispatch/completion mechanisms, or the branch unit. The MPC750 four-stage pipeline model is unchanged (fetch, decode/dispatch, execute, complete/writeback).

Some comments on the MPC7410 with respect to the MPC7400:

- The MPC7410 adds configurable direct-mapped SRAM capability to the L2 cache interface.
- The MPC7410 adds 32-bit interface support to the L2 cache interface. The MPC7410 implements a 19th L2 address pin (L2ASPARE on the MPC7400) in order to support additional address range.
- The MPC7410 removes support for 3.3-V I/O on the L2 cache interface.

Figure 1 shows a block diagram of the MPC7410.

2 Features

This section summarizes features of the MPC7410 implementation of the PowerPC architecture. Major features of the MPC7410 are as follows:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to eight independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point, AltiVec permute, AltiVec ALU)
  - Serialization control (predispatch, postdispatch, execution serialization)

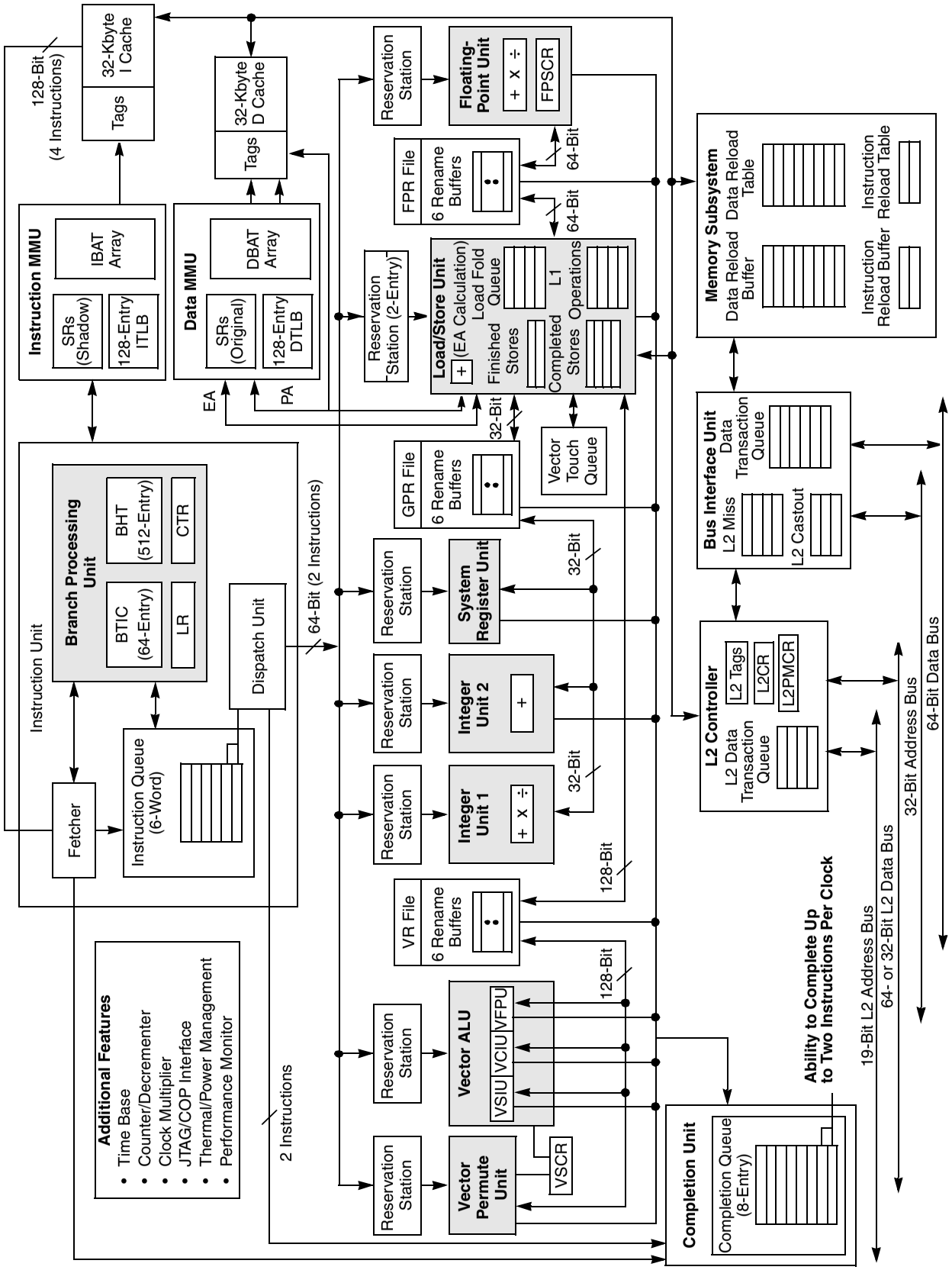


Figure 1. MPC7410 Block Diagram

- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Eight-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage floating-point unit and a 32-entry FPR file
  - Support for IEEE Std 754™ single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single- or double-precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- AltiVec unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit.
  - Contains its own 32-entry, 128-bit vector register file (VRF) with 6 renames
  - The vector ALU unit is further subdivided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU), and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/store unit
  - One-cycle load or store cache access (byte, half word, word, double word)
  - Two-cycle load latency with 1-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations

  - Store gathering
  - Executes the cache and TLB instructions
  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all four architecture AltiVec DST streams
- Level 1 (L1) cache structure
  - 32 Kbyte, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32 Kbyte, 32-byte line, eight-way set-associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports all PowerPC memory coherency modes
  - Nonblocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Level 2 (L2) cache interface
  - Internal L2 cache controller and tags; external data SRAMs
  - 512-Kbyte, 1-Mbyte, and 2-Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - 32-byte (512-Kbyte), 64-byte (1-Mbyte), or 128-byte (2-Mbyte) sectored line size
  - Supports pipelined (register-register) synchronous BurstRAMs and pipelined (register-register) late write synchronous BurstRAMs
  - Supports direct-mapped mode for 256 Kbytes, 512 Kbytes, 1 Mbyte, or 2 Mbytes of SRAM (either all, half, or none of L2 SRAM must be configured as direct-mapped)
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, ÷3, ÷3.5, and ÷4 supported
  - 64-bit data bus which also supports 32-bit bus mode
  - Selectable interface voltages of 1.8 and 2.5 V
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Four instruction BATs and four data BATs
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Snooped and invalidated for TLBI instructions
- Efficient data flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2, and the bus are 128 bits wide
  - dL1 is fully pipelined to provide 128 bits/cycle to/from the VRF

  - L2 is fully pipelined to provide 128 bits per L2 clock cycle to the L1s.
  - Up to eight outstanding, out-of-order, cache misses between dL1 and L2/bus
  - Up to seven outstanding, out-of-order transactions on the bus
  - Load folding to fold new dL1 misses into older, outstanding load and store misses to the same line
  - Store miss merging for multiple store misses to the same line. Only coherency action taken (that is, address only) for store misses merged to all 32 bytes of a cache line (no data tenure needed).
  - Two-entry finished store queue and four-entry completed store queue between load/store unit and dL1
  - Separate additional queues for efficient buffering of outbound data (castouts, write throughs, and so on) from dL1 and L2
- Bus interface
  - MPX bus extension to 60x processor interface
  - Mode-compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus
  - Bus-to-core frequency multipliers of 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 9x supported
  - Selectable interface voltages of 1.8, 2.5, and 3.3 V
- Power management
  - Low-power design with thermal requirements very similar to MPC740 and MPC750
  - Low-voltage processor core
  - Selectable interface voltages can reduce power in output buffers
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE Std 1149.1™ JTAG interface
  - Array built-in self test (ABIST)—factory test only
  - Redundancy on L1 data arrays and L2 tag arrays
- Reliability and serviceability
  - Parity checking on 60x and L2 cache buses

3 General Parameters

The following list provides a summary of the general parameters of the MPC7410:

Technology	0.18 µm CMOS, six-layer metal
Die size	6.32 mm × 8.26 mm (52 mm^2)
Transistor count	10.5 million
Logic design	Fully static
Packages	Surface mount 360 ceramic ball grid array (CBGA) Surface mount 360 high coefficient of thermal expansion ceramic ball grid array (HCTE_CBGA) Surface mount 360 high coefficient of thermal expansion ceramic ball grid array with lead free C5 spheres (HCTE_CBGA Lead Free C5 Spheres) Surface mount 360 high coefficient of thermal expansion ceramic land grid array (HCTE_LGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 3 for recommended operating conditions)
I/O power supply	1.8 V ± 100 mV DC or 2.5 V ± 100 mV 3.3 V ± 165 mV (system bus only) (input thresholds are configuration pin selectable)

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7410.

4.1 DC Electrical Characteristics

The tables in this section describe the MPC7410 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 2.1	V	4
PLL supply voltage		AV_{DD}	–0.3 to 2.1	V	4
L2 DLL supply voltage		$L2AV_{DD}$	–0.3 to 2.1	V	4
Processor bus supply voltage		OV_{DD}	–0.3 to 3.6	V	3, 6
L2 bus supply voltage		$L2OV_{DD}$	–0.3 to 2.8	V	3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.2 V	V	2, 5
	L2 bus	V_{in}	–0.3 to $L2OV_{DD}$ + 0.2 V	V	2, 5
	JTAG signals	V_{in}	–0.3 to OV_{DD} + 0.2 V	V	—
Storage temperature range		T_{stg}	–55 to 150	°C	—

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic	Symbol	Maximum Value	Unit	Notes
Rework temperature	T_{rwk}	260	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.2 V at any time including during power-on reset.
3. **Caution**: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 2.0 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a maximum value OV_{DD} of –0.3 to 2.8 V.

Figure 2 shows the allowable undershoot and overshoot voltage for the MPC7410.

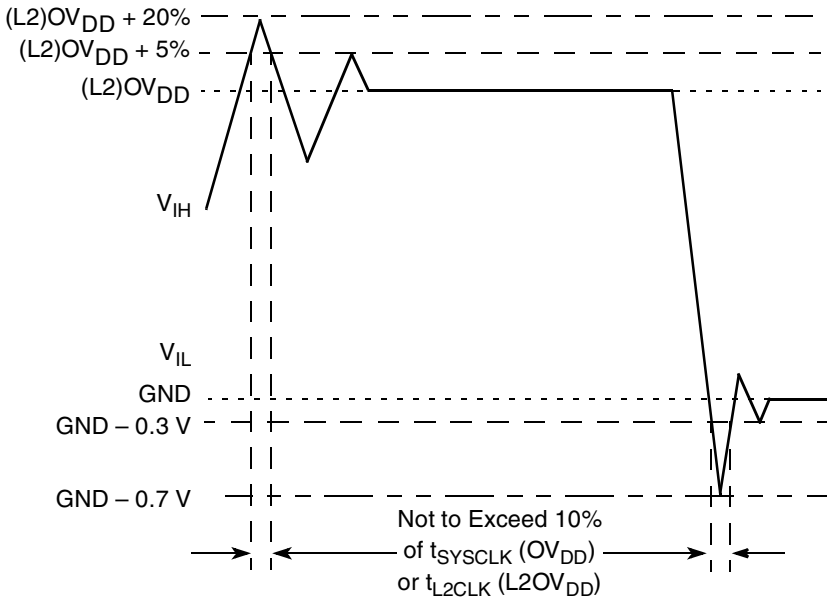


Figure 2. Overshoot/Undershoot Voltage

The MPC7410 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7410 core voltage must always be provided at nominal voltage (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. Voltage must be provided to the $L2OV_{DD}$ power pins even if the interface is not used. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL at the negation of the signal $\overline{\text{HRESET}}$. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 2. Input Threshold Voltage Setting

BVSEL Signal [3]	Processor Bus Input Threshold is Relative to:	L2VSEL Signal [3]	L2 Bus Input Threshold is Relative to:	Notes
0	1.8 V	0	1.8 V	1
$\overline{\text{HRESET}}$	2.5 V	$\overline{\text{HRESET}}$	2.5 V	1, 2
1	3.3 V	1	2.5 V	1, 4, 5
¬$\overline{\text{HRESET}}$	3.3 V	¬$\overline{\text{HRESET}}$	Not Supported	6

Notes:

1. **Caution:** The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.
2. To select the 2.5-V threshold option, BVSEL and/or L2VSEL should be tied to $\overline{\text{HRESET}}$ so that the two signals change state together. This is the preferred method for selecting this mode of operation.
3. To overcome the internal pull-up resistance, a pull-down resistance less than 250 Ω should be used.
4. Default voltage setting if left unconnected (internal pulled-up). MPC7410RX*nnn*LE (Rev 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD}; the default voltage setting if left unconnected is 2.5 V.
5. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD}; having BVSEL = 1 selects the 2.5-V threshold.
6. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support BVSEL = ¬$\overline{\text{HRESET}}$. (¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.)

Table 3 provides the recommended operating conditions for the MPC7410.

Table 3. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.8 V ± 100 mV	V	—
PLL supply voltage		AV_{DD}	1.8 V ± 100 mV	V	—
L2 DLL supply voltage		$L2AV_{DD}$	1.8 V ± 100 mV	V	—
Processor bus supply voltage	BVSEL = 0	OV_{DD}	1.8 V ± 100 mV	V	—
	BVSEL = $\overline{\text{HRESET}}$	OV_{DD}	2.5 V ± 100 mV	V	—
	BVSEL = ¬$\overline{\text{HRESET}}$ or BVSEL = 1	OV_{DD}	3.3 V ± 165 mV	V	2, 3
L2 bus supply voltage	L2VSEL = 0	$L2OV_{DD}$	1.8 V ± 100 mV	V	—
	L2VSEL = $\overline{\text{HRESET}}$ or L2VSEL = 1	$L2OV_{DD}$	2.5 V ± 100 mV	V	—
Input voltage	Processor bus and JTAG signals	V_{in}	GND to OV_{DD}	V	—
	L2 bus	V_{in}	GND to $L2OV_{DD}$	V	—
Die-junction temperature		T_j	0 to 105	°C	—

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a recommended OV_{DD} value of 2.5 V ± 100 mV for BVSEL = 1.
3. M*xx*7410*xxnnn*LE (Rev. 1.4) and later only. Previous revisions do not support BVSEL = ¬$\overline{\text{HRESET}}$.

Table 4 provides the package thermal characteristics for the MPC7410.

Table 4. Package Thermal Characteristics

Characteristic	Symbol	Value		Unit	Notes
		MPC7410 CBGA	MPC7410 HCTE		
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	18	20	°C/W	1, 2
Junction-to-ambient thermal resistance, 1m/sec airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	16	°C/W	1, 2
Junction-to-ambient thermal resistance, 2m/sec airflow, four-layer (2s2p) board	$R_{\theta JMA}$	13	15	°C/W	1, 2
Junction-to-board thermal resistance	$R_{\theta JB}$	9	11	°C/W	3

Table 4. Package Thermal Characteristics (continued)

Characteristic	Symbol	Value		Unit	Notes
		MPC7410 CBGA	MPC7410 HCTE		
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	< 0.1	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active portion of the die and the calculated case temperature at the top of the die. The actual value of R JC is less than 0.1 °C/W.

Note: Refer to Section 8.8, "Thermal Management Information," for details on thermal management.

Table 5 provides the DC electrical characteristics for the MPC7410.

Table 5. DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	1.8	V_{IH}	$0.65 \times (L2)OV_{DD}$	$(L2)OV_{DD} + 0.2$	V	2, 3, 8
	2.5	V_{IH}	1.7	$(L2)OV_{DD} + 0.2$		
	3.3	V_{IH}	2.0	$OV_{DD} + 0.3$		
Input low voltage (all inputs except SYSCLK)	1.8	V_{IL}	–0.3	$0.35 \times (L2)OV_{DD}$	V	8
	2.5	V_{IL}	–0.3	$0.2 \times (L2)OV_{DD}$		
	3.3	V_{IL}	–0.3	0.8		
SYSCLK input high voltage	1.8	CV_{IH}	1.5	$OV_{DD} + 0.2$	V	2, 8
	2.5	CV_{IH}	2.0	$OV_{DD} + 0.2$		
	3.3	CV_{IH}	2.4	$OV_{DD} + 0.3$		
SYSCLK input low voltage	1.8	CV_{IL}	–0.3	0.2	V	8
	2.5	CV_{IL}	–0.3	0.4		
	3.3	CV_{IL}	–0.3	0.4		
Input leakage current, $V_{in} = L2OV_{DD}/OV_{DD}$	1.8	I_{in}	—	20	µA	2, 3, 6, 7
	2.5	I_{in}	—	35		
	3.3	I_{in}	—	70		

Table 5. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
High-Z (off-state) leakage current, V_{in} = $L2OV_{DD}/OV_{DD}$	1.8	I_{TSI}	—	20	µA	2, 3, 5, 7
	2.5	I_{TSI}	—	35		
	3.3	I_{TSI}	—	70		
Output high voltage, I_{OH} = –5 mA	1.8	V_{OH}	$(L2)OV_{DD}$ – 0.45	—	V	8
	2.5	V_{OH}	1.7	—		
	3.3	V_{OH}	2.4	—		
Output low voltage, I_{OL} = 5 mA	1.8	V_{OL}	—	0.45	V	8
	2.5	V_{OL}	—	0.4		
	3.3	V_{OL}	—	0.4		
Capacitance, V_{in} = 0 V, f = 1 MHz		C_{in}	—	6.0	pF	3, 4, 7

Notes:

1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes factory test signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and $L2OV_{DD}$, or both OV_{DD} and $L2OV_{DD}$ must vary in the same direction (for example, both OV_{DD} and $L2OV_{DD}$ vary by either +5% or –5%).
6. Measured at max $OV_{DD}/L2OV_{DD}$.
7. Excludes IEEE 1149.1 boundary scan (JTAG) signals.
8. For JTAG support: all signals controlled by BVSEL and L2VSEL will see $V_{IL}/V_{IH}/V_{OL}/V_{OH}/CV_{IH}/CV_{IL}$ DC limits of 1.8 V mode while either the EXTEST or CLAMP instruction is loaded into the IEEE 1149.1 instruction register by the UpdateIR TAP state until a different instruction is loaded into the instruction register by either another UpdateIR or a Test-Logic-Reset TAP state. If only $\overline{\text{TSRT}}$ is asserted to the part, and then a SAMPLE instruction is executed, there is no way to control or predict what the DC voltage limits are. If $\overline{\text{HRESET}}$ is asserted before executing a SAMPLE instruction, the DC voltage limits will be controlled by the BVSEL/L2VSEL settings during $\overline{\text{HRESET}}$. Anytime $\overline{\text{HRESET}}$ is not asserted (that is, just asserting $\overline{\text{TRST}}$), the voltage mode is not known until either EXTEST or CLAMP is executed, at which time the voltage level will be at the DC limits of 1.8 V.

Table 6 provides the power consumption for the MPC7410.

Table 6. Power Consumption for MPC7410

	Processor (CPU) Frequency			Unit	Notes
	400 MHz	450 MHz	500 MHz		
Full-On Mode					
Typical	4.2	4.7	5.3	W	1, 3
Maximum	9.5	10.7	11.9	W	1, 2
Doze Mode					
Maximum	4.3	4.8	5.3	W	1
Nap Mode					
Maximum	1.35	1.5	1.65	W	1
Sleep Mode					
Maximum	1.3	1.45	1.6	W	1
Sleep Mode—PLL and DLL Disabled					
Typical	600	600	600	mW	1
Maximum	1.1	1.1	1.1	W	1

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <5% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at 105°C and V_{DD} = 1.8 V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at 65°C and V_{DD} = 1.8 V in a system while running typical benchmarks.

4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7410. After fabrication, functional parts are sorted by maximum processor core frequency, see Section 4.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 10, “Ordering Information.”

4.2.1 Clock AC Specifications

Table 7 provides the clock AC timing specifications as defined in Figure 3.

Table 7. Clock AC Timing Specifications

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit	Notes
		400 MHz		450 MHz		500 MHz			
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	350	400	350	450	350	500	MHz	1
VCO frequency	f_{VCO}	700	800	700	900	700	1000	MHz	1
SYSCLK frequency	f_{SYSCLK}	33	133	33	133	33	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	30	7.5	30	7.5	30	ns	—
SYSCLK rise and fall time	t_{KR} and t_{KF}	—	0.5	—	0.5	—	0.5	ns/V	2
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	3
SYSCLK jitter	—	—	±150	—	±150	—	±150	ps	4
Internal PLL-relock time	—	—	100	—	100	—	100	µs	5

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 8.1, "PLL Configuration," for valid PLL_CFG[0:3] settings.
2. Rise and fall times measurement are determined by the slew rates of the bus interface, rather than by time. As a result, the 0.5 ns rise/fall time spec of the 1.8- and 2.5-V bus interfaces is equivalent to the 1 ns rise/fall time of the 3.3-V bus interface. Both interfaces required a 2 V/ns slew rate. The slew rate is measured as a 1-V change (from 0.2 to 1.2 V) in 0.5 ns for the 1.8- and 2.5-V bus interfaces, whereas the 3.3-V bus interface required a 2-V change (from 0.4 to 2.4 V) in 1 ns.
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short- and long-term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

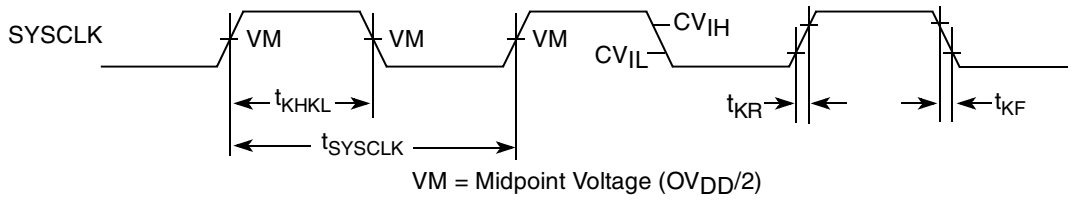


Figure 3. SYSCLK Input Timing Diagram

4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 as defined in Figure 4 and Figure 5. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

Table 8. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
Input setup	t_{IVKH}	1.0	—	ns	4
Input hold	t_{IXKH}	0	—	ns	4
Output valid times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSV} t_{KHARV} t_{KHOV}	 — — —	 3.0 2.3 3.0	ns	5, 6
Output hold times: TS $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ All other outputs	 t_{KHTSX} t_{KHARX} t_{KHOX}	 0.5 0.5 0.5	 — — —	ns	5
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	9
SYSCLK to output high impedance (all except $\overline{ABB}$/$\overline{AMON}$(0), $\overline{ARTRY}$/$\overline{SHD}$, $\overline{DBB}$/$\overline{DMON}$(0), $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	3.5	ns	
SYSCLK to $\overline{ABB}$/$\overline{AMON}$(0), $\overline{DBB}$/$\overline{DMON}$(0) high impedance after precharge	t_{KHABPZ}	—	1	t_{SYSCLK}	3, 7, 9
Maximum delay to $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 8, 9

Table 8. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 8, 9

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)— note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Includes mode select signals: BVSEL, EMODE, L2VSEL. See Figure 5 for mode select timing with respect to $\overline{\text{HRESET}}$.
5. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
6. Output valid time is measured from 2.4 to 0.8 V which may be longer than the time required to discharge from V_{DD} to 0.8 V.
7. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
8. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
9. Guaranteed by design and not tested.

Figure 4 provides the AC test load for the MPC7410.

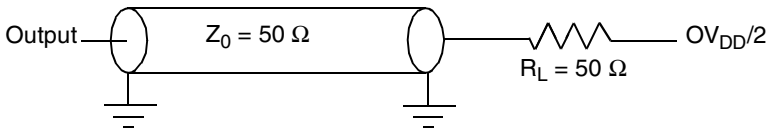


Figure 4. AC Test Load

Figure 5 provides the mode select input timing diagram for the MPC7410. The mode select inputs are sampled twice, once before and once after $\overline{\text{HRESET}}$ negation.

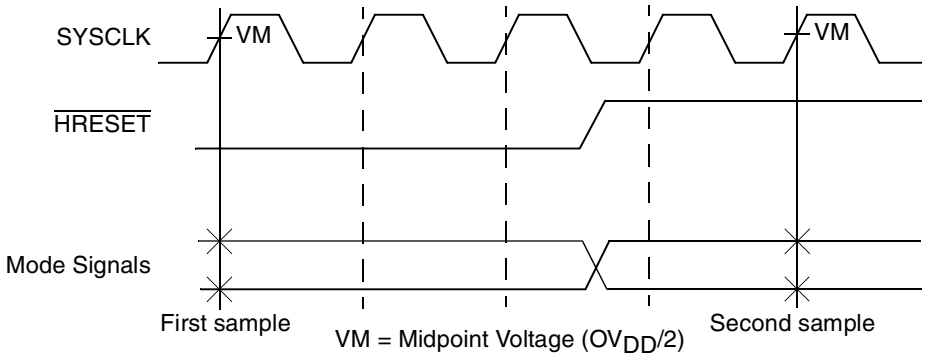


Figure 5. Mode Input Timing Diagram

Figure 6 provides the input/output timing diagram for the MPC7410.

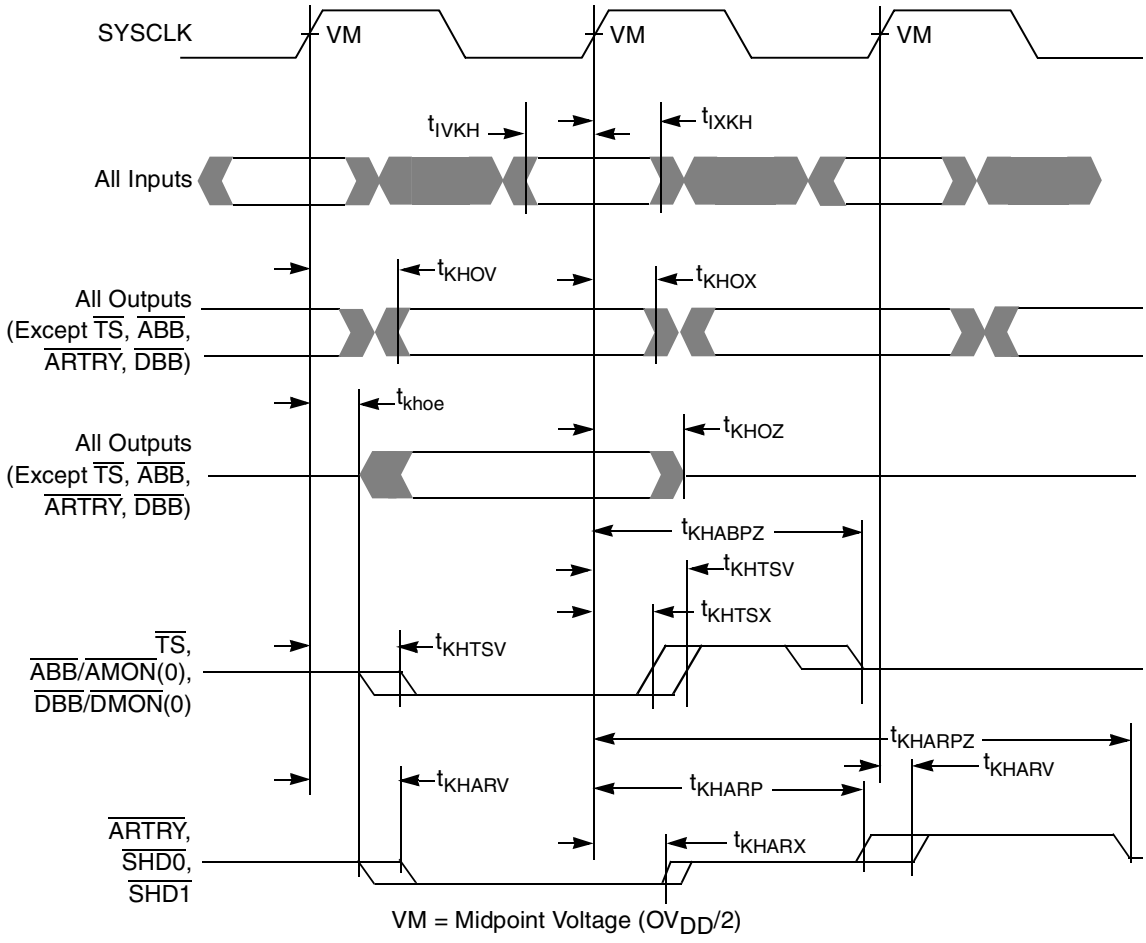


Figure 6. Input/Output Timing Diagram

4.2.3 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 14 for example core and L2 frequencies at various divisors. Table 9 provides the potential range of L2CLK output AC timing specifications as defined in Figure 7.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the MPC7410 to synchronize L2CLK_OUT at the SRAM with the processor's internal clock. L2CLK_OUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Freescale Application Note AN1794, *Backside L2 Timing Analysis for the PCB Design Engineer.*

The minimum L2CLK frequency in Table 9 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase-aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor that results in an L2 frequency below this minimum, or the L2CLK_OUT signals provided for SRAM clocking will not be phase-aligned with the MPC7410 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 9 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the MPC7410 will be a function of the AC timings of the MPC7410, the AC timings for the SRAM, bus loading, and printed-circuit board trace length.

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies in Table 9. Therefore, functional operation and AC timing information are tested at core-to-L2 divisors of two or greater.

L2 input and output signals are latched or enabled, respectively, by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings in Table 10 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLK_OUTA and L2CLK_OUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase-alignment with the internal L2CLK, the signals in Table 10 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

Table 9. L2CLK Output AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK frequency	f_{L2CLK}	133	400	133	400	133	400	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	7.5	2.5	7.5	2.5	7.5	ns	—
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	50		50		50		%	2
Internal DLL-relock time	—	640	—	640	—	640	—	L2CLK	3
DLL capture window	—	0	10	0	10	0	10	ns	5
L2CLK_OUT output-to-output skew	t_{L2CSKW}	—	50	—	50	—	50	ps	6

Table 9. L2CLK Output AC Timing Specifications (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK_OUT output jitter	—	—	±150	—	±150	—	±150	ps	6

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2CLK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. Guaranteed by design and not tested. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.

The L2CLK_OUT timing diagram is shown in Figure 7.

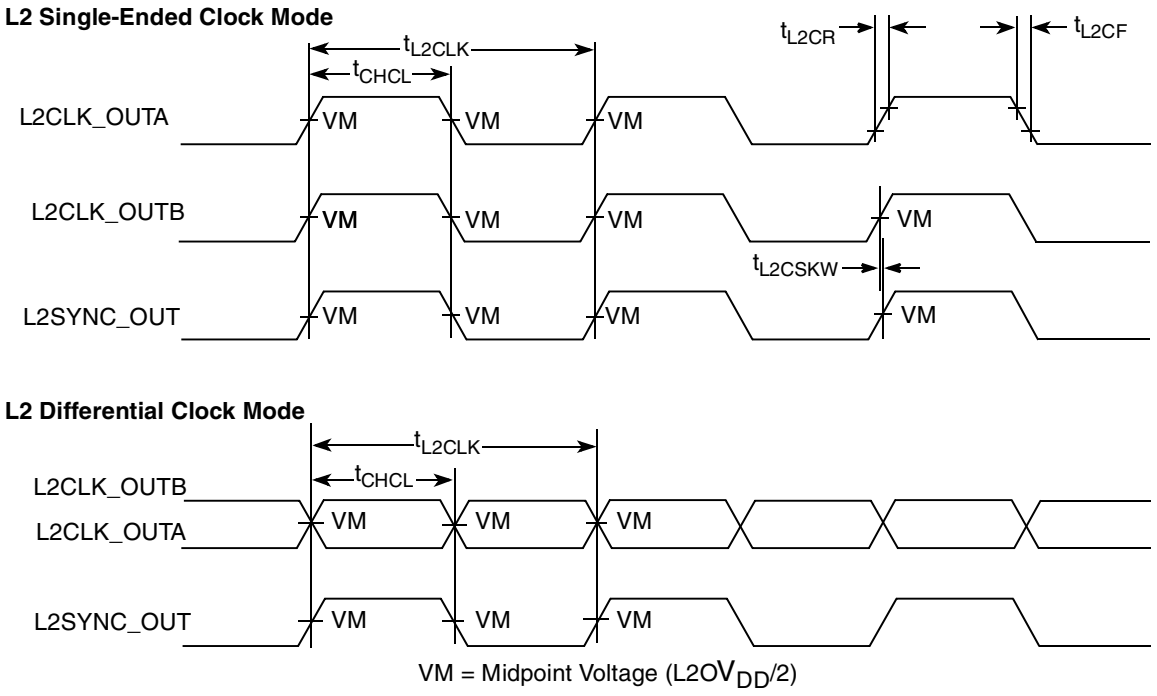


Figure 7. L2CLK_OUT Output Timing Diagram

4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 bus interface AC timing specifications for the MPC7410 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

Table 10. L2 Bus Interface AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	400, 450, 500 MHz		Unit	Notes
		Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR} and t_{L2CF}	—	1.0	ns	1
Setup times: Data and parity	t_{DVL2CH}	1.5	—	ns	2
Input hold times: Data and parity	t_{DXL2CH}	—	0.0	ns	2
Valid times: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOV}	 — — — —	 2.5 2.5 2.9 3.5	ns	3, 4
Output hold times All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOX}	 0.4 0.8 1.2 1.6	 — — — —	ns	3
L2SYNC_IN to high impedance: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOZ}	 — — — —	 2.0 2.5 3.0 3.5	ns	—

Notes:

1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 8). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14–15] = 00 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14–15] = 10 is recommended.

Figure 8 shows the L2 bus input timing diagrams for the MPC7410.

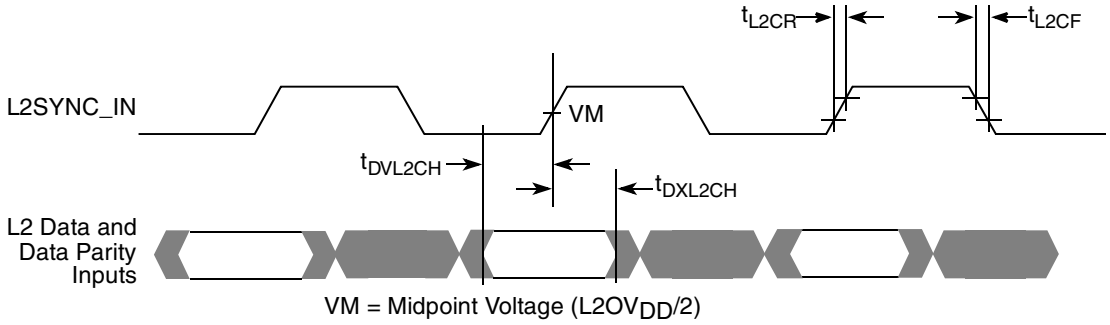


Figure 8. L2 Bus Input Timing Diagrams

Figure 9 shows the L2 bus output timing diagrams for the MPC7410.

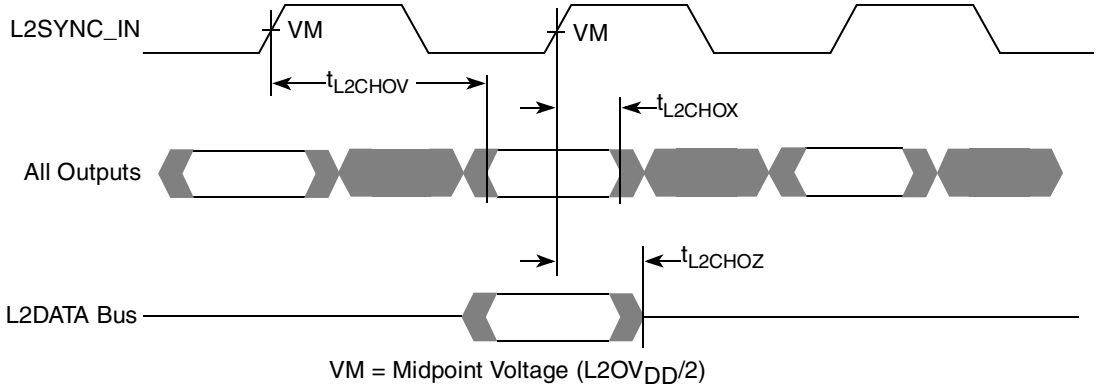


Figure 9. L2 Bus Output Timing Diagrams

Figure 10 provides the AC test load for L2 interface of the MPC7410.

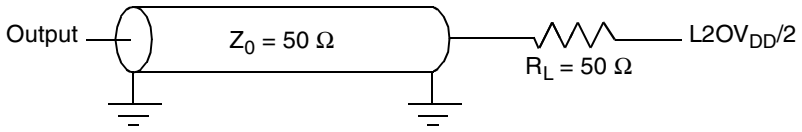


Figure 10. AC Test Load for the L2 Interface

4.2.5 IEEE 1149.1 AC Timing Specifications

Table 11 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	—
TCK cycle time	t_{TCLK}	30	—	ns	—
TCK clock pulse width measured at $OV_{DD}/2$	t_{JHJL}	15	—	ns	—
TCK rise and fall times	t_{JR} and t_{JF}	0	2	ns	—

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	 4, 5 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC7410.

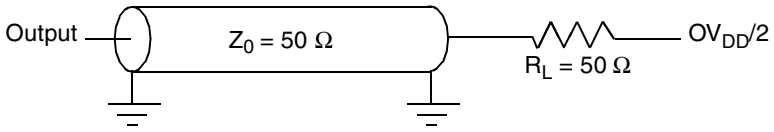


Figure 11. Alternate AC Test Load for the JTAG Interface

Figure 12 provides the JTAG clock input timing diagram.

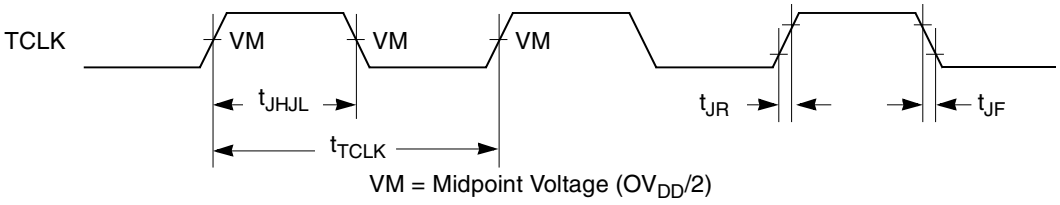


Figure 12. JTAG Clock Input Timing Diagram

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.

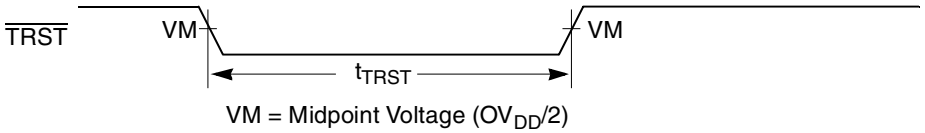


Figure 13. $\overline{\text{TRST}}$ Timing Diagram

Figure 14 provides the boundary-scan timing diagram.

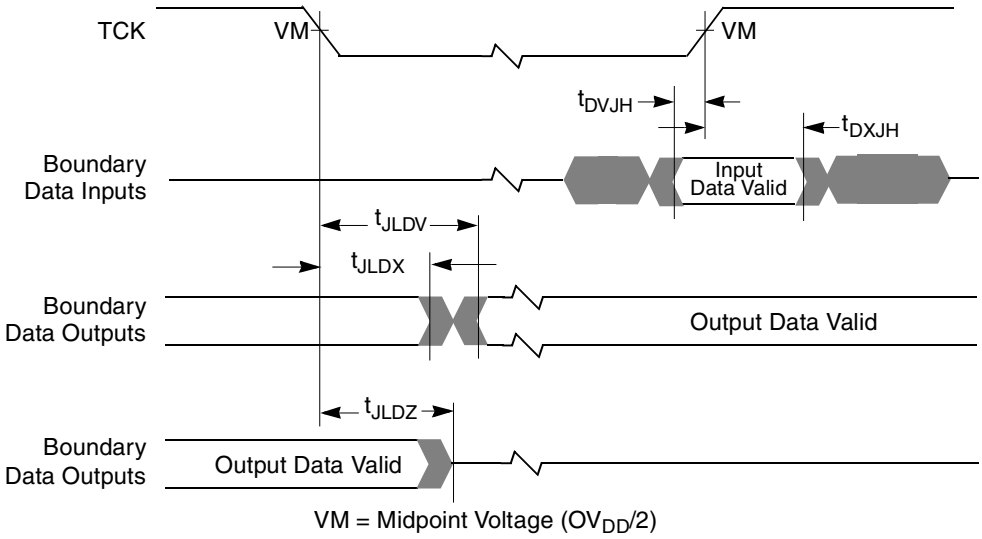


Figure 14. Boundary-Scan Timing Diagram

Figure 15 provides the test access port timing diagram.

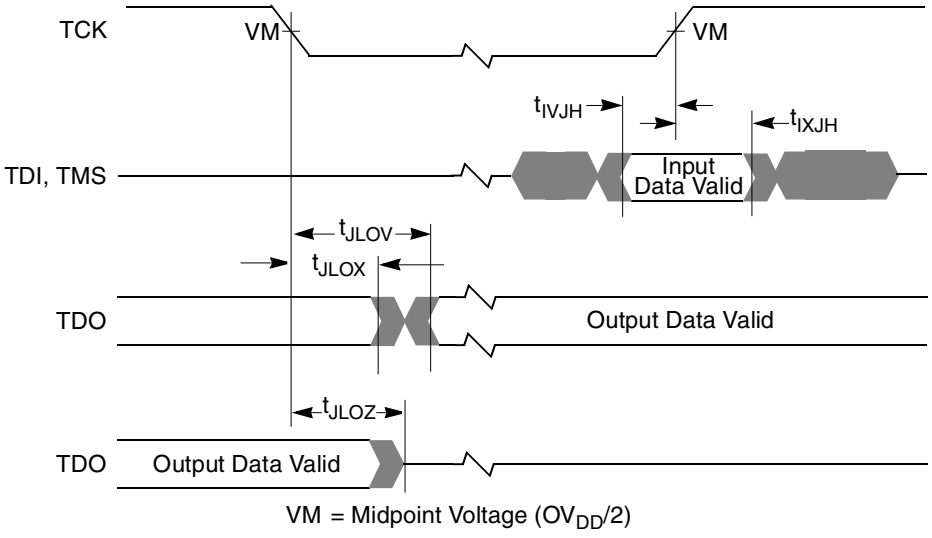
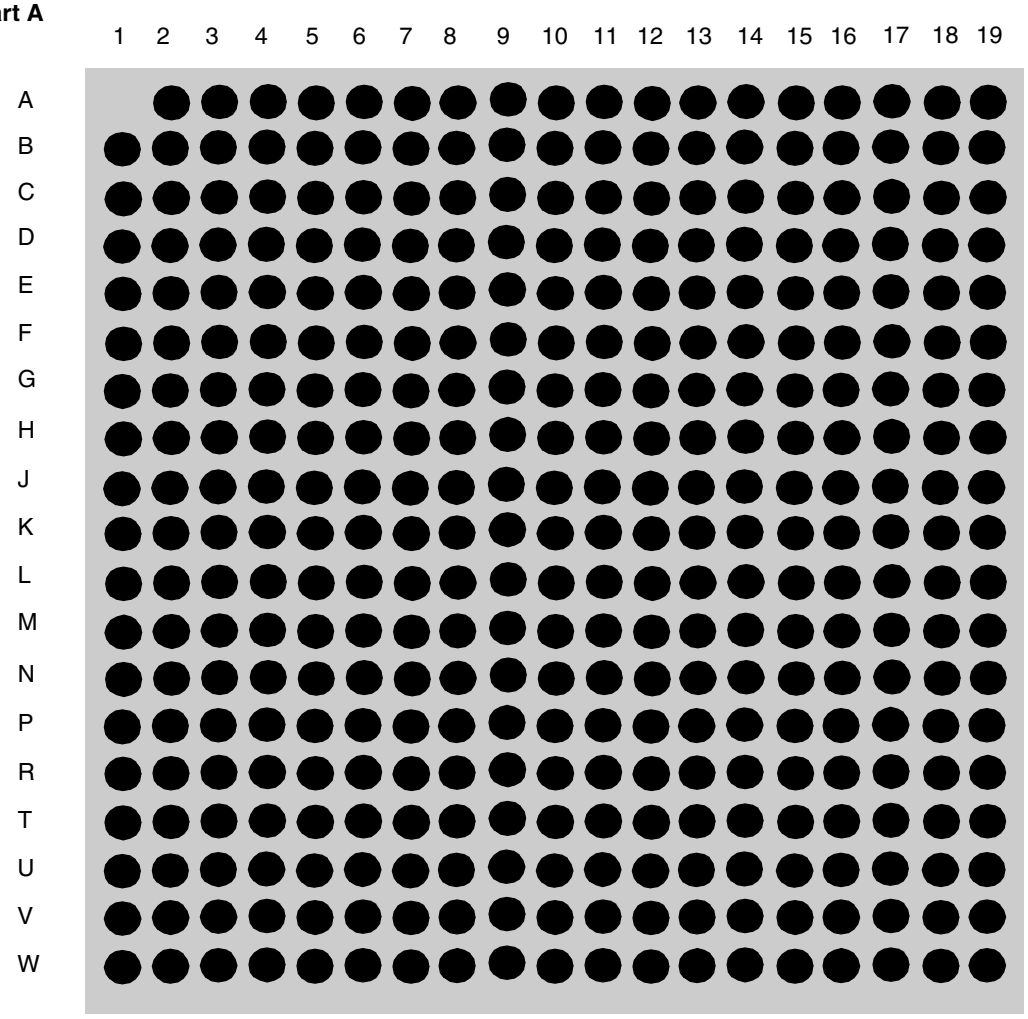


Figure 15. Test Access Port Timing Diagram

5 Pin Assignments

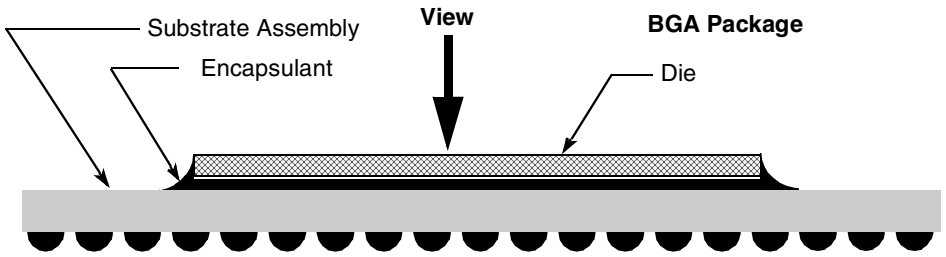
Figure 16, part A shows the pinout for the MPC7410, 360 CBGA, 360 HCTE, and 360 HCTE Lead Free C5 Spheres packages as viewed from the top surface. Figure 16, part B shows the side profile of the CBGA and HCTE_CBGA packages to indicate the direction of the top surface view. Figure 16, part C shows the side profile of the HCTE_LGA package to indicate the direction of the top surface view.

Part A



Not to Scale

Part B



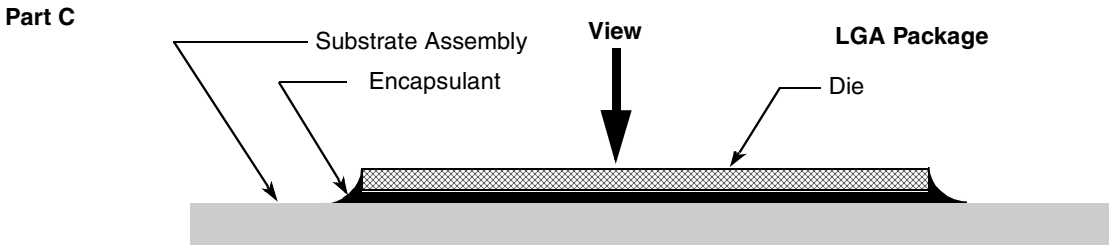


Figure 16. Pinout of the MPC7410, 360 CBGA and 360 HCTE Packages as Viewed from the Top Surface

6 Pinout Listings

Table 12 provides the pinout listing for the MPC7410 360 CBGA, 360 HCTE packages.

Table 12. Pinout Listing for the MPC7410, 360 CBGA and 360 HCTE Packages

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	BVSEL	
$\overline{\text{AACK}}$	N3	Low	Input	BVSEL	—
$\overline{\text{ABB}}$	L7	Low	Output	BVSEL	12, 16
AP[0:3]	C4, C5, C6, C7	High	I/O	BVSEL	—
$\overline{\text{ARTRY}}$	L6	Low	I/O	BVSEL	—
AV_{DD}	A8	—	Input	V_{DD}	—
$\overline{\text{BG}}$	H1	Low	Input	BVSEL	—
$\overline{\text{BR}}$	E7	Low	Output	BVSEL	—
BVSEL	W1	High	Input	N/A	1, 3, 8, 9, 14
$\overline{\text{CHK}}$	K11	Low	Input	BVSEL	2, 8, 9
$\overline{\text{CI}}$	C2	Low	I/O	BVSEL	—
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	BVSEL	—
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	BVSEL	—
CLK_OUT	E3	High	Output	BVSEL	—
$\overline{\text{DBB}}$	K5	Low	Output	BVSEL	12, 16
$\overline{\text{DBG}}$	K1	Low	Input	BVSEL	—
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	BVSEL	—