



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# MPC8250 Hardware Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC8250 PowerQUICC II™ communications processor.

The following topics are addressed:

The MPC8250 is available in two packages—the standard TBGA package (480 pins) and an alternate PBGA package (516 pins)—as described in [Section 4, “Pinout,”](#) and [Section 5, “Package Description.”](#) For more information on PBGA packages, contact your Freescale sales office. Note that throughout this document references to the MPC8250 are inclusive of its PBGA version unless otherwise specified.

## Contents

1. Features	2
2. Electrical and Thermal Characteristics	6
3. Clock Configuration Modes	20
4. Pinout	29
5. Package Description	55
6. Ordering Information	59
7. Document Revision History	59

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Figure 1 shows the block diagram for the MPC8250.

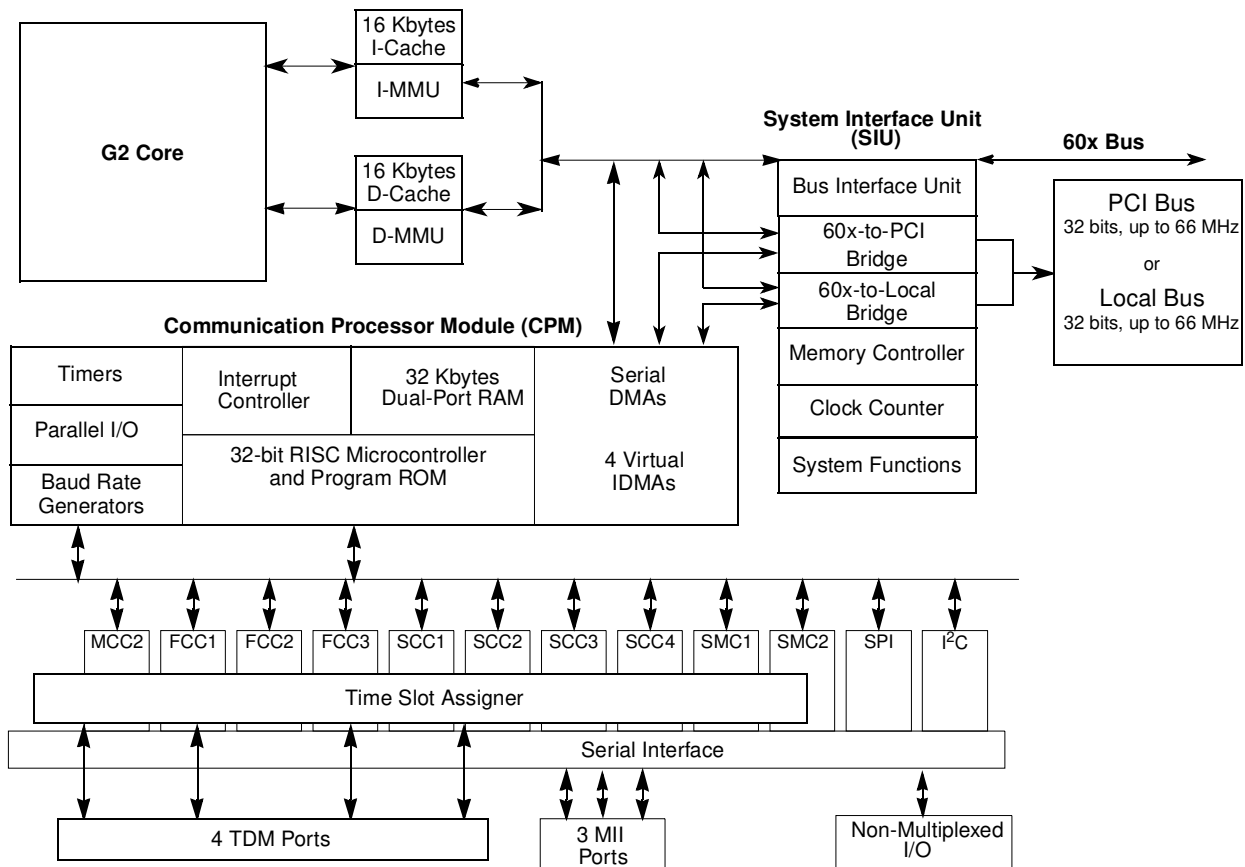


Figure 1. MPC8250 Block Diagram

# 1 Features

The major features of the MPC8250 are as follows:

- Footprint-compatible with the MPC8260
- Dual-issue integer core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 150–200 MHz
  - Separate 16-Kbyte data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - PowerPC architecture-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)



- Supports bus snooping for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic (1.8 V) and for I/O (3.3V)
- Separate PLLs for G2 core and for the CPM
  - G2 core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1™ JTAG test access port
- Twelve-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)

- Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3® CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - One multichannel controller (MCC2)
    - Handles 128 serial, full-duplex, 64-Kbps data channels. The MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
    - Transparent
    - UART (low-speed operation)
  - One serial peripheral interface identical to the MPC860 SPI
  - One inter-integrated circuit (I<sup>2</sup>C) controller (identical to the MPC860 I<sup>2</sup>C controller)
    - Microwire compatible
    - Multiple-master, single-master, and slave modes
  - Up to four TDM interfaces
    - Supports one group of four TDM channels

- 2,048 bytes of SI RAM
- Bit or byte resolution
- Independent transmit and receive routing, frame synchronization
- Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers
- PCI bridge
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI to 60x memory and 60x memory to PCI streaming
  - PCI Host Bridge or Peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - PCI-to-60x to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI
  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265A) required by the PCI standard as well as message and doorbell registers
  - Supports the I<sub>2</sub>O standard
  - Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66 MHz, 3.3 V specification
  - 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
  - Makes use of the local bus signals, so there is no need for additional pins

## 2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC8250.

### 2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC8250. [Table 1](#) shows the maximum electrical ratings.

**Table 1. Absolute Maximum Ratings**<sup>1</sup>

Rating	Symbol	Value	Unit
Core supply voltage <sup>2</sup>	VDD	-0.3 – 2.5	V
PLL supply voltage <sup>2</sup>	VCCSYN	-0.3 – 2.5	V
I/O supply voltage <sup>3</sup>	VDDH	-0.3 – 4.0	V
Input voltage <sup>4</sup>	VIN	GND(-0.3) – 3.6	V
Junction temperature	T <sub>j</sub>	120	°C
Storage temperature range	T <sub>STG</sub>	(-55) – (+150)	°C

<sup>1</sup> Absolute maximum ratings are stress ratings only; functional operation (see [Table 2](#)) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

<sup>2</sup> **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

<sup>3</sup> **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

<sup>4</sup> **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

[Table 2](#) lists recommended operational voltage conditions.

**Table 2. Recommended Operating Conditions**<sup>1</sup>

Rating	Symbol	Value			Unit
Core supply voltage	VDD	1.7 – 1.9 <sup>2</sup>	1.7–2.1 <sup>3</sup>	1.9–2.2 <sup>4</sup>	V
PLL supply voltage	VCCSYN	1.7 – 1.9 <sup>2</sup>	1.7–2.1 <sup>3</sup>	1.9–2.2 <sup>4</sup>	V
I/O supply voltage	VDDH	3.135 – 3.465			V
Input voltage	VIN	GND (-0.3) – 3.465			V
Junction temperature (maximum)	T <sub>j</sub>	105 <sup>5</sup>			°C
Ambient temperature	T <sub>A</sub>	0–70 <sup>5</sup>			°C

<sup>1</sup> **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

<sup>2</sup> CPU frequency less than or equal to 200 MHz.

<sup>3</sup> CPU frequency greater than 200 MHz but less than 233 MHz.

<sup>4</sup> CPU frequency greater than or equal to 233 MHz.

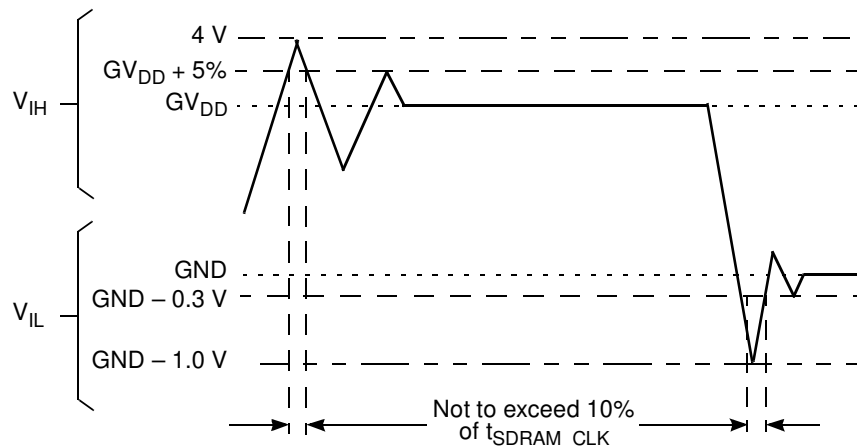
<sup>5</sup> Note that for extended temperature parts the range is  $(-40)_{T_A} - 105_{T_j}$ .

**NOTE: Core, PLL, and I/O Supply Voltages**

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (-5% and -0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or  $V_{CC}$ ).

Figure 2 shows the overshoot and undershoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.



**Figure 2. Overshoot/Undershoot Voltage**

Table 3 shows DC electrical characteristics.

**Table 3. DC Electrical Characteristics <sup>1</sup>**

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	$V_{IH}$	2.0	3.465	V
Input low voltage	$V_{IL}$	GND	0.8	V
CLKIN input high voltage	$V_{IHC}$	2.4	3.465	V
CLKIN input low voltage	$V_{ILC}$	GND	0.4	V
Input leakage current, $V_{IN} = VDDH^2$	$I_{IN}$	—	10	$\mu A$
Hi-Z (off state) leakage current, $V_{IN} = VDDH^2$	$I_{OZ}$	—	10	$\mu A$
Signal low input current, $V_{IL} = 0.8$ V	$I_L$	—	1	$\mu A$
Signal high input current, $V_{IH} = 2.0$ V	$I_H$	—	1	$\mu A$
Output high voltage, $I_{OH} = -2$ mA	$V_{OH}$	2.4	—	V



**Table 3. DC Electrical Characteristics <sup>1</sup> (continued)**

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 7.0\text{mA}$ $\overline{\text{BR}}$ $\overline{\text{BG}}$ $\overline{\text{ABB/IRQ2}}$ $\overline{\text{TS}}$ $\overline{\text{A[0-31]}}$ $\overline{\text{TT[0-4]}}$ $\overline{\text{TBST}}$ $\overline{\text{TSIZE[0-3]}}$ $\overline{\text{AACK}}$ $\overline{\text{ARTRY}}$ $\overline{\text{DBG}}$ $\overline{\text{DBB/IRQ3}}$ $\overline{\text{D[0-63]}}$ $\overline{\text{DP(0)/RSRV/EXT_BR2}}$ $\overline{\text{DP(1)/IRQ1/EXT_BG2}}$ $\overline{\text{DP(2)/TLBISYNC/IRQ2/EXT_DBG2}}$ $\overline{\text{DP(3)/IRQ3/EXT_BR3/CKSTP_OUT}}$ $\overline{\text{DP(4)/IRQ4/EXT_BG3/CORE_SRESET}}$ $\overline{\text{DP(5)/TBEN/IRQ5/EXT_DBG3}}$ $\overline{\text{DP(6)/CSE(0)/IRQ6}}$ $\overline{\text{DP(7)/CSE(1)/IRQ7}}$ $\overline{\text{PSDVAL}}$ $\overline{\text{TA}}$ $\overline{\text{TEA}}$ $\overline{\text{GBL/IRQ1}}$ $\overline{\text{CI/BADDR29/IRQ2}}$ $\overline{\text{WT/BADDR30/IRQ3}}$ $\overline{\text{L2_HIT/IRQ4}}$ $\overline{\text{CPU_BG/BADDR31/IRQ5}}$ $\overline{\text{CPU_DBG}}$ $\overline{\text{CPU_BR}}$ $\overline{\text{IRQ0/NMI_OUT}}$ $\overline{\text{IRQ7/INT_OUT/APE}}$ $\overline{\text{PORESET}}$ $\overline{\text{HRESET}}$ $\overline{\text{SRESET}}$ $\overline{\text{RSTCONF}}$ $\overline{\text{QREQ}}$	$V_{OL}$	—	0.4	V

Table 3. DC Electrical Characteristics <sup>1</sup> (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ $\overline{ALE}$ $\overline{BCTL0}$ $\overline{PWE}(0:7)/\overline{PSDDQM}(0:7)/\overline{PBS}(0:7)$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0:3]/\overline{LBS}[0-3]/\overline{PCI\_CFG}[0-3]$ $\overline{LSDA10}/\overline{LGPL0}/\overline{PCI\_MODCKH0}$ $\overline{LSDWE}/\overline{LGPL1}/\overline{PCI\_MODCKH1}$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}/\overline{PCI\_MODCKH2}$ $\overline{LSDCAS}/\overline{LGPL3}/\overline{PCI\_MODCKH3}$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}/\overline{LGPL5}/\overline{PCI\_MODCK}$ $\overline{LWR}$ $\overline{MODCK1}/\overline{AP}(1)/\overline{TC}(0)/\overline{BNKSEL}(0)$ $\overline{MODCK2}/\overline{AP}(2)/\overline{TC}(1)/\overline{BNKSEL}(1)$ $\overline{MODCK3}/\overline{AP}(3)/\overline{TC}(2)/\overline{BNKSEL}(2)$ $I_{OL} = 3.2\text{mA}$ $\overline{L\_A14}/\overline{PAR}$ $\overline{L\_A15}/\overline{FRAME}/\overline{SMI}$ $\overline{L\_A16}/\overline{TRDY}$ $\overline{L\_A17}/\overline{IRDY}/\overline{CKSTP\_OUT}$ $\overline{L\_A18}/\overline{STOP}$ $\overline{L\_A19}/\overline{DEVSEL}$ $\overline{L\_A20}/\overline{IDSEL}$ $\overline{L\_A21}/\overline{PERR}$ $\overline{L\_A22}/\overline{SERR}$ $\overline{L\_A23}/\overline{REQ0}$ $\overline{L\_A24}/\overline{REQ1}/\overline{HSEJSW}$ $\overline{L\_A25}/\overline{GNT0}$ $\overline{L\_A26}/\overline{GNT1}/\overline{HSLED}$ $\overline{L\_A27}/\overline{GNT2}/\overline{HSENUM}$ $\overline{L\_A28}/\overline{RST}/\overline{CORE\_SRESET}$ $\overline{L\_A29}/\overline{INTA}$ $\overline{L\_A30}/\overline{REQ2}$ $\overline{L\_A31}$ $\overline{LCL\_D}(0-31)/\overline{AD}(0-31)$ $\overline{LCL\_DP}(0-3)/\overline{C}/\overline{BE}(0-3)$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ $\overline{TDO}$	$V_{OL}$	—	0.4	V

- <sup>1</sup> The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.
- <sup>2</sup> The leakage current is measured for nominal VDD, VCCSYN, and VDD.

## 2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

**Table 4. Thermal Characteristics**

Characteristic	Symbol	Value		Unit	Air Flow
		480 TBGA	516 PBGA		
Junction to ambient— single-layer board <sup>1</sup>	$\theta_{JA}$	13	24	$^{\circ}\text{C}/\text{W}$	Natural convection
		10	18		1 m/s
Junction to ambient— four-layer board		11	16		Natural convection
		8	13		1 m/s
Junction to board <sup>2</sup>	$\theta_{JB}$	4	8	$^{\circ}\text{C}/\text{W}$	—
Junction to case <sup>3</sup>	$\theta_{JC}$	1.1	6	$^{\circ}\text{C}/\text{W}$	—

- <sup>1</sup> Assumes no thermal vias
- <sup>2</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- <sup>3</sup> Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

## 2.3 Power Considerations

The average chip-junction temperature,  $T_J$ , in  $^{\circ}\text{C}$  can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \tag{1}$$

where

- $T_A$  = ambient temperature  $^{\circ}\text{C}$
- $\theta_{JA}$  = package thermal resistance, junction to ambient,  $^{\circ}\text{C}/\text{W}$
- $P_D = P_{INT} + P_{I/O}$
- $P_{INT} = I_{DD} \times V_{DD}$  Watts (chip internal power)
- $P_{I/O}$  = power dissipation on input and output pins (determined by user)

For most applications  $P_{I/O} < 0.3 \times P_{INT}$ . If  $P_{I/O}$  is neglected, an approximate relationship between  $P_D$  and  $T_J$  is the following:

$$P_D = K / (T_J + 273^{\circ}\text{C}) \tag{2}$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273^{\circ}\text{C}) + \theta_{JA} \times P_D^2 \tag{3}$$

where  $K$  is a constant pertaining to the particular part.  $K$  can be determined from equation (3) by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of  $K$ , the values of  $P_D$  and  $T_J$  can be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ .

### 2.3.1 Layout Practices

Each  $V_{CC}$  pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The  $V_{CC}$  power supply should be bypassed to ground using at least four  $0.1 \mu\text{F}$  by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip  $V_{CC}$  and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as  $V_{CC}$  and GND planes.

All output pins on the MPC8250 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the  $V_{CC}$  and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above  $P_D = 3\text{W}$  (when the ambient temperature is  $70^\circ\text{C}$  or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

**Table 5. Estimated Power Dissipation for Various Configurations <sup>1</sup>**

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	$P_{INT}(W)$ <sup>2</sup>			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	—	—	2.3	2.9
66.66	3	4.5	200	300	—	—	2.4	3.1
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2.5	3.5	208	291	—	—	2.4	3.1

<sup>1</sup> Test temperature = room temperature ( $25^\circ\text{C}$ )

<sup>2</sup>  $P_{INT} = I_{DD} \times V_{DD}$  Watts

## 2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC8250 device. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in [Table 6](#).

**Table 6. Output Buffer Impedances <sup>1</sup>**

Output Buffers	Typical Impedance ( $\Omega$ )
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

<sup>1</sup> These are typical values at 65° C. The impedance may vary by  $\pm 25\%$  with process and temperature.

[Table 7](#) lists CPM output characteristics.

**Table 7. AC Characteristics for CPM Outputs <sup>1</sup>**

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

<sup>1</sup> Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

[Table 8](#) lists CPM input characteristics.

**Table 8. AC Characteristics for CPM Inputs <sup>1</sup>**

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2



**Table 8. AC Characteristics for CPM Inputs <sup>1</sup>**

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

<sup>1</sup> Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

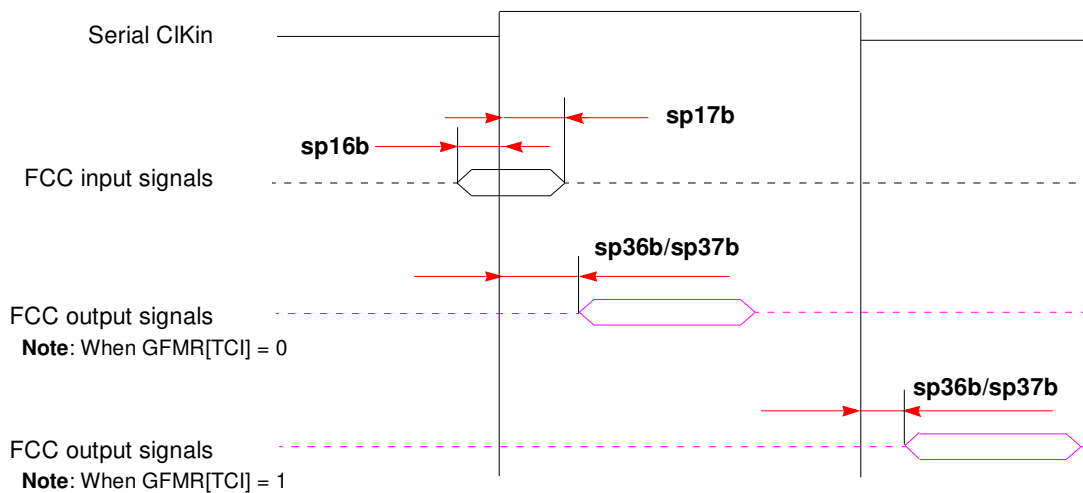

**Figure 3. FCC External Clock Diagram**

Figure 4 shows the FCC internal clock.

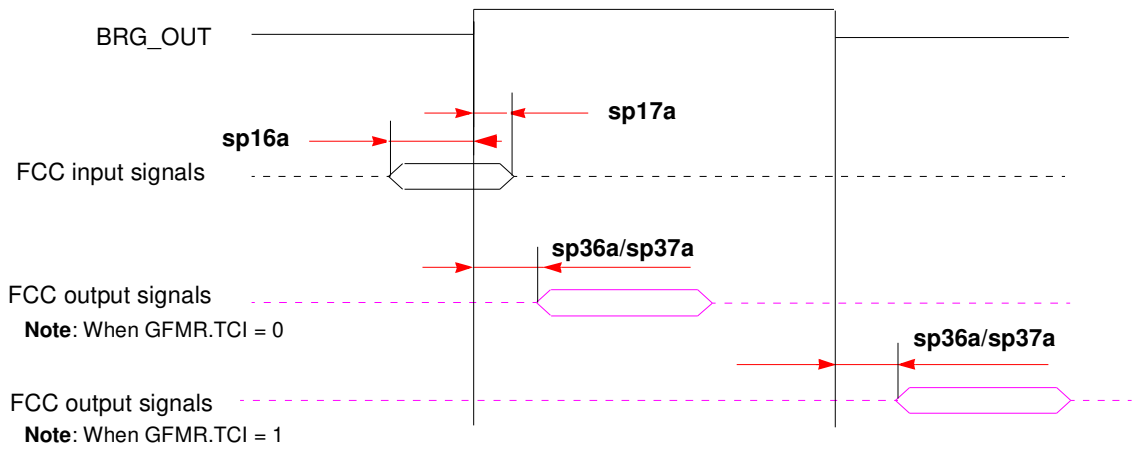
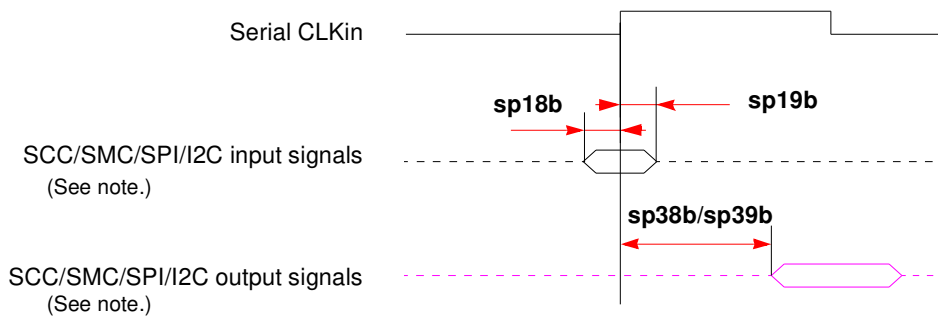


Figure 4. FCC Internal Clock Diagram

Figure 5 shows the SCC/SMC/SPI/I<sup>2</sup>C external clock.

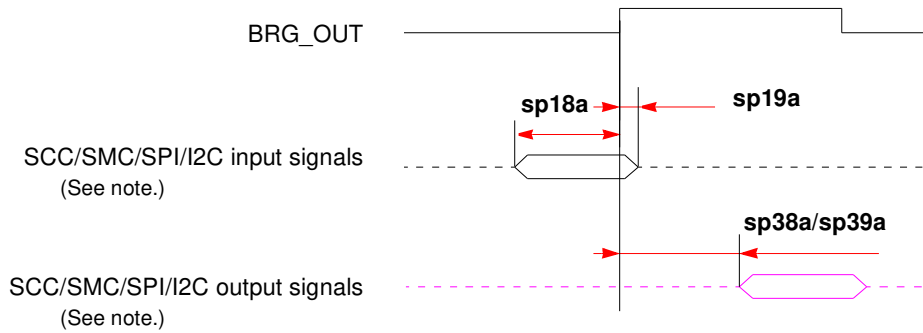


**Note:** There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I<sup>2</sup>C External Clock Diagram

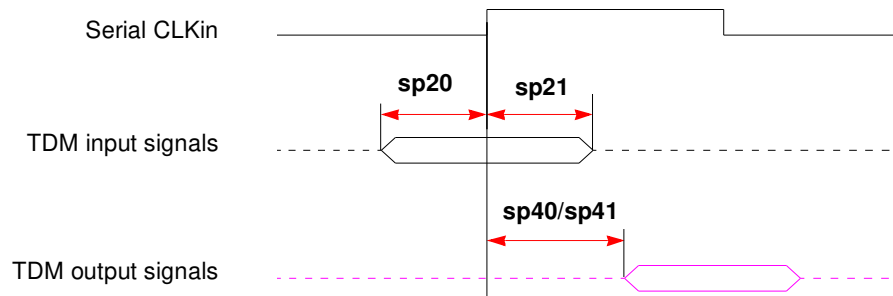
Figure 6 shows the SCC/SMC/SPI/I<sup>2</sup>C internal clock.



- Note:** There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
  2. Input sampled on the rising edge and output driven on the falling edge.
  3. Input sampled on the falling edge and output driven on the falling edge.
  4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 6. SCC/SMC/SPI/I<sup>2</sup>C Internal Clock Diagram**

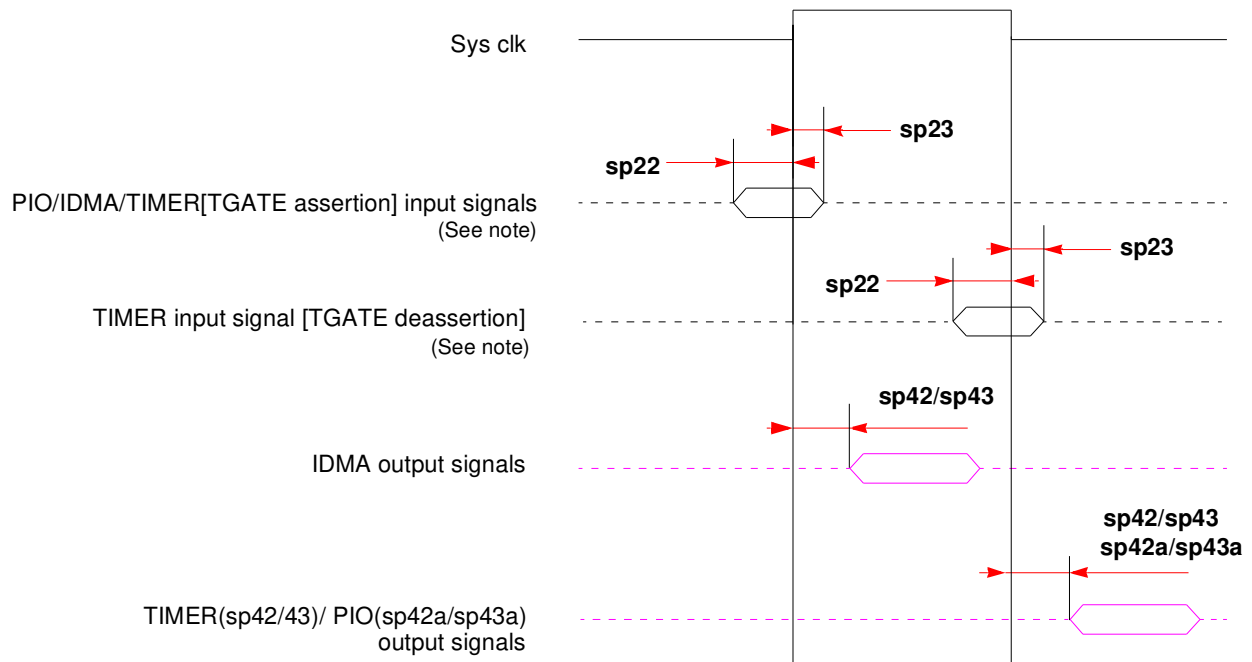
Figure 7 shows TDM input and output signals.



- Note:** There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
  2. Input sampled on the rising edge and output driven on the falling edge.
  3. Input sampled on the falling edge and output driven on the falling edge.
  4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 7. TDM Signal Diagram**

Figure 8 shows PIO, timer, and DMA signals.



**Note:** TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

**Figure 8. PIO, Timer, and DMA Signal Diagram**

Table 9 lists SIU input characteristics.

**Table 9. AC Characteristics for SIU Inputs <sup>1</sup>**

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	AACK/ARTRY/T $\bar{A}$ /TS/TEA/DBG/BG/BR	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

<sup>1</sup> Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 10 lists SIU output characteristics.

**Table 10. AC Characteristics for SIU Outputs <sup>1</sup>**

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	PSDVAL/TEA/TA	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

<sup>1</sup> Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

**NOTE**

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.



Figure 9 shows the interaction of several bus signals.

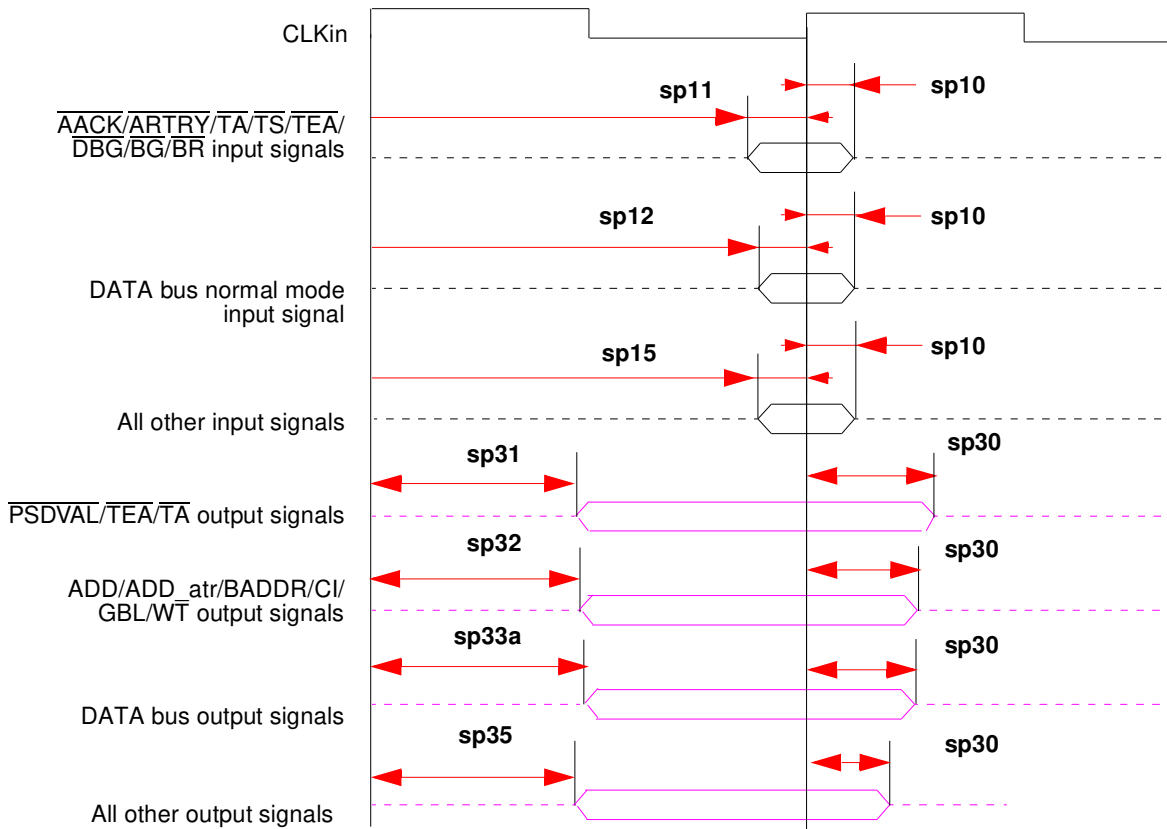


Figure 9. Bus Signals

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

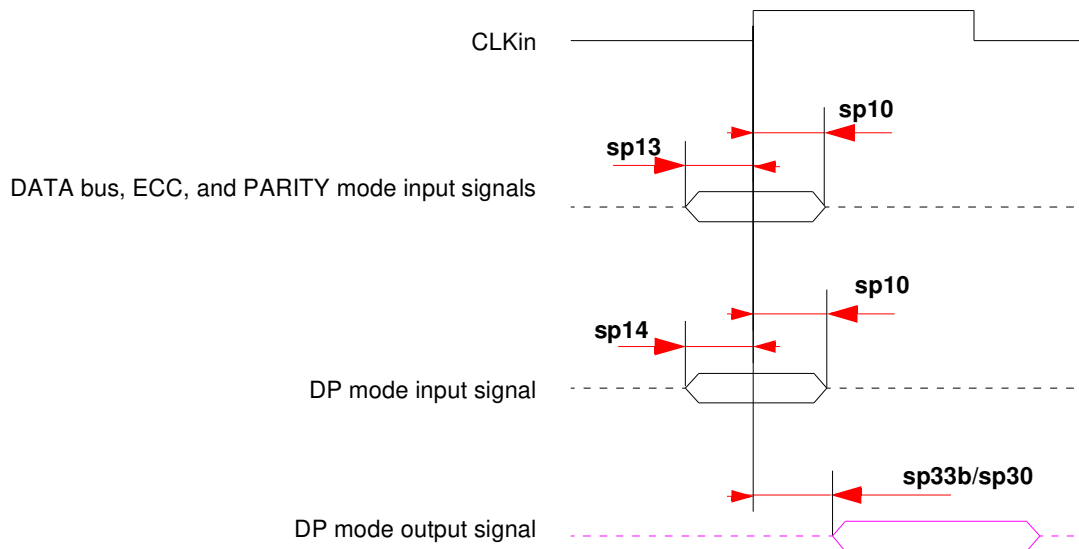


Figure 10. Parity Mode Diagram

Figure 11 shows signal behavior in MEMC mode.

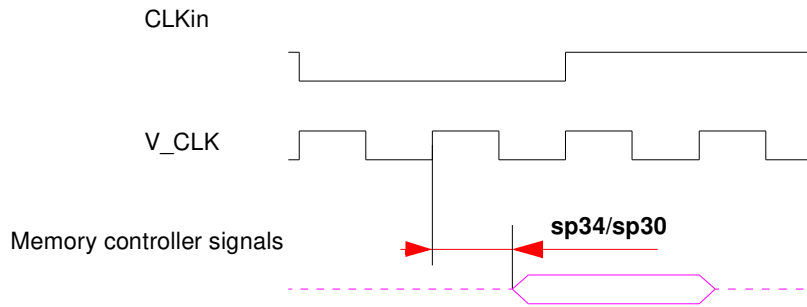


Figure 11. MEMC Mode Diagram

**NOTE**

Generally, all MPC8250 bus and system output signals are driven from the rising edge of the input clock (CLKIn). Memory controller signals, however, trigger on four points within a CLKIn cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKIn. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKIn)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKIn	1/2 CLKIn	3/4 CLKIn
1:2.5	3/10 CLKIn	1/2 CLKIn	8/10 CLKIn
1:3.5	4/14 CLKIn	1/2 CLKIn	11/14 CLKIn

Figure 12 is a graphical representation of Table 11.

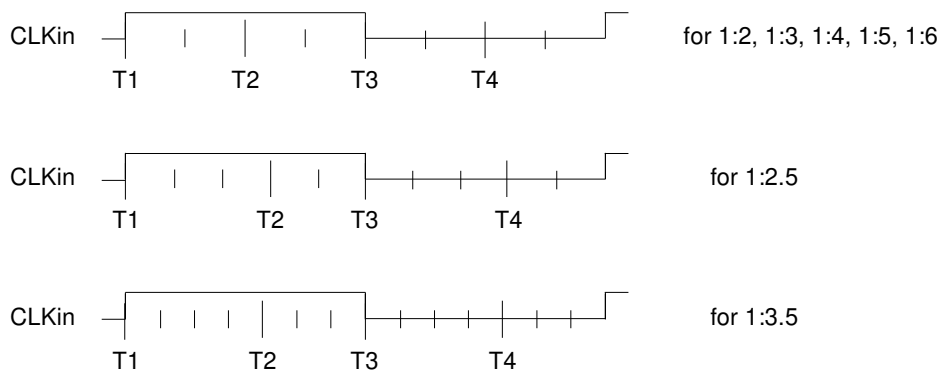


Figure 12. Internal Tick Spacing for Memory Controller Signals

**NOTE**

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKIn’s rising edge.

### 3 Clock Configuration Modes

The MPC8250 has three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins—PCI\_MODE, PCI\_CFG[0], PCI\_MODCK—as shown in [Table 12](#).

**Table 12. MPC8250 Clocking Modes**

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK <sup>1</sup>			
1	—	—	Local bus	—	<a href="#">Table 13</a> and <a href="#">Table 14</a>
0	0	0	PCI host	50–66	<a href="#">Table 15</a> and <a href="#">Table 16</a>
0	0	1		25–50	
0	1	0	PCI agent	50–66	<a href="#">Table 17</a> and <a href="#">Table 18</a>
0	1	1		25–50	

<sup>1</sup> Determines PCI clock frequency range. Refer to [Section 3.2, “PCI Mode.”](#)

In each clocking mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-up reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK\_H). Both the PLLs and the dividers are set according to the selected MPC8250 clock operation mode as described in the following sections.

**NOTE**

Clock configurations change only after  $\overline{\text{POR}}$  is asserted.

#### 3.1 Local Bus Mode

[Table 13](#) shows the eight basic clock configurations for the MPC8250. Another 49 configurations are available by using the configuration pin ( $\overline{\text{RSTCONF}}$ ) and driving four pins on the data bus.

**Table 13. Clock Default Configurations**

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz

**Table 13. Clock Default Configurations**

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 14 describes all possible clock configurations when using the hard reset configuration sequence. Note also that basic modes are shown in **boldface** type. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

**Table 14. Clock Configuration Modes <sup>1</sup>**

MODCK_H–MODCK[1–3]	Input Clock Frequency <sup>2,3</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency <sup>2</sup>	Core Multiplication Factor <sup>2</sup>	Core Frequency <sup>2</sup>
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	<b>33 MHz</b>	<b>4</b>	<b>133 MHz</b>	<b>4</b>	<b>133 MHz</b>
0010_011	<b>33 MHz</b>	<b>4</b>	<b>133 MHz</b>	<b>5</b>	<b>166 MHz</b>
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz

**Table 14. Clock Configuration Modes <sup>1</sup> (continued)**

MODCK_H–MODCK[1–3]	Input Clock Frequency <sup>2,3</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency <sup>2</sup>	Core Multiplication Factor <sup>2</sup>	Core Frequency <sup>2</sup>
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	<b>66 MHz</b>	<b>2</b>	<b>133 MHz</b>	<b>2.5</b>	<b>166 MHz</b>
0101_111	<b>66 MHz</b>	<b>2</b>	<b>133 MHz</b>	<b>3</b>	<b>200 MHz</b>
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	<b>66 MHz</b>	<b>2.5</b>	<b>166 MHz</b>	<b>2.5</b>	<b>166 MHz</b>
0110_101	<b>66 MHz</b>	<b>2.5</b>	<b>166 MHz</b>	<b>3</b>	<b>200 MHz</b>
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz



**Table 14. Clock Configuration Modes <sup>1</sup> (continued)**

MODCK_H–MODCK[1–3]	Input Clock Frequency <sup>2,3</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency <sup>2</sup>	Core Multiplication Factor <sup>2</sup>	Core Frequency <sup>2</sup>
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

<sup>1</sup> Because of speed dependencies, not all of the possible configurations in Table 14 are applicable.

<sup>2</sup> The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than 133 MHz (150 MHz for extended temperature parts) and the CPM ranges between 66–233 MHz.

<sup>3</sup> Input clock frequency is given only for the purpose of reference. User should set MODCK\_H–MODCK\_L so that the resulting configuration does not exceed the frequency rating of the user's part.

## 3.2 PCI Mode

The PCI mode is selected according to three input pins, as shown in Table 12. In addition, note the following:

### NOTE: PCI\_MODCK

In PCI mode only, PCI\_MODCK comes from the LGPL5 pin and MODCK\_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

### NOTE: Tval (Output Hold)

The minimum Tval = 2 when PCI\_MODCK = 1, and the minimum Tval = 1 when PCI\_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

### NOTE

Clock configurations change only after  $\overline{\text{POR}}$  is asserted.

### 3.2.1 PCI Host Mode

The frequencies listed in [Table 15](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

**Table 15. Clock Default Configurations in PCI Host Mode (MODCK\_HI = 0000)**

MODCK[1–3] <sup>1</sup>	Input Clock Frequency (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor <sup>2</sup>	PCI Frequency <sup>2</sup>
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

<sup>1</sup> Assumes MODCK\_HI = 0000.

<sup>2</sup> The frequency depends on the value of PCI\_MODCK. If PCI\_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) Refer to [Table 12](#).

[Table 16](#) describes all possible clock configurations when using the MPC8250's internal PCI bridge in host mode.

**Table 16. Clock Configuration Modes in PCI Host Mode**

MODCK_H – MODCK[1–3]	Input Clock Frequency <sup>1</sup> (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor <sup>2</sup>	PCI Frequency <sup>2</sup>
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	<b>33 MHz</b>	<b>4</b>	<b>133 MHz</b>	<b>5</b>	<b>166 MHz</b>	<b>4/8</b>	<b>33/16 MHz</b>
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000 <sup>3</sup>	33 MHz	5	166 MHz	5	166 MHz	5	<b>33 MHz</b>
0011_001 <sup>3</sup>	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz

Table 16. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1– 3]	Input Clock Frequency <sup>1</sup> (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor <sup>2</sup>	PCI Frequency <sup>2</sup>
0011_010 <sup>3</sup>	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz
0011_011 <sup>3</sup>	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000 <sup>3</sup>	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001 <sup>3</sup>	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010 <sup>3</sup>	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011 <sup>3</sup>	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	<b>66 MHz</b>	<b>2</b>	<b>133 MHz</b>	<b>2.5</b>	<b>166 MHz</b>	<b>2/4</b>	<b>66/33 MHz</b>
0101_001	<b>66 MHz</b>	<b>2</b>	<b>133 MHz</b>	<b>3</b>	<b>200 MHz</b>	<b>2/4</b>	<b>66/33 MHz</b>
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	<b>66 MHz</b>	<b>2.5</b>	<b>166 MHz</b>	<b>2.5</b>	<b>166 MHz</b>	<b>3/6</b>	<b>55/28 MHz</b>
0110_001	<b>66 MHz</b>	<b>2.5</b>	<b>166 MHz</b>	<b>3</b>	<b>200 MHz</b>	<b>3/6</b>	<b>55/28 MHz</b>
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz