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**Freescale Semiconductor**

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# MPC8308 PowerQUICC II Pro Processor Hardware Specification

This document provides an overview of the MPC8308 features and its hardware specifications, including a block diagram showing the major functional components. The MPC8308 is a cost-effective, low-power, highly integrated host processor. The MPC8308 extends the PowerQUICC family, adding higher CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and package size.

**Contents**

# 1 Overview

This figure shows the major functional units within the MPC8308. The e300 core in the MPC8308, with its 16 Kbytes of instruction and 16 Kbytes of data cache, implements the Power Architecture user instruction set architecture and provides hardware and software debugging support. In addition, the MPC8308 offers a PCI Express controller, two three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSEC), a DDR2 SDRAM memory controller, a SerDes block, an enhanced local bus controller (eLBC), an integrated programmable interrupt controller (IPIC), a general purpose DMA controller, two $I^2C$ controllers, dual UART (DUART), GPIOs, USB, general purpose timers, and an SPI controller. The high level of integration in the MPC8308 helps simplify board design and offers significant bandwidth and performance.

This figure shows a block diagram of the device.

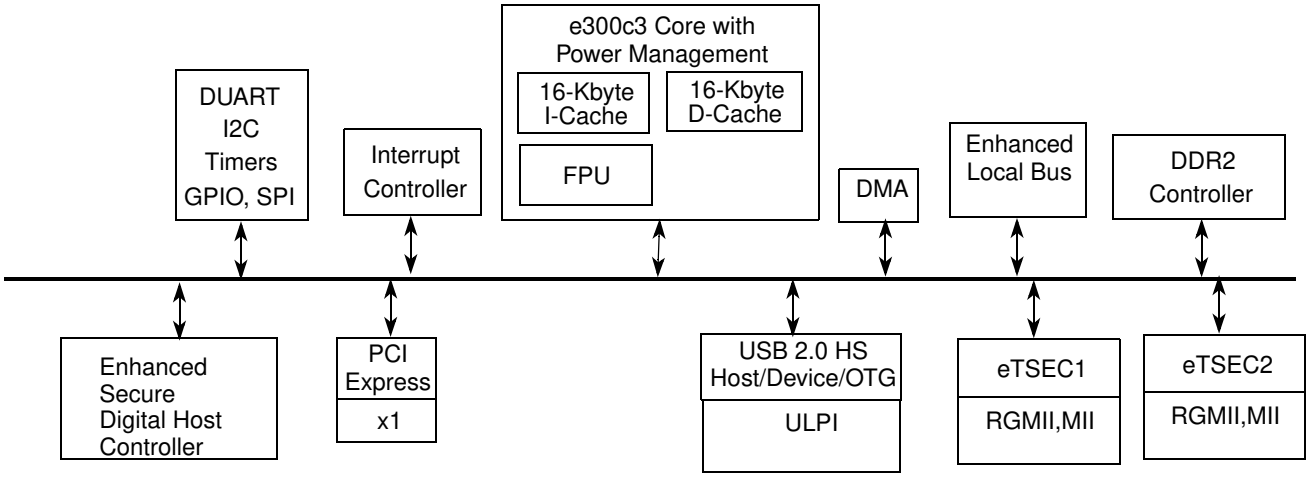


**Figure 1. MPC8308 Block Diagram**

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8308. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

## 2.1.1 Absolute Maximum Ratings

This table lists the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | –0.3 to 1.26 | V | — |
| PLL supply voltage | | $AV_{DD1}$, $AV_{DD2}$ | –0.3 to 1.26 | V | — |
| DDR2 DRAM I/O voltage | | $GV_{DD}$ | –0.3 to 1.9 | V | — |
| Local bus, DUART, system control and power management, eSDHC, $I^2C$, USB, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage | | $NV_{DD}$ | –0.3 to 3.6 | V | 7 |
| SerDes PHY | | $XCOREV_{DD}$, $XPADV_{DD}$, $SDAV_{DD}$ | –0.3 to 1.26 | V | — |
| eTSEC I/O Voltage | | $LV_{DD1}$, $LV_{DD2}$ | –0.3 to 2.75 or –0.3 to 3.6 | V | 6, 8 |
| Input voltage | DDR2 DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | DDR2 DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | eTSEC | $LV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3) | V | 4, 5,8 |
| | Local bus, DUART, system control and power management, eSDHC, $I^2C$, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage | $OV_{IN}$ | –0.3 to ($NV_{DD}$ + 0.3) | V | 3, 5,7 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Notes:**

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $OV_{IN}$ must not exceed $NV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $LV_{IN}$ must not exceed $LV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M, L, O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2
6. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
7. $NV_{DD}$ here refers to $NV_{DDA}$, $NV_{DDB}$,$NV_{DDG}$, $NV_{DDH}$, $NV_{DDJ}$, $NV_{DDP\_K}$ from the ball map.
8. $LV_{DD1}$ here refers to $NV_{DDC}$ and $LV_{DD2}$ refers to $NV_{DDF}$ from the ball map

## 2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

## Table 2. Recommended Operating Conditions

| Characteristic | Symbol | Recommended Value[1] | Unit |
|---|---|---|---|
| SerDes internal digital power | $XCOREV_{DD}$ | 1.0 V ± 50 mV | V |
| SerDes internal digital power | $XCOREV_{SS}$ | 0.0 | V |
| SerDes I/O digital power | $XPADV_{DD}$ | 1.0 V ± 50 mV | V |
| SerDes analog power for PLL | $SDAV_{DD}$ | 1.0 V ± 50 mV | V |
| SerDes analog power for PLL | $SDAV_{SS}$ | 0 | V |
| SerDes I/O digital power | $XPADV_{SS}$ | 0 | V |
| Core supply voltage | $V_{DD}$ | 1.0 V ± 50 mV | V |
| Analog supply for e300 core APLL[2] | $AV_{DD1}$ | 1.0 V ± 50 mV | V |
| Analog supply for system APLL[2] | $AV_{DD2}$ | 1.0 V ± 50 mV | V |
| DDR2 DRAM I/O voltage | $GV_{DD}$ | 1.8 V ± 100 mV | V |
| Differential reference voltage for DDR controller | $MV_{REF}$ | GVDD/2 ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$) | V |
| Standard I/O voltage (Local bus, DUART, system control and power management, eSDHC, USB, $I^2C$, Interrupt, Ethernet management, SPI, Miscellaneous and JTAG I/O voltage)[3] | $NV_{DD}$ | 3.3 V ± 300 mV | V |
| eTSEC IO supply[4,5] | $LV_{DD1}$, $LV_{DD2}$ | 2.5 V ± 125 mV<br>3.3 V ± 300 mV | V |
| Analog and digital ground | $V_{SS}$ | 0.0 | V |
| Operating temperature range[6] | $T_A/T_J$ | Standard = 0 to 105<br>Extended = -40 to 105 | °C |

**Notes:**

1. $GV_{DD}$, $NV_{DD}$, $AV_{DD}$, and $V_{DD}$ must track each other and must vary in the same direction—either in the positive or negative direction.
2. This voltage is the input to the filter discussed in Section 23.2, "PLL Power Supply Filtering," and not necessarily the voltage at the $AV_{DD}$ pin, which may be reduced from $V_{DD}$ by the filter.
3. $NV_{DD}$ here refers to $NV_{DDA}$, $NV_{DDB}$,$NV_{DDG}$, $NV_{DDH}$, $NV_{DDJ}$ and $NV_{DDP\_K}$ from the ball map.
4. The max value of supply voltage should be selected based on the RGMII mode. The lower range applies to RGMII mode.
5. $LV_{DD1}$ here refers to $NV_{DDC}$ and $LV_{DD2}$ refers to $NV_{DDF}$ from the ball map.
6. Minimum temperature is specified with $T_A$; Maximum temperature is specified with $T_J$.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.

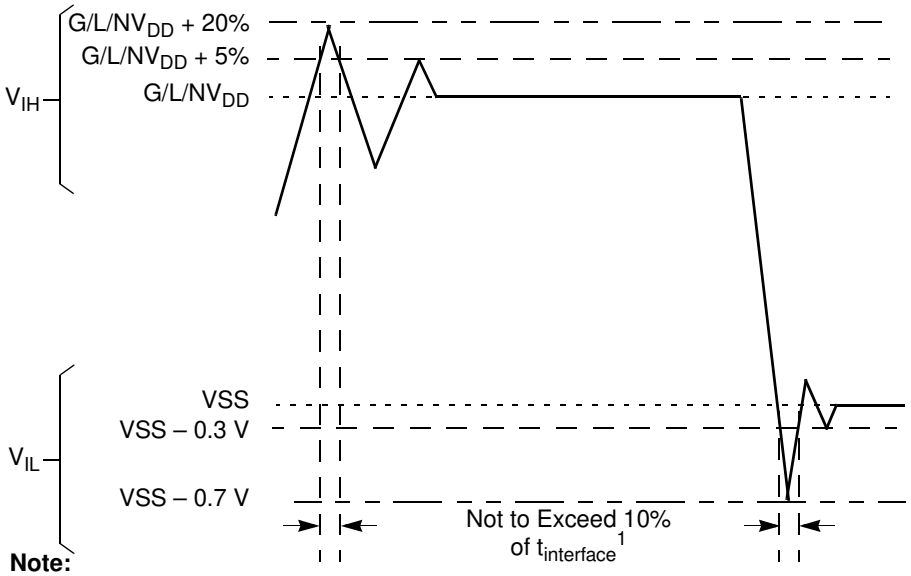


**Figure 2. Overshoot/Undershoot Voltage for GVDD/NVDD/LVDD**

## 2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths.

**Table 3. Output Drive Capability**

| Driver Type | Output Impedance (Ω) | Supply Voltage |
|---|---|---|
| Local bus interface utilities signals | 42 | $NV_{DD}$ = 3.3 V |
| DDR2 signals[1] | 18 | $GV_{DD}$ = 1.8 V |
| DUART, system control, $I^2C$, JTAG, eSDHC, GPIO,SPI, USB | 42 | $NV_{DD}$ = 3.3 V |
| eTSEC signals | 42 | $LV_{DD}$ = 2.5/3.3 V |

[1] Output Impedance can also be adjusted through configurable options in DDR Control Driver Register (DDRCDR). For more information, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

## 2.1.4 Power Sequencing

It is required to apply the core supply voltage ($V_{DD}$) before the I/O supply voltages ($GV_{DD}$, $LV_{DD}$, and $NV_{DD}$) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. The core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3.

If this recommendation is not observed and I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. To overcome side effects of this condition, the application environment may require tuning of external pull-up or pull-down resistors on particular signals to lesser values.

The I/O power supply ramp-up slew rate should be slower than 4V/100 μs, this requirement is for ESD circuit. Note that there is no specific power down sequence requirement for the device. I/O voltage supplies ($GV_{DD}$, $LV_{DD}$, and $NV_{DD}$) do not have any ordering requirements with respect to one another.

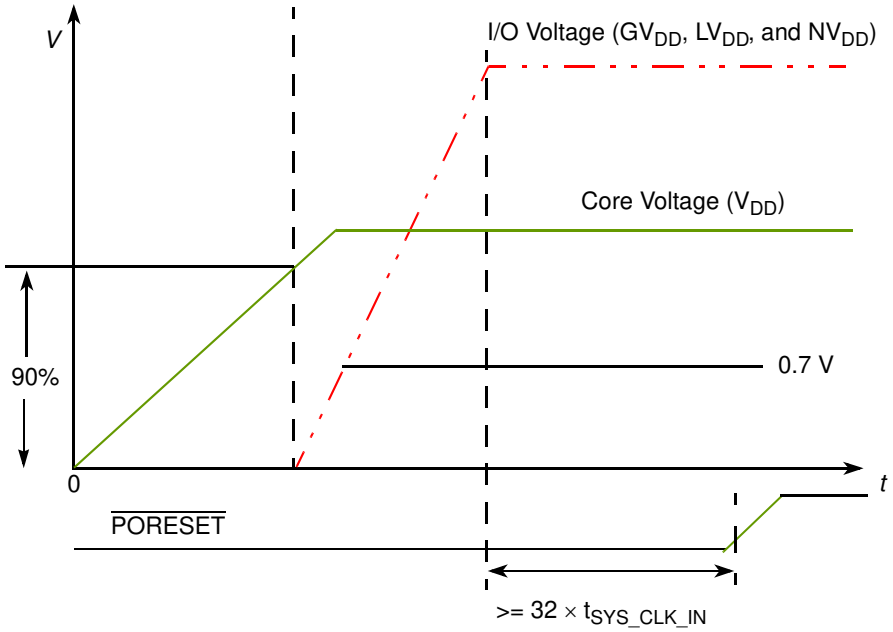


**Figure 3. Power-Up Sequencing Example**

# 3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power for the device is shown in this table. Table 5 shows the estimated typical I/O power dissipation.

**Table 4. MPC8308 Power Dissipation[1]**

| Core Frequency (MHz) | CSB Frequency (MHz) | Typical[2] | Maximum [3] | Unit |
|---|---|---|---|---|
| 266 | 133 | 530 | 900 | mW |
| 333 | 133 | 565 | 950 | mW |
| 400 | 133 | 600 | 1000 | mW |

**Note:**

1 The values do not include I/O supply power but do include core ($V_{DD}$) and PLL ($AV_{DD1}$, $AV_{DD2}$, $XCOREV_{DD}$, $XPADV_{DD}$, and $SDAV_{DD}$)

2 Typical power is based on best process, a voltage of $V_{DD}$ = 1.0 V and ambient temperature of $T_A$ = 25° C and an artificial smoker test.

3 Maximum power is estimated based on best process, a voltage of $V_{DD}$ = 1.05 V, a junction temperature of $T_J$ = 105° C

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

**Table 5. MPC8308 Typical I/O Power Dissipation**

| Interface | Parameter | $GV_{DD}$ (1.8 V) | $NV_{DD}$ (3.3 V) | $LV_{DD}$/ (3.3 V) | $LV_{DD}$ (2.5 V) | Unit | Comments |
|---|---|---|---|---|---|---|---|
| DDR2<br>$R_s$ = 22 Ω<br>$R_t$ = 75 Ω | 250 MHz<br>32 bits+ECC<br>266 MHz<br>32 bits+ECC | 0.302<br><br>0.309 | — | — | — | W | — |
| Local bus I/O load = 20 pF | 62.5 MHz<br>66 MHZ | — | 0.038<br>0.040 | — | — | W | — |
| TSEC I/O load = 20 pF | MII, 25 MHz | — | — | 0.008 | — | W | 2 controllers |
| | RGMII, 125 MHz | — | — | 0.078 | 0.044 | W | |
| eSDHC IO Load = 40 pF | 50 MHz | — | — | 0.008 | — | W | — |
| USB IO Load = 20 pF | 60 MHz | — | — | 0.012 | | W | — |
| Other I/O | — | — | 0.017 | — | — | W | — |

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

## 4.1 DC Electrical Characteristics

This table provides the system clock input (SYS_CLK_IN) DC electrical specifications for the device.

**Table 6. SYS_CLK_IN DC Electrical Characteristics**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 2.4 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | — | $V_{IL}$ | –0.3 | 0.4 | V |
| SYS_CLK_IN input current | 0 V $\le V_{IN} \le NV_{DD}$ | $I_{IN}$ | — | ±10 | μA |

This table provides the RTC clock input (RTC_PIT_CLOCK) DC electrical specifications for the device.

**Table 7. RTC_PIT_CLOCK DC Electrical Characteristics**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 3.3 V – 400 mV | | V |
| Input low voltage | — | $V_{IL}$ | 0 | 0.4 | V |

## 4.2 AC Electrical Characteristics

The primary clock source for the device is SYS_CLK_IN. This table provides the system clock input (SYS_CLK_IN) AC timing specifications for the device.

**Table 8. SYS_CLK_IN AC Timing Specifications**

| Parameter/ | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SYS_CLK_IN frequency | $f_{SYS\_CLK\_IN}$ | 24 | — | 66.67 | MHz | 1, 6 |
| SYS_CLK_IN period | $t_{SYS\_CLK\_IN}$ | 15 | — | 41.67 | ns | — |
| SYS_CLK_IN rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | | 1.2 | ns | 2 |
| SYS_CLK_IN duty cycle | $t_{KHK}/t_{SYS\_CLK\_IN}$ | 40 | — | 60 | % | 3 |
| SYS_CLK_IN jitter | — | — | — | ±150 | ps | 4, 5 |

**Notes:**
1. **Caution:** The system and core must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33 kHz (max rate).

**Table 9. RTC_PIT_CLOCK AC Timing Specifications**

| Parameter/ | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| RTC_PIT_CLOCK frequency | $f_{RTC\_PIT\_CLOCK}$ | 1 | 32768 | — | Hz | — |
| RTC_PIT_CLOCK rise and fall time | $t_{RTCH}$, $t_{RTCL}$ | 1.5 | — | 3 | μs | — |
| RTC_PIT_CLOCK duty cycle | $t_{RTCHK}/t_{RTC\_PIT\_CLOCK}$ | 45 | — | 55 | % | — |

# 5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the device.

## 5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

**Table 10. RESET Pins DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.0 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le NV_{DD}$ | | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

## 5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

**Table 11. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ (input) to activate reset flow | 32 | — | $t_{SYS\_CLK\_IN}$ | 1 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable power and clock applied to SYS_CLK_IN | 32 | — | $t_{SYS\_CLK\_IN}$ | — |
| $\overline{\text{HRESET}}$ assertion (output) | 512 | — | $t_{SYS\_CLK\_IN}$ | 1 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of PORESET | 4 | — | $t_{SYS\_CLK\_IN}$ | — |
| Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$ | 0 | — | ns | — |
| Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$ | — | 4 | ns | 2 |
| Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$ | 1 | — | ns | 1, 2 |

**Notes:**
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN.
2. POR configuration signals consists of CFG_RESET_SOURCE[0:3].

This table provides the PLL lock times.

**Table 12. PLL Lock Times**

| Parameter/Condition | Min | Max | Unit | Note |
|---|---|---|---|---|
| System PLL lock time | — | 100 | μs | — |
| e300 core PLL lock time | — | 100 | μs | — |

# 6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface. Note that DDR2 SDRAM is $GV_{DD}$(typ) = 1.8 V.

## 6.1 DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when $GV_{DD}$(typ) = 1.8 V.

**Table 13. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.7 | 1.9 | V | 1 |
| I/O reference voltage | $MV_{REF}$ | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | $MV_{REF}$ – 0.04 | $MV_{REF}$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.125 | $GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | $MV_{REF}$ – 0.125 | V | — |
| Output leakage current | $I_{OZ}$ | –9.9 | 9.9 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.420 V) | $I_{OH}$ | –13.4 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.280 V) | $I_{OL}$ | 13.4 | — | mA | — |

**Notes:**
1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. $MV_{REF}$ is expected to be equal to 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to $MV_{REF}$. This rail should track variations in the DC level of $MV_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

This table provides the DDR2 capacitance when $GV_{DD}$(typ) = 1.8 V.

**Table 14. DDR2 SDRAM Capacitance for $GV_{DD}$(typ)=1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$ | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$ | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. $GV_{DD}$ = 1.8 V ± 0.090 V, f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for $MV_{REF}$.

**Table 15. Current Draw Characteristics for $MV_{REF}$**

| Parameter / Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Current draw for $MV_{REF}$ | $I_{MVREF}$ | — | 500 | μA | 1 |

**Note:**
1. The voltage regulator for $MV_{REF}$ must be able to supply up to 500 μA current.

## 6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

### 6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ)$=1.8 V.

**Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.8 ± 100 mV

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.45 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.45 | — | V | — |

This table provides input AC timing specifications for the DDR2 SDRAM interface.

**Table 17. DDR2 SDRAM Input AC Timing Specifications**

At recommended operating conditions. with $GV_{DD}$ of 1.8± 100 mV

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Controller skew for MDQS—MDQ/MECC 266 MHz | $t_{CISKEW}$ | –875 | 875 | ps | 1, 2,3 |

**Notes:**
1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ or MECC signal is called $t_{DISKEW}$. This can be determined by the following equation: $t_{DISKEW}$ = +/–(T/4 – abs($t_{CISKEW}$)) where T is the clock period and abs($t_{CISKEW}$) is the absolute value of $t_{CISKEW}$.
3. Memory controller ODT value of 150 Ω is recommended

This figure illustrates the DDR2 input timing diagram showing the $t_{DISKEW}$ timing parameter.

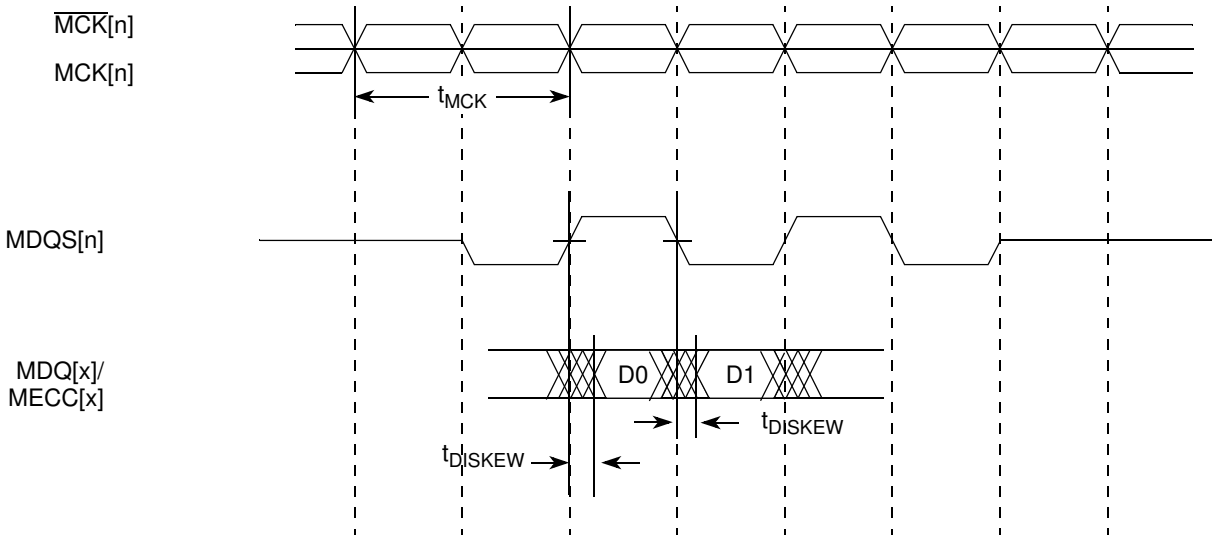


**Figure 4. Timing Diagram for $t_{DISKEW}$**

## 6.2.2 DDR2 SDRAM Output AC Timing Specifications

**Table 18. DDR2 SDRAM Output AC Timing Specifications**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time, MCK[n]/MCK[n] crossing | $t_{MCK}$ | 7.5 | 10 | ns | 2 |
| ADDR/CMD output setup with respect to MCK | $t_{DDKHAS}$ | | — | ns | 3 |
| 266 MHz | | 2.9 | | | |
| ADDR/CMD output hold with respect to MCK | $t_{DDKHAX}$ | | — | ns | 3 |
| 266 MHz | | 2.33 | | | |
| MCS[n] output setup with respect to MCK | $t_{DDKHCS}$ | | — | ns | 3 |
| | | | | | |
| 266 MHz | | 2.5 | | | |
| MCS[n] output hold with respect to MCK | $t_{DDKHCX}$ | | — | ns | 3 |
| 266 MHz | | 3.15 | | | |
| MCK to MDQS Skew | $t_{DDKHMH}$ | –0.6 | 0.6 | ns | 4 |

**Table 18. DDR2 SDRAM Output AC Timing Specifications (continued)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MDQ//MDM/MECC output setup with respect to MDQS | $t_{DDKHDS}$, $t_{DDKLDS}$ | | — | ps | 5 |
| 266 MHz | | 900 | | | |
| MDQ//MDM/MECC output hold with respect to MDQS | $t_{DDKHDX}$, $t_{DDKLDX}$ | | — | ps | 5 |
| 266 MHz | | 1100 | | | |
| MDQS preamble start | $t_{DDKHMP}$ | 0.75 x $t_{MCK}$ | — | ns | 6 |
| MDQS epilogue end | $t_{DDKHME}$ | 0.4 x $t_{MCK}$ | 0.6 x $t_{MCK}$ | ns | 6 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. For a description and understanding of the timing modifications enabled by use of these bits, see the *MPC8308 PowerQUICC II Pro Processor Reference Manual*.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.

This figure shows the DDR2 SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

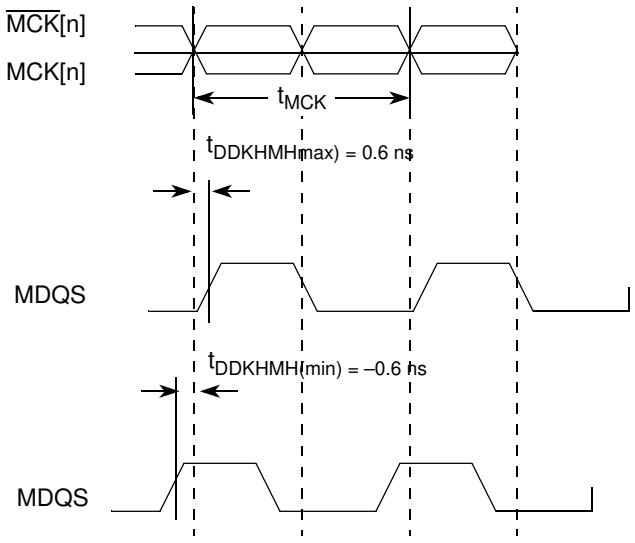


**Figure 5. Timing Diagram for $t_{DDKHMH}$**

This figure shows the DDR2 SDRAM output timing diagram.

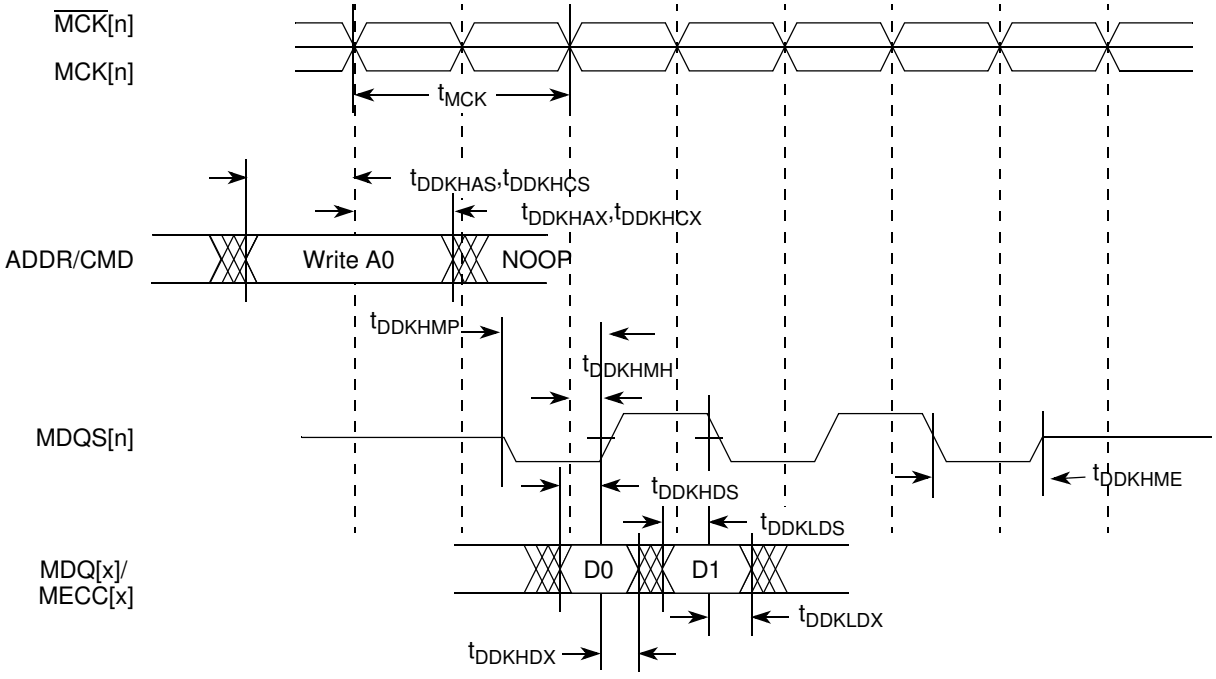


**Figure 6. DDR2 SDRAM Output Timing Diagram**

This figure provides the AC test load for the DDR2 bus.

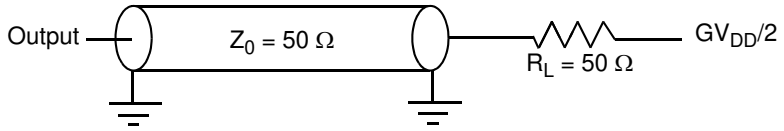


**Figure 7. DDR2 AC Test Load**

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

## 7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

**Table 19. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2.1 | $NV_{DD}$ + 0.3 | V |
| Low-level input voltage NVDD | $V_{IL}$ | –0.3 | 0.8 | V |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $NV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |
| Input current (0 V ≤$V_{IN}$ ≤ $NV_{DD}$) | $I_{IN}$ | — | ± 5 | μA |

## 7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

**Table 20. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | 256 | baud | — |
| Maximum baud rate | > 1,000,000 | baud | 1 |
| Oversample rate | 16 | — | 2 |

**Notes:**
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the $8^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each $16^{th}$ sample.

# 8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management. MPC8308 supports dual Ethernet controllers.

# 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII) and reduced gigabit media independent interface (RGMII), signals except management data input/output (MDIO) and management data clock (MDC). The RGMII interface is defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RGMII interface follows the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

## 8.1.1 eTSEC DC Electrical Characteristics

All MII and RGMII drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The RGMII signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 21. MII DC Electrical Characteristics**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$ | — | | 3.0 | 3.6 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –4.0 mA | $LV_{DD}$ = Min | 2.40 | $LV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 4.0 mA | $LV_{DD}$= Min | VSS | 0.50 | V |
| Input high voltage | $V_{IH}$ | — | — | 2.1 | $LV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | — | –0.3 | 0.90 | V |
| Input high current | $I_{IH}$ | $V_{IN}$ [1] = $LV_{DD}$ | | — | 40 | μA |
| Input low current | $I_{IL}$ | $V_{IN}$ [1] = VSS | | –600 | — | μA |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.

**Table 22. RGMII DC Electrical Characteristics**

| Parameters | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}$ | — | | 2.37 | 2.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $LV_{DD}$ = Min | 2.00 | $LV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $LV_{DD}$= Min | VSS – 0.3 | 0.40 | V |
| Input high voltage | $V_{IH}$ | — | $LV_{DD}$ = Min | 1.7 | $LV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | $LV_{DD}$ = Min | –0.3 | 0.70 | V |
| Input high current | $I_{IH}$ | $V_{IN}$ [1] = $LV_{DD}$ | | — | 15 | μA |
| Input low current | $I_{IL}$ | $V_{IN}$ [1] = VSS | | –15 | — | μA |

**Note:**
1. $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.

## 8.2 MII and RGMII AC Timing Specifications

The AC timing specifications for MII and RGMII are presented in this section.

### 8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

#### 8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

**Table 23. MII Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DDA}/LV_{DDB}/NV_{DD}$ of 3.3 V ± 0.3V.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$ | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | — | 40 | — | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$ | 1 | 5 | 15 | ns |
| TX_CLK data clock rise $V_{IL}$(min) to $V_{IH}$(max) | $t_{MTXR}$ | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall $V_{IH}$(max) to $V_{IL}$(min) | $t_{MTXF}$ | 1.0 | — | 4.0 | ns |

**Note:**
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

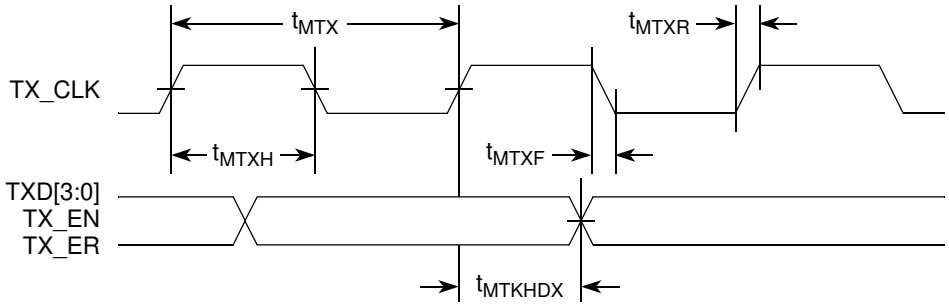


**Figure 8. MII Transmit AC Timing Diagram**

### 8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

**Table 24. MII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ /$NV_{DD}$ of 3.3 V ± 0.3V.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$ | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise $V_{IL}$(min) to $V_{IH}$(max) | $t_{MRXR}$ | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time $V_{IH}$(max) to $V_{IL}$(min) | $t_{MRXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII receive AC timing diagram.

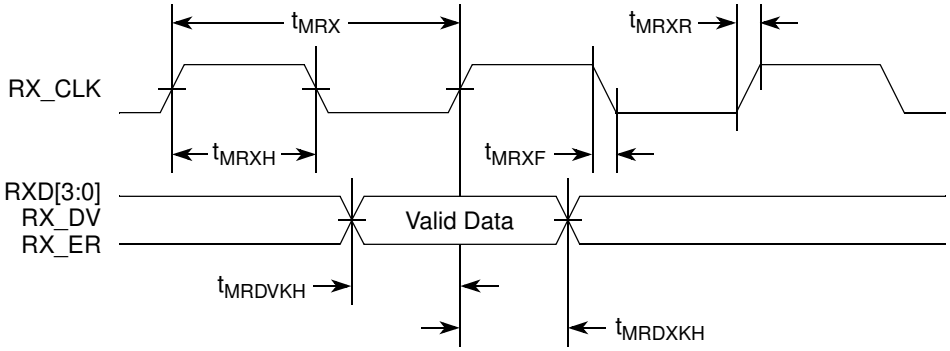


**Figure 9. MII Receive AC Timing Diagram RMII AC Timing Specifications**

This figure provides the AC test load.

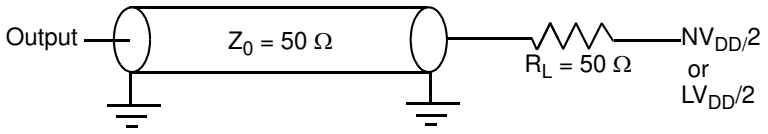


**Figure 10. AC Test Load**

## 8.2.2 RGMII AC Timing Specifications

This table presents the RGMII AC timing specifications.

**Table 25. RGMII AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$ | –0.6 | — | 0.6 | ns |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT}$ | 1.0 | — | 2.6 | ns |
| Clock cycle duration [3] | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 1000Base-T [4, 5] | $t_{RGTH}/t_{RGT}$ | 45 | 50 | 55 | % |
| Duty cycle for 10BASE-T and 100BASE-TX [3, 5] | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns |
| Fall time (20%–80%) | $t_{RGTF}$ | — | — | 0.75 | ns |

**Table 25. RGMII AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}$ of 2.5 V ± 5%.

| | | | | | |
|---|---|---|---|---|---|
| GTX_CLK125 reference clock period | $t_{G12}$ [6] | — | 8.0 | — | ns |
| GTX_CLK125 reference clock duty cycle | $t_{G125H}/t_{G125}$ | 47 | — | 53 | % |

**Notes:**

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of $t_{RGT}$ represents the RGMII receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.
5. Duty cycle reference is $0.5*LV_{DD}$
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.

This figure shows the RGMII AC timing and multiplexing diagrams.

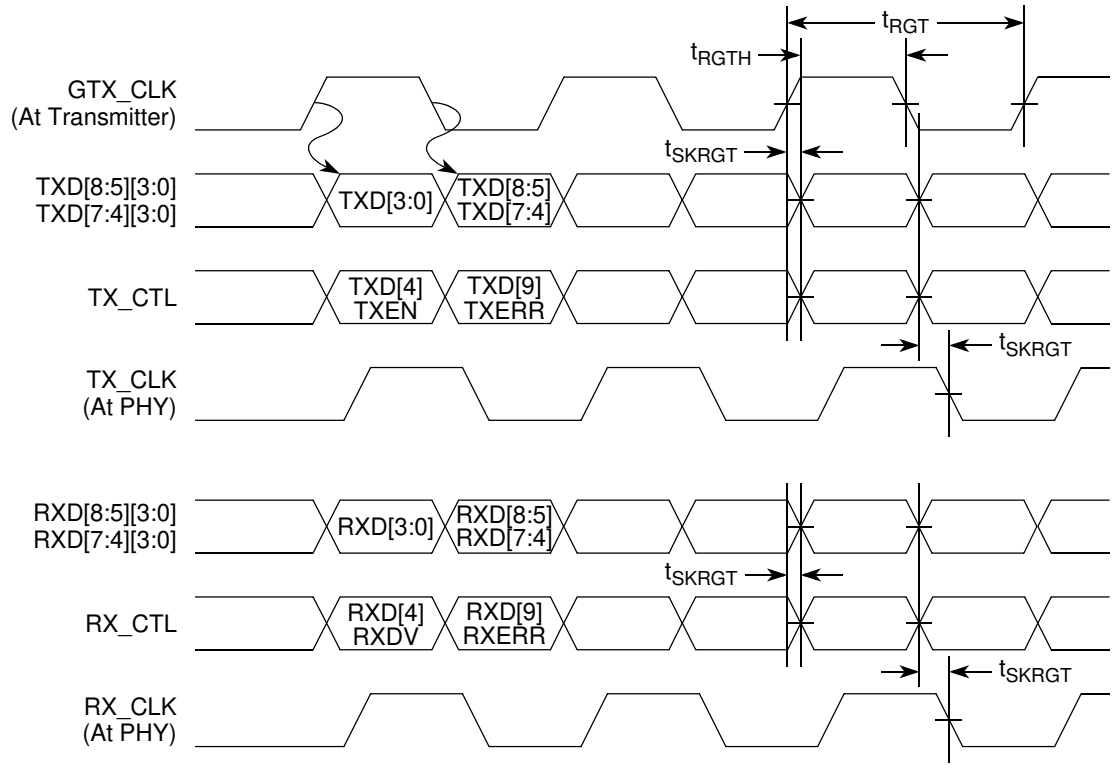


**Figure 11. RGMII AC Timing and Multiplexing Diagrams**

## 8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII

and RGMII are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII Electrical Characteristics."

### 8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. This table provides the DC electrical characteristics for MDIO and MDC.

**Table 26. MII Management DC Electrical Characteristics When Powered at 3.3 V**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (3.3 V) | $NV_{DD}$ | — | | 3.0 | 3.6 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $NV_{DD}$ = Min | 2.10 | $NV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $LV_{DD}$ = Min | VSS | 0.50 | V |
| Input high voltage | $V_{IH}$ | — | | 2.0 | — | V |
| Input low voltage | $V_{IL}$ | — | | — | 0.80 | V |
| Input high current | $I_{IH}$ | $NV_{DD}$ = Max | $V_{IN}$ [1] = 2.1 V | — | 40 | μA |
| Input low current | $I_{IL}$ | $NV_{DD}$ = Max | $V_{IN}$ = 0.5 V | –600 | — | μA |

**Note:**
1. $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.

### 8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

**Table 27. MII Management AC Timing Specifications**

At recommended operating conditions with $LV_{DDA}/LV_{DDB}$ is 3.3 V ± 0.3V

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | — | 2.5 | — | MHz | 2 |
| MDC period | $t_{MDC}$ | — | 400 | — | ns | — |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| MDC to MDIO delay | $t_{MDKHDX}$ | 10 | — | 170 | ns | 3 |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | — |

**Table 27. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DDA}/LV_{DDB}$ is 3.3 V ± 0.3V

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Notes:**

1. The symbols used for timing specifications Follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)
3. This parameter is dependent on the cbs_clk speed (that is, for a csb_clk of 133 MHz, the delay is 60 ns).

This figure shows the MII management AC timing diagram.

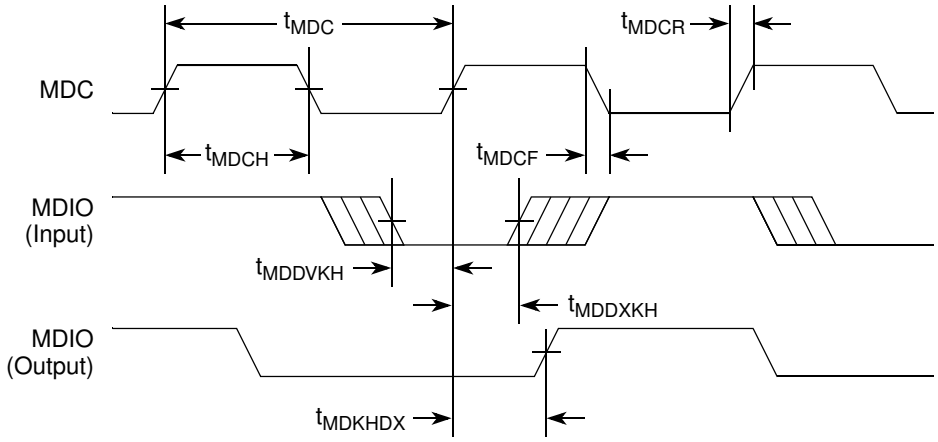


**Figure 12. MII Management Interface Timing Diagram**

## 8.4 IEEE Std 1588™ Timer Specifications

This section describes the DC and AC electrical specifications for the 1588 timer.

### 8.4.1 IEEE 1588 Timer DC Specifications

This table provides the IEEE 1588 timer DC specifications.

**Table 28. GPIO DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |
| Input high voltage | $V_{IH}$ | — | 2.0 | NVDD + 0.3 | V |

**Table 28. GPIO DC Electrical Characteristics (continued)**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le NVDD$ | — | ± 5 | μA |

### 8.4.2 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

**Table 29. IEEE 1588 Timer AC Specifications**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Timer clock cycle time | $t_{TMRCK}$ | 0 | 70 | MHz | 1 |
| Input setup to timer clock | $t_{TMRCKS}$ | — | — | — | 2, 3 |
| Input hold from timer clock | $t_{TMRCKH}$ | — | — | — | 2, 3 |
| Output clock to output valid | $t_{GCLKNV}$ | 0 | 6 | ns | — |
| Timer alarm to output valid | $t_{TMRAL}$ | — | — | — | 2 |

**Note:**
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

# 9 USB

## 9.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB-ULPI interface.

### 9.1.1 USB DC Electrical Characteristics

This table lists the DC electrical characteristics for the USB interface.

**Table 30. USB DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | LVDD + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | LVDD – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $NV_{IN}$ symbol referenced in Table 1 and Table 2.

## 9.1.2 USB AC Electrical Specifications

This table lists the general timing parameters of the USB-ULPI interface.

**Table 31. USB General Timing Parameters**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| USB clock cycle time | $t_{USCK}$ | 15 | — | ns | 1, 2 |
| Input setup to USB clock—all inputs | $t_{USIVKH}$ | 4 | — | ns | 1, 4 |
| Input hold to USB clock—all inputs | $t_{USIXKH}$ | 1 | — | ns | 1, 4 |
| USB clock to output valid—all outputs | $t_{USKHOV}$ | — | 9 | ns | 1 |
| Output hold from USB clock—all outputs | $t_{USKHOX}$ | 1 | — | ns | 1 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{USIXKH}$ symbolizes usb timing (US) for the input (I) to go invalid (X) with respect to the time the usb clock reference (K) goes high (H). Also, $t_{USKHOX}$ symbolizes usb timing (US) for the usb clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from NVDD/2 of the rising edge of USB clock to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

The following two figures provide the AC test load and signals for the USB, respectively.

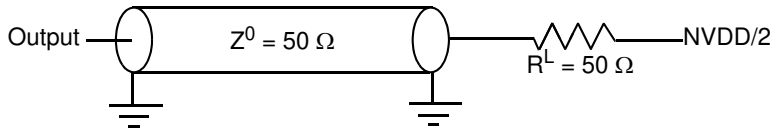


**Figure 13. USB AC Test Load**

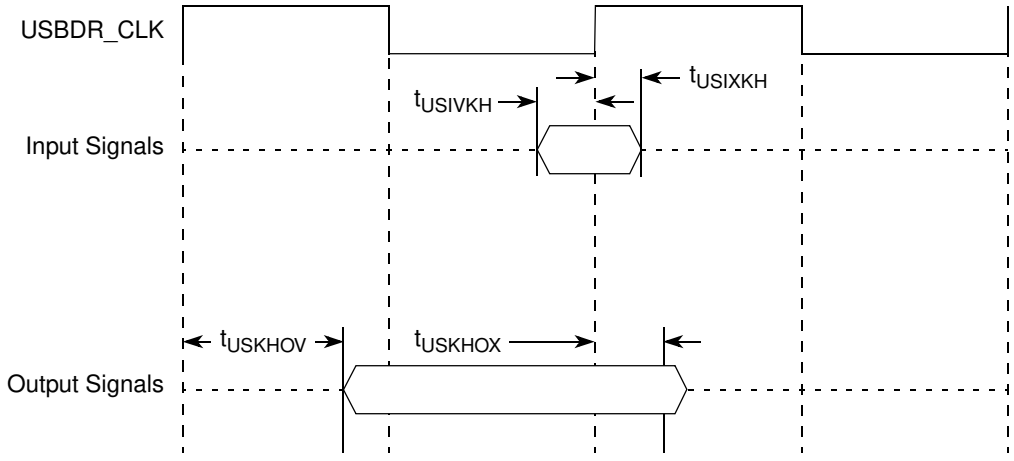


**Figure 14. USB Signals**

# 10 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

## 10.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 15 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TX*n* and $\overline{\text{TX}n}$) or a receiver input (RX*n* and $\overline{\text{RX}n}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- **Single-Ended Swing**

  The transmitter output signals and the receiver input signals TX*n*, $\overline{\text{TX}n}$, RX*n*, and $\overline{\text{RX}n}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's single-ended swing.
- **Differential Output Voltage, $V_{OD}$** (or **Differential Output Swing**)

  The differential output voltage (or swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The $V_{OD}$ value can be either positive or negative.
- **Differential Input Voltage, $V_{ID}$** (or **Differential Input Swing**)

  The differential input voltage (or swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The $V_{ID}$ value can be either positive or negative.
- **Differential Peak Voltage, $V_{DIFFp}$**

  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.
- **Differential Peak-to-Peak, $V_{DIFFp-p}$**

  Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.
- **Differential Waveform**

  The differential waveform is constructed by subtracting the inverting signal (for example, $\overline{\text{TX}n}$) from the non-inverting signal (for example, TX*n*) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 24 as an example for differential waveform.