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Freescale Semiconductor
User's Guide

Document Number: MPC8349EMITXUG
Rev. 2, 10/2006

MPC8349E-mITXE Reference Design Platform User's Guide

The MPC8349E-mITXE reference design platform is a system featuring the powerful PowerQUICC™ II Pro processor, which includes a built-in security accelerator. This low-cost, high-performance system solution consists of a printed circuit board (PCB) assembly known as the MPC8349E-mITXE Board, a hard disk, plus a board support package (BSP), distributed in a CD image. This BSP enables fastest possible time-to-market for development or integration of applications including media servers, network attached storage devices, and next-generation small office home office/small medium business gateways.

Section 1, "MPC8349E-mITXE Board," describes the board in terms of its hardware: the features, specifications, block diagram, connectors, interface specification, and hardware straps.

Section 2, "Getting Started," describes the board settings and physical connections needed to boot the MPC8349E-mITXE board.

Section 3, "MPC8349E-mITXE Software," describes the software that is shipped with the platform.

Use this manual in conjunction with the following documents:

- *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual* (MPC8349ERM)

Contents

WARNING

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

NOTE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

freescale™ semiconductor

- *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications* (MPC8349EEC)
- *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582)
- MC9S08QG8 Data Sheet

1 MPC8349E-mITXE Board

This section presents the features and block diagram, specifications, and mechanical data for the MPC8349E-mITXE board.

1.1 Features

This section presents the features, specification, and block diagram of the MPC8349E-mITXE board. The features are as follows:

- CPU: Freescale MPC8349E running at 533/266 MHz (CPU/CSB (Coherent System Bus))
- Memory subsystem:
  - 256 MByte unbuffered DIMM SDRAM that is expandable to 1 Gbyte
  - 16 MByte Flash memory (two Macronix™ MX29LV640M Flash memory banks or two ESSI EN29LV640 Flash memory banks)
  - Type I Compact Flash connector to interface with the compact Flash storage card in true IDE mode (3.3 mm thick)
- Interfaces:
  - 10/100/1000 BaseT Ethernet ports:
    - TSEC1, GMII interface: one 10/100/1000 BaseT RJ-45 with RJ-45 interface using Vitesse™ VSC8201 single port 10/100/1000 BaseT PHY
    - TSEC 2, GMII interface: five 10/100/1000 BaseT RJ-45 with Vitesse VSC7385 SparX-G5™ 5 + 1 port Gigabit Ethernet integrated PHY switch
  - USB 2.0 host and OTG and hub:
    - USB1, ULPI interface: four USB2.0 type A receptacle connectors, with Genesys Logic™ GL850A 4-PORT USB 2.0 hub controller
    - USB2, ULPI interface: one USB2.0 type mini-AB receptacle connector, with SMSC™ USB3300 Hi-Speed USB host/device/OTG PHY
  - Serial ATA controller:
    - Silicon Image™ SiI3114 PCI to serial ATA controller that connects to a 66 MHz PCI-1
    - Supports four independent serial ATA channels
  - PCI2: 32-bit PCI interface running at up to 66 MHz
    - One 32-bit 3.3 V PCI slot connected to PCI-2
    - One 32-bit 3.3 V miniPCI slot connected to PCI-2
  - ST M24256 Serial EEPROM
  - Dallas™ DS1339 RTC with battery holder

  - Freescale MC9S08QG8 MCU (20 MHz HCS08 CPU) for fan control and soft start
- Board connectors:
  - Expansion connectors: 16-bit local bus expansion connector, 9-bit addressing for external Local Bus Expansion (LEXP) module
  - LCD interface using GPIO
  - 2 × 10 ATX power supply connector
  - RS-232 connectors
    - 1 × 9 pin DB9 receptacle
    - 1 × 10 pin 2.54 mm connector
    - JTAG/COP for debugging
  - Form factor: Mini-ITX form factor (170 mm × 170 mm, or 6692 mils × 6692 mils)
- 6-layer Printed Circuit Board (4-layer signals, 2-layer power and ground)

Figure 1 shows the MPC8349E-mITXE board block diagram.

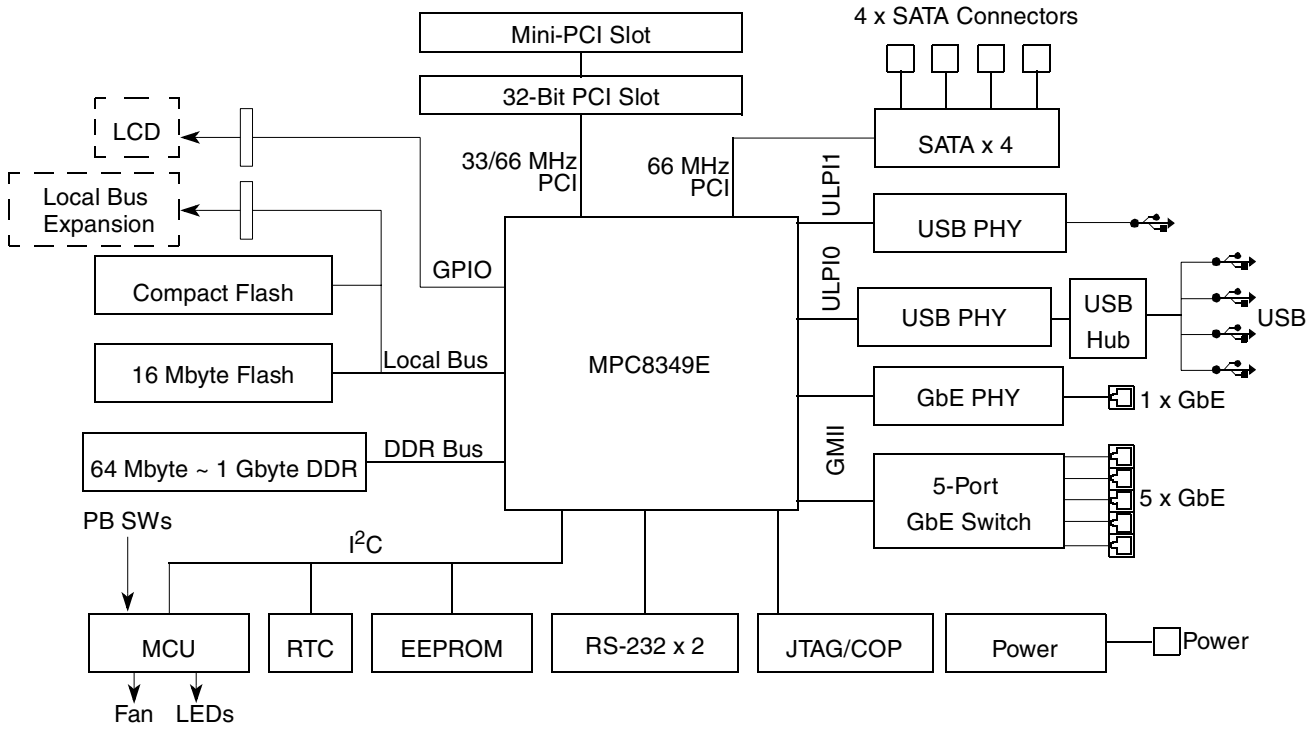

Figure 1. MPC8349E-mITXE Board Block Diagram

1.2 Board-Level Functions

The board-level functions discussed in this section are reset, interrupts, and clock distribution.

1.2.1 Reset and Reset Configurations

The MPC8349E-mITXE reset module generates a single reset to reset the MPC8349E and other peripherals on the board. The reset unit provides power-on reset, hard reset, and soft reset signals in compliance with the MPC8349E hardware specification. Figure 2 shows the reset circuitry.

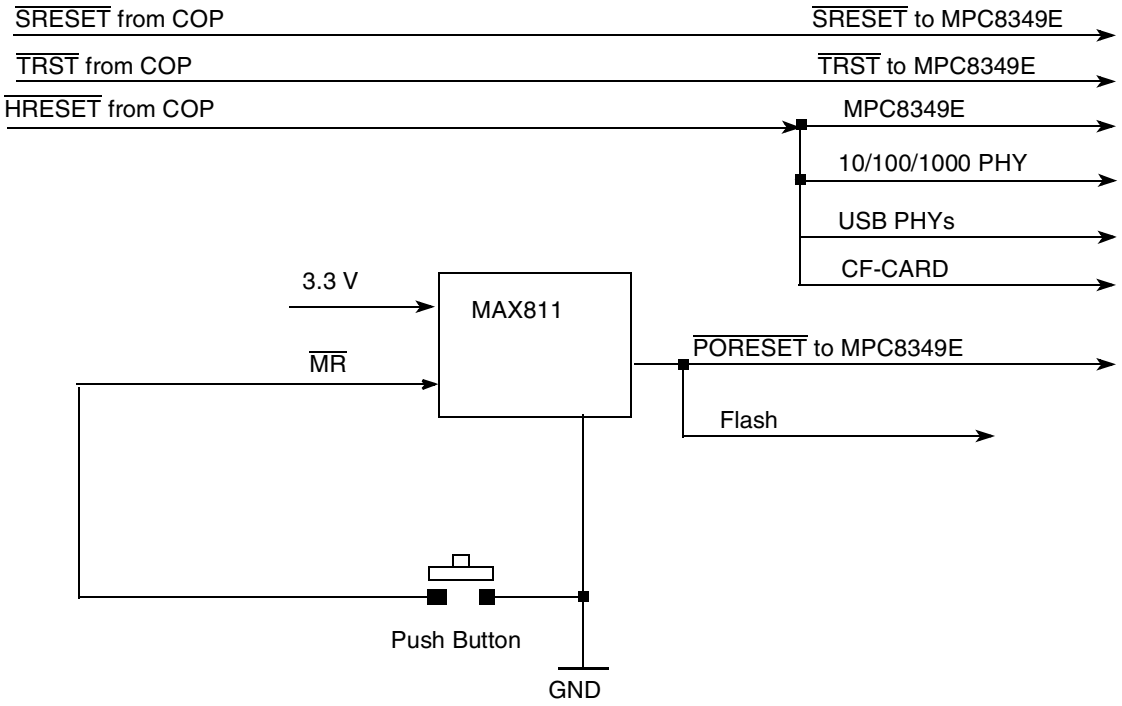

Figure 2. Reset Circuitry of the MPC8349E

- Hard reset is generated either by the COP/JTAG port or the MPC8349E.
- Power-on reset is generated by the Maxim MAX811 device. When $\overline{\text{MR}}$ is deasserted and 3.3 V is ready, the MAX811 internal timeout guarantees a minimum reset active time of 150 ms before $\overline{\text{PORESET}}$ is deasserted. This circuitry guarantees a 150 ms $\overline{\text{PORESET}}$ pulse width after 3.3 V reaches the right voltage level, and this meets the specification of the $\overline{\text{PORESET}}$ input of MPC834x.
- COP/JTAG port reset provides convenient hard-reset capability for a COP/JTAG controller. The $\overline{\text{RESET}}$ line is available at the COP/JTAG port connector. The COP/JTAG controller can directly generate the hard-reset signal by asserting this line low.
- Push button reset interfaces the $\overline{\text{MR}}$ signal with a debounce capability to produce a manual master reset of the processor card.
- Soft reset is generated by the COP/JTAG port. Assertion of $\overline{\text{SRESET}}$ causes the MPC8349E to abort all current internal and external transactions and set most registers to their default values.

1.2.2 External Interrupts

Figure 3 shows the external interrupt circuitry to the MPC8349E.

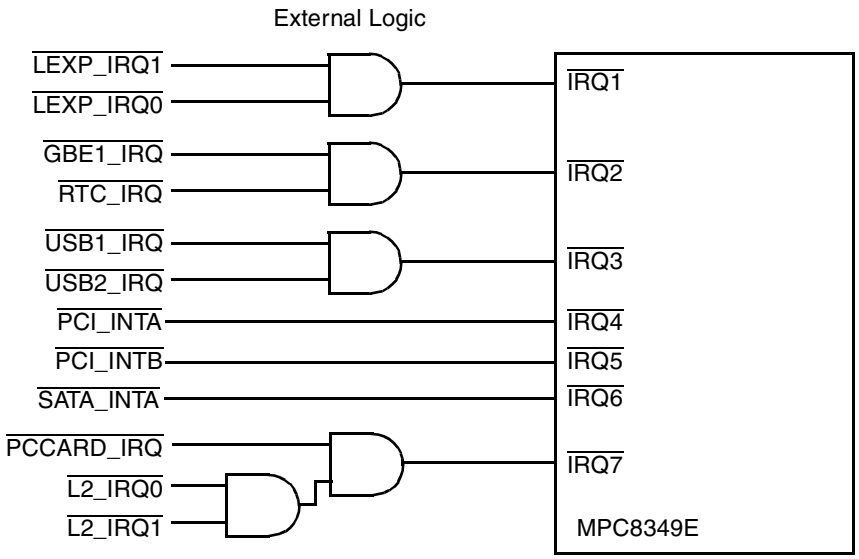

Figure 3. MPC8349E Interrupt Circuitry

Following are descriptions of the interrupt signals shown in Figure 3:

- Local bus connector interrupt ($\overline{\text{LEXP\_IRQ1}}$, $\overline{\text{LEXP\_IRQ0}}$). The local bus expansion connector has two interrupt signals that are ORed on the MPC8349E-mITXE board and generate an interrupt to the MPC8349E $\overline{\text{IRQ1}}$.
- PHY interrupt ($\overline{\text{GBE1\_IRQ}}$) and RTC interrupt ($\overline{\text{RTC\_IRQ}}$).The VSC8201 GBE PHY interrupt is ORed with the DS1339 RTC interrupt and connected to $\overline{\text{IRQ2}}$ of the MPC8349E. Therefore, the system software can detect the status of the Ethernet link, the PHY internal status, and the RTC status.
- PCI interrupt ($\overline{\text{PCI\_INTA}}$, $\overline{\text{PCI\_INTB}}$). The 32-bit PCI slot $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ are connected to the $\overline{\text{IRQ4}}$ and $\overline{\text{IRQ5}}$ of the MPC8349E, respectively, and the MiniPCI $\overline{\text{INTA}}$ is connected to $\overline{\text{IRQ5}}$ of the MPC8349E.
- SATA interrupt ($\overline{\text{SATA\_INTA}}$). The on-board SATA controller (SiI3114) interrupt signal is connected to the $\overline{\text{IRQ6}}$ of the MPC8349E.
- USB over current ($\overline{\text{USB1\_IRQ}}$, $\overline{\text{USB2\_IRQ}}$). The USB1 and USB2 power supplies have an over current detection circuit and generate an interrupt when the current limit reaches (2A) or a thermal shutdown or under voltage lockout (UVLO) condition occurs. These two interrupt pins are ORed to generate an interrupt to $\overline{\text{IRQ3}}$ of the MPC8349E.
- Compact Flash interrupt ($\overline{\text{PCCARD\_IRQ}}$) and L2 Switch (VSC7385) interrupt ($\overline{\text{L2\_IRQ1}}$, $\overline{\text{L2\_IRQ0}}$). The L2 Switch (VSC7385) has two IRQs that are ORed with the compact Flash interrupt signal and generate an interrupt to the MPC8349E via the $\overline{\text{IRQ7}}$ signal.

1.2.3 Clock Distribution

Figure 4 and Table 1 show the clock distribution on the MPC8349E-mITXE board.

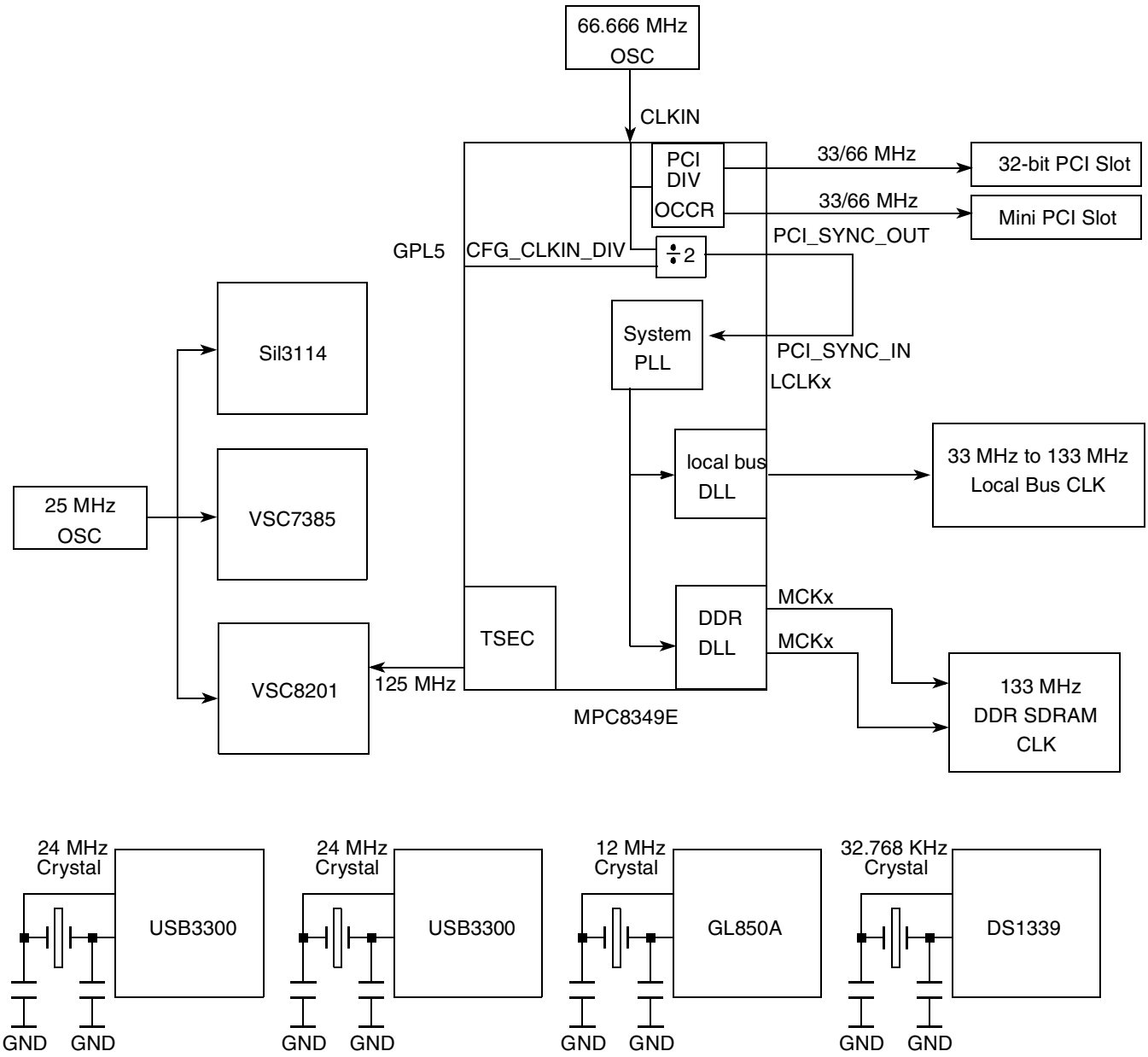

Figure 4. MPC8349E-mITXE Clock Scheme

Table 1. Clock Distribution

Clock Frequency	Module	Generated by	Description
66.666 MHz	MPC8349E CLKIN	66.666 MHz oscillator	The MPC834x uses CLKIN to generate the PCI_SYNC_OUT clock signal, which is fed back on the board through the PCI_SYNC_IN signal to the internal system PLL. From the power-on reset configuration, the CSB clock is generated by the internal PLL and is fed to the e300 core PLL for generating the e300 core clock. The GPL5 (CFG_CLKIN_DIV) configuration input selects whether CLKIN or CLKIN/2 is driven on the PCI_SYNC_OUT signal. The GPL5 is tied to jumper J22.D.
125 MHz	MPC8349E TSEC	VSC8201	For TSEC operation, a 125 MHz clock is provided by the gigabit Ethernet PHY (VSC8201) on the board.
133/166 MHz	DDR SDRAM	MPC8349E	The DDR memory controller is configured to use the 1:1 mode CSB to DDR clock for the DDR interface. The local bus clock uses CCB/n clock, where n is configured from the LCRR register.
25 MHz	SATA Controller (SiI3114) GBE PHY (VSC8201) GBE L2 Switch (VSC7385)	125 MHz oscillator	The 25 MHz oscillator generates the clock for the SiI3114, VSC7385, and VSC8201
33/66 MHz	PCI 32-bit slot and MiniPCI slot	MPC8349E	The PCI module uses the PCI_SYNC_IN as its clock source. The trace of the PCI_SYNC_IN/ PCI_SYNC_OUT signal is synchronized with all the PCI signals of the PCI slots. The trace length of the PCI_SYNC_IN/PCI_SYNC_OUT clock is 2.5 inches from the pin of the PowerQUICC II Pro device to the PCI sockets.
24 MHz	USB PHY1 and PHY2 (USB3300)	24 MHz crystal	
12 MHz	USB HUB (GL850A)	12 MHz crystal	
32.768 KHz	RTC (DS1339)	32.768 KHz crystal	

1.2.4 DDR SDRAM Controller

MPC8349E uses DDR SDRAM as the system memory. The DDR interface uses the SSTL2 driver/receiver and 2.5 V power. A Vref 2.5V/2 is needed for all SSTL2 receivers in the DDR interface. For details on DDR timing design and termination, refer to the Freescale application note entitled *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582). The termination scheme uses one series resistor (R_S) from the MPC8349E to the memory and one termination resistor (R_T) attached to the termination rail (V_{TT}). This approach is used in commodity PC motherboard designs.

The MPC8349E reads the DIMM SPD data using the DIMM SCL (clock) and the SDA (data) signals through the I2C2 interface. Figure 5 shows the DDR SDRAM controller connection.

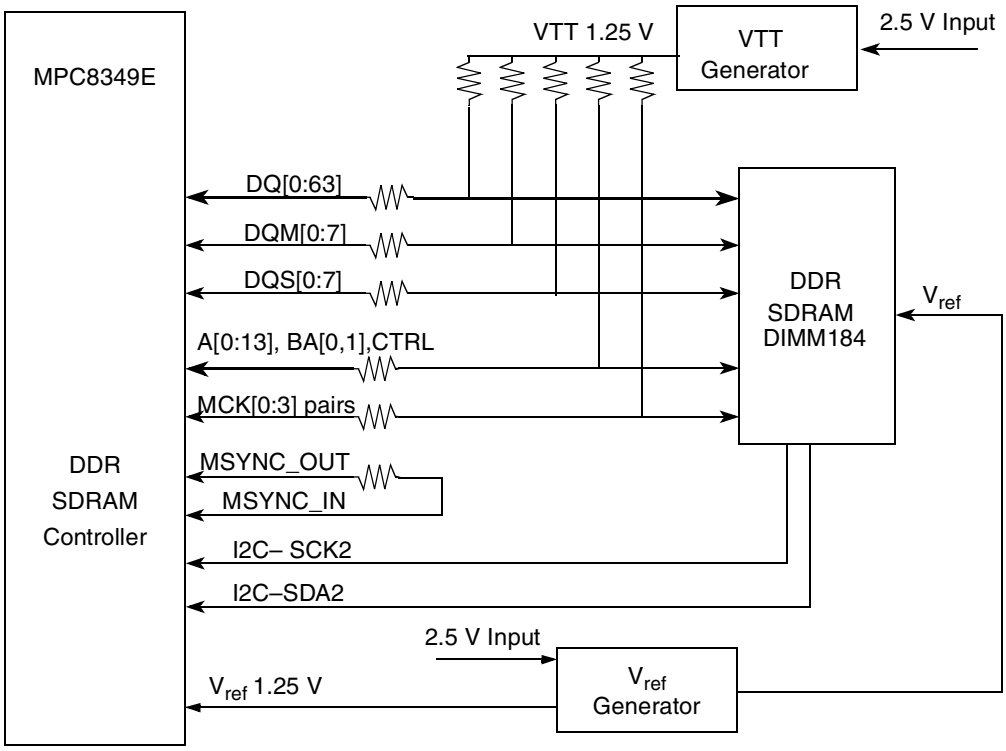

Figure 5. DDR SDRAM Connection

1.2.5 Local Bus Controller

The MPC8349E local bus controller has a 32-bit LAD[0–31] address that consists of data multiplex bus and control signals. The local bus speed is up to 133 MHz. To interface with the standard memory device, an address latch must provide the address signals. The LALE is used as the latching signal. To reduce the load of the high speed 32-bit local bus interface, there is a data buffer for all low-speed devices attached to the memory controller. The followings modules are connected to the local bus:

- On-board single bank 2/4/8/16 Mbyte Flash memory
- Compact Flash interface
- GBE L2 switch (VSC7385) parallel interface (PI)
- Expansion connector for the 32-bit local bus interface

Figure 6 shows the block diagram and connections for the local bus.

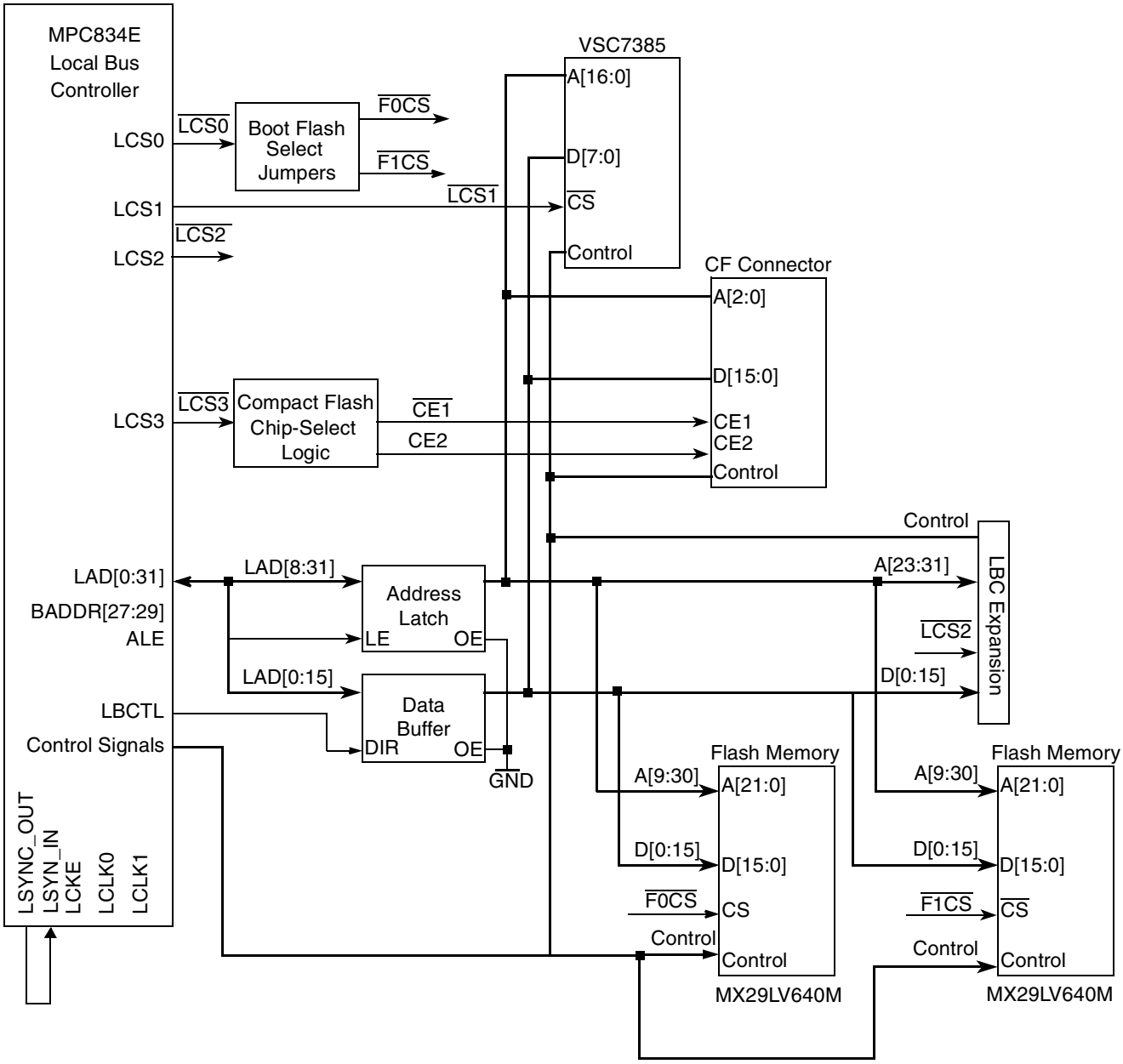

Figure 6. Local Bus Connections

1.2.6 On-Board Flash Memory

Through the general-purpose chip-select machine (GPCM), the MPC8349E-mITXE provides a total of 2/4/8/16 Mbyte of 90 ns Flash memory using one chip-select signal. The Flash memory is used with the 16-bit port size. As Table 2 shows, either of the two Flash memory devices can be selected as the boot Flash.

Table 2. Boot Flash Selection

J22.E	BOOT1	Boot Flash	Backup Flash
Jumper Off	1	U4	U7
Jumper On	0	U7	U4

A boot Flash selector jumper allows the user to select between two different boot images in each bank of Flash memory.

Table 3. Flash Memory Map

	16 Mbyte MX29LV640M (2 × 8 Mbyte)
Boot Flash	0xFE80_0000 to 0xFEFF_FFFF
Backup Flash	0xFE00_0000 to 0xFE7F_FFFF

1.2.7 I²C

The MPC8349E has two I²C interfaces. On the MPC8349E-mITXE board, the MPC8349E acts as I²C master for both I²C buses (I2C1 and I2C2). I2C1 is connected to the M24256 serial EEPROM, and I2C2 is connected to the DDR DIMM module SPD (serial presence detect) EEPROM, the two PCF8574 I²C expanders, the DS1339 RTC (real time clock) and the I²C interface of the MC9S08QG8.

The M24256 serial EEPROM can be used to store the reset configuration word of the MPC8349E, as well as storing the configuration registers values if boot sequencer of MPC8349E is enabled. If user wants to load the reset configuration word from the I2C1 M24256 EEPROM, the jumper J22 should be set to ABCDEFGH=01011110, with 1=jumper removed and 0=jumper installed. For more details on how to program the reset configuration word value in I²C EEPROM and the boot sequencer mode, please refer to the MPC8349ERM. The I²C address of the M24256 EEPROM on I2C1 bus is 0x50.

The DDR SPD EEPROM is connected to the I2C2 of MPC8349E. The bootload program optionally reads the SPD EEPROM data to determine the DDR DIMM physical structure (e.g. number of rows and columns), the DDR timings (e.g. CAS latency, re-fresh timing), and setup the configuration registers of the MPC8349E DDR memory controller. The I²C address of the DDR SPD EEPROM on I2C2 bus is 0x51.

There are two PCF8574A I²C I/O expander on the MPC8349E-mITXE board to provide general purpose I/O expansion via the I2C2 interface. The first PCF8574A (U8) has I2C2 address 0x38 and it is able to control the Green LED (D1) and Yellow LED (D2), set the VSC8201 to powerdown mode, set the logic level of PCI_PME signal of the miniPCI card, and enable the LCD interface of the MPC8349E-mITXE board. The bit definition of this PCF8574A (U8) is defined as in Table 4.

Table 4. PCF8574A (U8) Bit Descriptions

PCF8574A (U8) Bit[0..7]	Name	Read/Write	Description
0	LED0	Write only, read returns 1	LED0 control 0: LED is on 1: LED is off
1	LED1	Write only, read returns 1	LED1 control 0: LED is on 1: LED is off
2	VSC8201_PWN	Write only, read returns 1	VSC8201 power down control 0: VSC8201 PHY is powerdown 1: VSC8201 PHY in normal mode
3	MPCI_PME	Write only, read returns 1	Output from the miniPCI card to indicate power management event 0: power management event has occurred 1: power management event has not occurred
4	LCD_EN	Write only, read returns 1	Enable/disable the LCD interface 0: LCD interface is enabled 1: LCD interface is disabled
5	Not used	—	—
6	Not used	—	—
7	Not used	—	—

The second PCF8574A (U10) has I2C2 address 0x39 and it is able to detect the board revision number, the compact Flash presence (card detect), the miniPCI clock run signal level, the PCI (slot and miniPCI) M66EN signal level and detect which Flash is currently used to boot. The bit definition of this PCF8574A (U10) is defined as in Table 5.

Table 5. PCF8574A (U10) Bit Descriptions

PCF8574A (U10) bit[0..7]	Name	Read/Write	Description
0	REV1	Read only, write has no effect	Board revision number REV[0:1] definition 00: revision 0.0 01: revision 0.1 10: revision 1.0 11: reserved
1	REV0		
2	Reserved	Read only, write has no effect	Reserved for future use
3	CF_CD	Read only, write has no effect	Compact Flash Card Detect 0: Compact Flash is installed 1: Compact Flash is removed

Table 5. PCF8574A (U10) Bit Descriptions (continued)

PCF8574A (U10) bit[0..7]	Name	Read/Write	Description
4	MPCI_CLKRUN	Read/Write	MiniPCI clock run signal level, defined by the PCI Mobile Design Guide. 0: MiniPCI clock is in normal operating frequency 1: MiniPCI clock is stopped or running very low
5	PCI_M66EN	Read only, write has no effect	PCI M66EN Signal 0: PCI M66EN signal is low, indicates the PCI cards on PCI slot and miniPCI slot are not 66 MHz capable 1: PCI M66EN signal is high, indicates the PCI cards on PCI slot and miniPCI slot are 66 MHz capable
6	BOOT0	Read only, write has no effect	Used to determine which Flash is used for boot Flash 0: Flash 0 (U4) is the boot Flash 1: Flash 1 (U7) is the boot Flash
7	Not used	—	—

The DS1339 RTC is connected to I^2C with address 0x68. The software running on PowerPC core can read or write to the RTC through the I2C2 interface.

1.2.8 Compact Flash Interface

A compact Flash interface connects directly to the local bus without a PCMCIA controller. The true IDE mode is the only compact Flash operating mode supported by this connection. Hot insertion and removal is not supported. The MPC8349E universal programmable machine A (UPMA) is used to generate the required timing for $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ through the LGPL0 and LGPL1 signals.

The true IDE mode requires three address signals (A[0:2]) and two chip-enable signals ($\overline{\text{CE}}$[1:2]) to address the 10 registers in the AT task file. Therefore, glue logic is used to split $\overline{\text{CS3}}$ into two regions. One chip-select signal ($\overline{\text{CS3}}$) is assigned to the compact Flash interface. Glue logic is used to generate the $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ signals required by the compact Flash. The logic simply uses the local bus address A22 to determine which chip-enable signal is generated. See Figure 7.

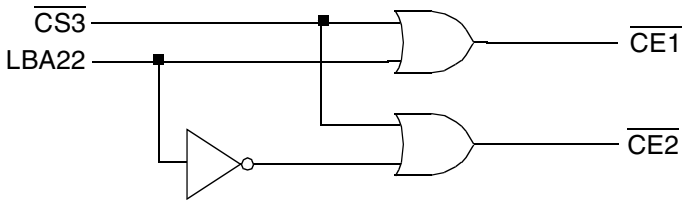

Figure 7. $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ Generation Logic

The AT task file and the corresponding address/chip-enable signal level are shown in Table 6.

Table 6. AT Task File

CE2	CE1	Compact Flash Address	Read(IORD=L)	Write(IOWR=L)	Local Bus Address
1	0	0h	Data register (16 bits)	Data register (16 bits)	0x*nnnn_n*000
1	0	1h	Error register	Feature register	0x*nnnn_n*001
1	0	2h	Sector count register	Sector count register	0x*nnnn_n*002
1	0	3h	Sector number register	Sector number register	0x*nnnn_n*003
1	0	4h	Cylinder low register	Cylinder low register	0x*nnnn_n*004
1	0	5h	Cylinder high register	Cylinder high register	0x*nnnn_n*005
1	0	6h	Drive head register	Drive head register	0x*nnnn_n*006
1	0	7h	Status register	Command register	0x*nnnn_n*007
0	1	6h	Alternate status register	Device control register	0x*nnnn_n*106
0	1	7h	Drive address register	Reserved	0x*nnnn_n*107

Figure 8 shows the UPM timing diagram for LGPL0 ($\overline{\text{IORD}}$) and LGPL1($\overline{\text{IOWR}}$). The UPM table of these two signals is listed in Table 7.

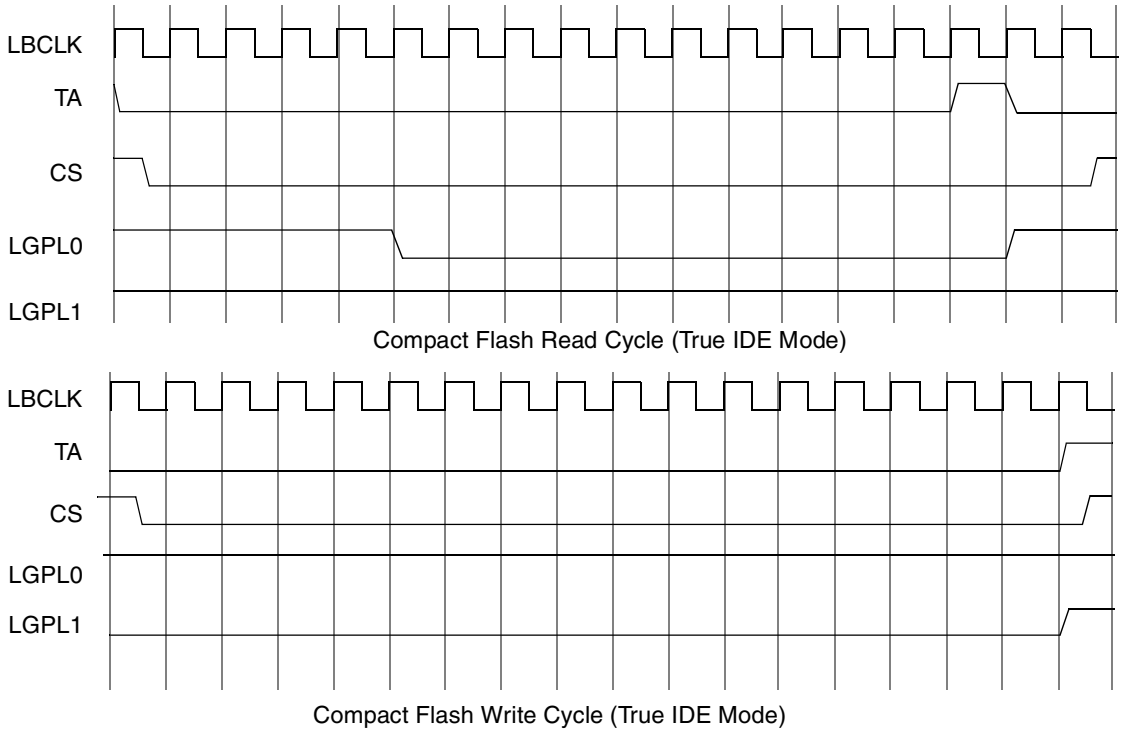

Figure 8. Read/Write UPM Timing of Compact Flash

The UPM RAM words of compact Flash read/write are shown in Table 7.

Table 7. UPM RAM Word for Compact Flash Read/Write

Read			Write		
Address	Address (Hexadecimal)	RAM Word	Address	Address (Hexadecimal)	RAM Word
0	0x00	0xCFFF_FC00	24	0x18	0xCFFF_FC00
1	0x01	0x0FFF_FF00	25	0x19	0x0FFF_FF00
2	0x02	0x0FAF_FF00	26	0x1A	0x0FF3_FF00
3	0x03	0x0FAF_FF00	27	0x1B	0x0FF3_FF00
4	0x04	0x0FAF_FD00	28	0x1C	0x0FF3_FE00
5	0x05	0x0FAF_FC04	29	0x1D	0x0FFF_FC00
6	0x06	0x0FFF_FC00	30	0x1E	0x3FFF_FC05
7	0x07	0x3FFF_FC01			

1.2.9 GBE L2 Switch (VSC7385) Parallel Interface

The Gigabit Ethernet L2 switch (VSC7385) parallel interface, connected to the local bus of the MPC8349E, gives the MPC8349E the ability to load program into the internal instruction memory of the switch at boot up, and to allow access of the internal registers of the L2 switch by the MPC8349E. The MPC8349E general-purpose chip-select machine (GPCM) generates the timing of read/write accesses. Read/write accesses to the VSC7385 are terminated by the $\overline{\text{DONE}}$ signal, which is connected to the $\overline{\text{LGTA}}$ of the GPCM and generates the internal $\overline{\text{TA}}$ for the PowerPC™ core. Figure 9 shows the connection between the VSC7385 and the MPC8349E.

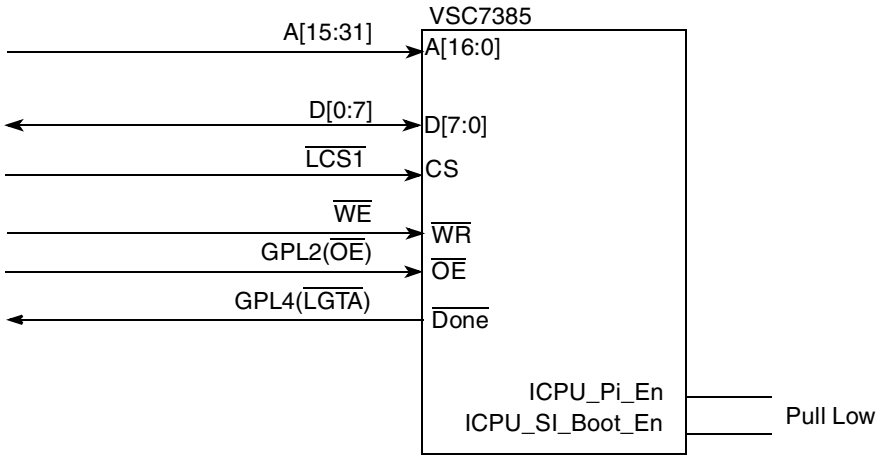

Figure 9. Parallel Interface of VSC7385

1.2.10 Local Bus Expansion Connector

The local bus expansion connector (J2) provides the signals listed in Table 8 to interface external devices.

Table 8. Local Bus Expansion Connector (J2) Pin Assignment

Pin	Signal	Pin	Signal
1	LBD15	2	WE
3	LBD14	4	LWE0
5	LBD13	6	LEXP_IRQ1
7	LBD12	8	LEXP_IRQ0
9	LBD11	10	LWE1
11	LBD10	12	3.3V
13	LBD9	14	3.3V
15	LBD8	16	3.3V
17	LBD7	18	3.3V
19	LBD6	20	GPIO0
21	LBD5	22	GPIO1
23	LBD4	24	GPIO2
25	LBD3	26	GPIO3
27	LBD2	28	GPIO4
29	LBD1	30	GPIO5
31	LBD0	32	CS2
33	LBA31	34	CS2
35	LBA30	36	GND
37	LBA29	38	GND
39	LBA28	40	GND
41	LBA27	42	GND
43	LBA26	44	SPISEL
45	LBA25	46	SPICLK
47	LBA24	48	SPIMISO
49	LBA23	50	SPIMOSI

1.2.11 SATA Controller

A SATA controller device for storage applications, SiI3114, is attached to the PCI1 interface with IDSEL = AD16. There are four SATA channels, as shown in Figure 10. The SiI3114 requires a 25 MHz input clock, which is provided by the a 25 MHz oscillator. It requires 3.3 V and 1.8 V supply voltages.

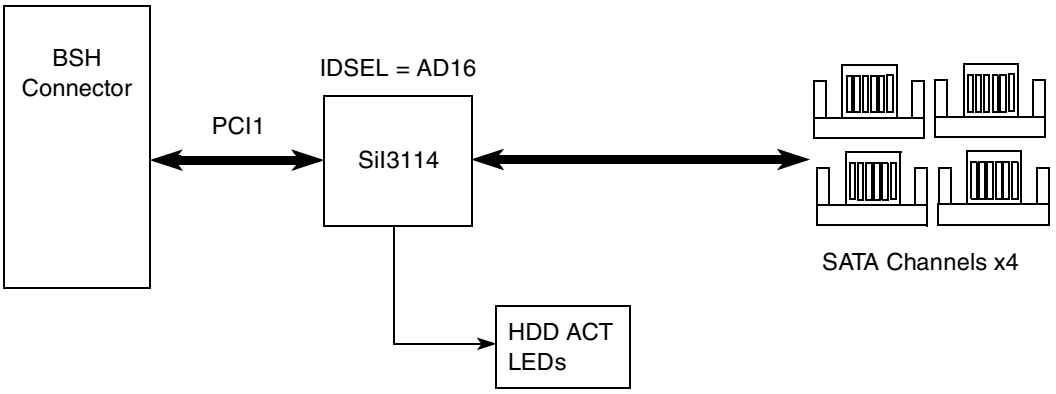

Figure 10. Sil3114 Connections

1.2.12 10/100/1000 BaseT Interface

On the MPC8349E-mITXE board, GMII mode is used on TSEC1 and TSEC2, which are connected to the on-board 10/100/1000 PHY (VSC8201) and the 5-port GBE switch (VSC7385), respectively. The TSEC I/O voltage is set to 3.3 V. The GMII (1000 BaseT) is a source synchronous bus. For a transmit bus connection, it is synchronous to GTX_CLK from the TSEC module. The receive bus connection is synchronous to RX_CLK generated from the PHY device. When the speed is 10/100 BaseT (MII), both transmit and receive clocks are generated by the VSC8201 PHY device. The VSC7385 GMII interface cannot be downgraded to MII mode, so only GMII (1000BaseT) mode is supported as the interface to the MPC8349E. The MPC8349E MII management interface is connected to the VSC8201 only. Figure 11 shows the connection between the MPC8349E TSEC1 to the VSC8201 and TSEC2 to the VSC7385.

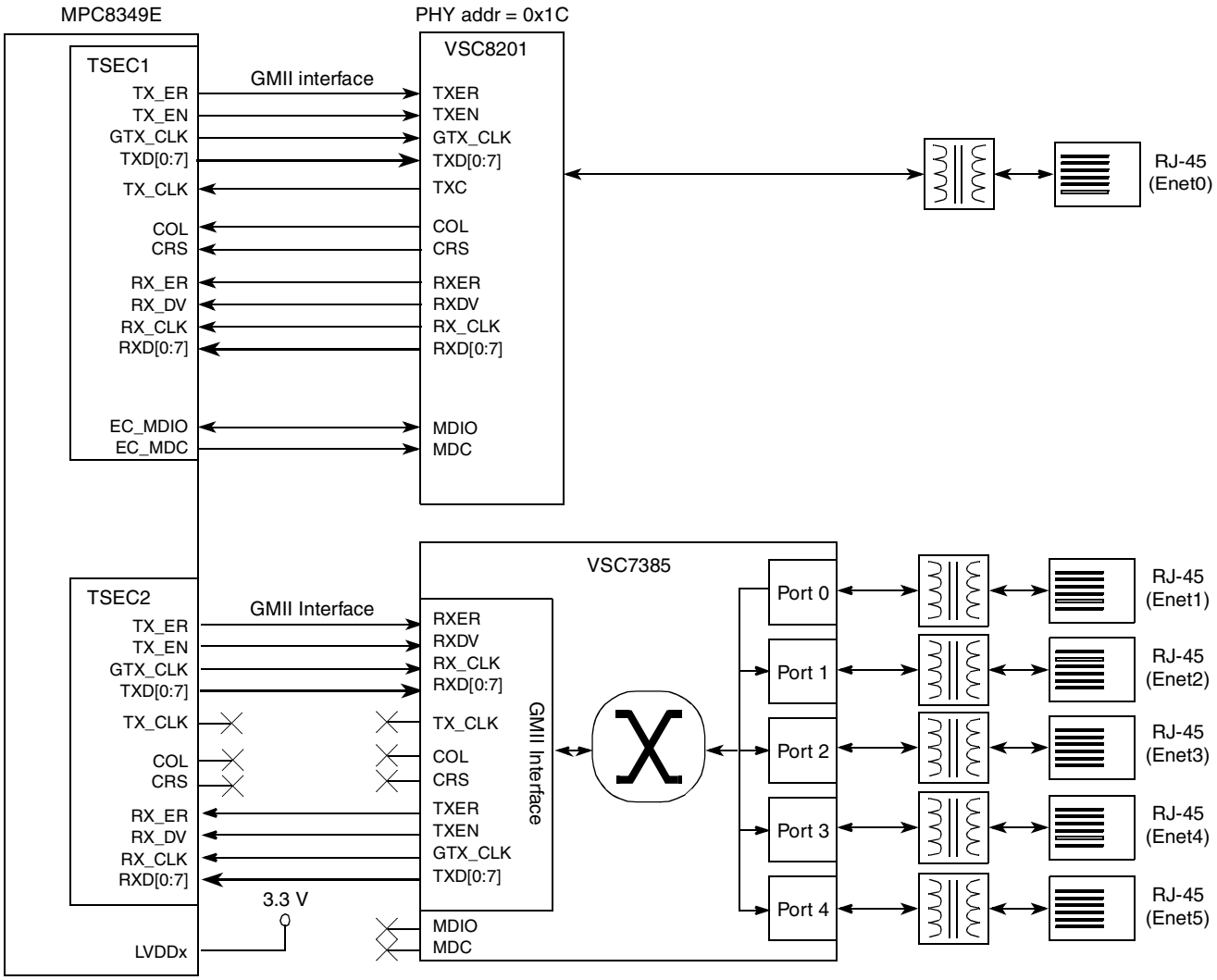

Figure 11. GMII Interface Connection for 10/100/1000 BaseT Ethernet

1.2.13 RS-232 Port

Figure 12 illustrates the serial port connection using a MAX3232 3.3 V RS-232 driver to interface with a 9-pin D type female connector. This serial connection runs at up to 115.2 Kbps.

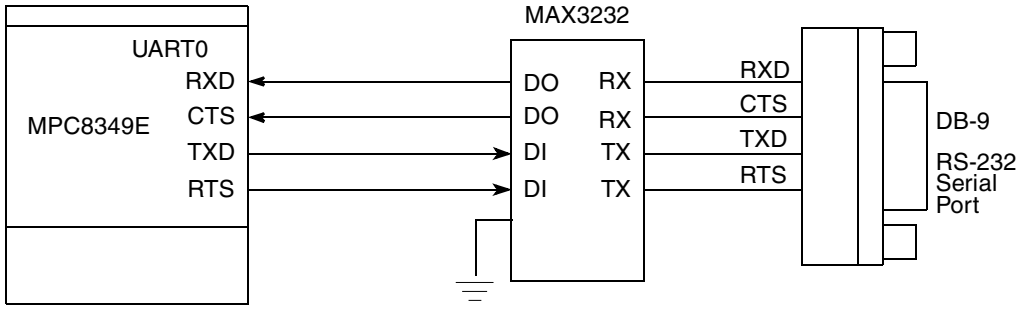

Figure 12. UART Debug Port Connection

1.2.14 USB 2.0 Interface

The MPC8349E has two internal USB modules (USB0 and USB1), a multi-port host (MPH) module, and a dual-role (DR) module. On the MPC8349E-mITXE board, both USB0 and USB1 connect to USB PHY (USB3300) through the 8-bit UTMI low pin count interface (ULPI). For USB0, the USB3300 PHY connects to an on-board USB2.0 hub controller (GL850A) to expand the USB interfaces to four USB2.0 host ports. For USB1, the USB3300 PHY connects to a USB Mini-AB type receptacle connector that serves as a host/device/OTG USB interface. Table 9 shows the USB0 and USB1 configuration. Note that OTG software support is subject to Linux kernel support.

Table 9. USB Port 0 and Port 1 Configurations

Port	Interface Type	USB PHY	Operating Mode	USB Hub	Connector Type
USB Port 0	ULPI	USB3300	MPH Host	GL850A	4 x Type B Receptacle
USB Port 1	ULPI	USB3300	DR Host/Device/OTG	Nil	1 x Type Mini-AB Receptacle

Figure 13 shows the connection of USB port 0 and port 1.

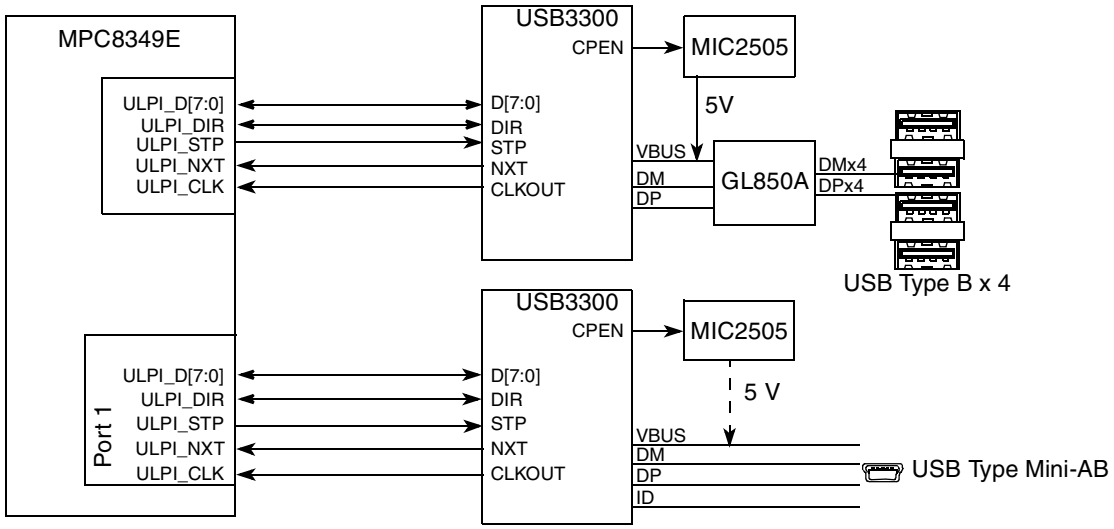

Figure 13. USB Port 0 and Port 1 Connections

1.2.15 PCI Subsystem

The MPC8349E has two PCI interfaces (PCI1 and PCI2). PCI1 interface signals connect only to the SATA controller (SiI3114). PCI2 connects to a 32-bit 3.3 V PCI slot and the MiniPCI slot.

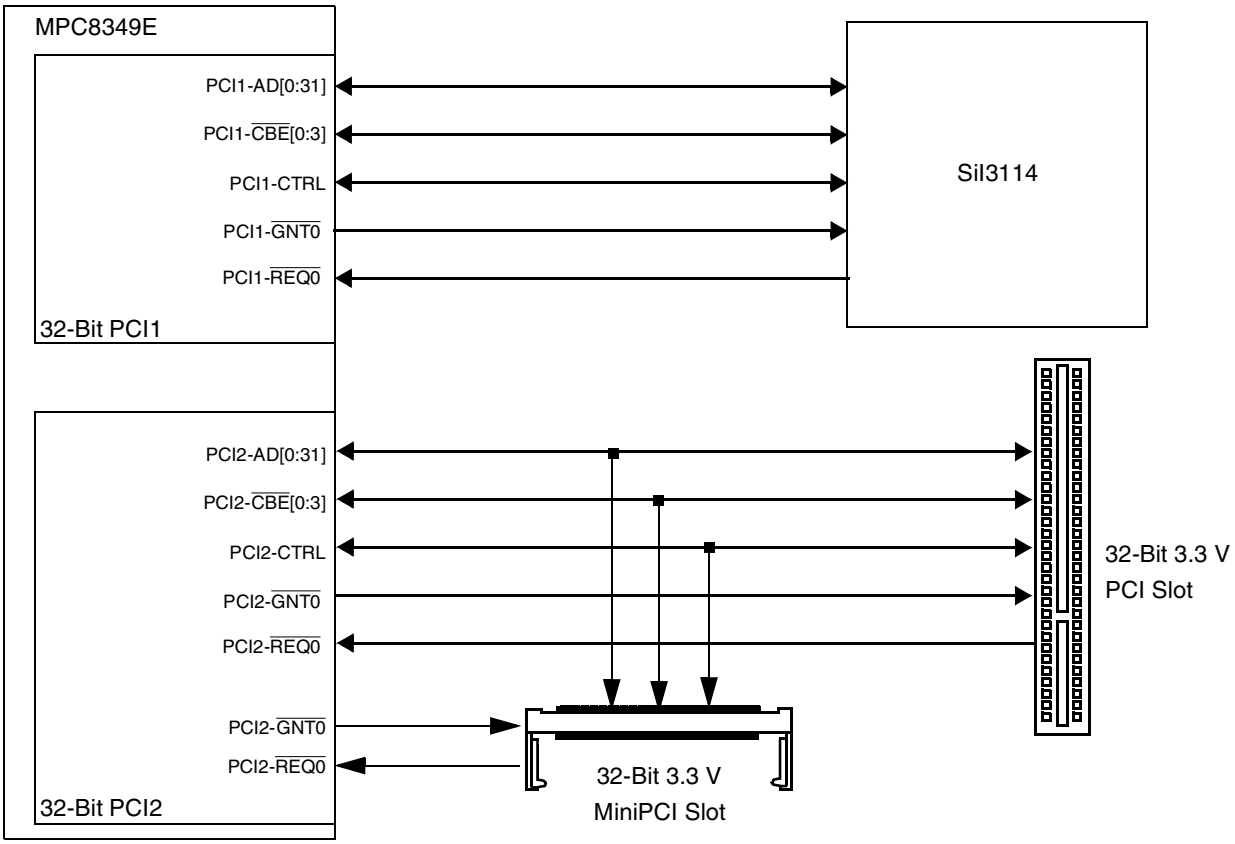

Figure 14. PCI Subsystem

1.2.16 MCU Subsystem

The Freescale MC9S08QG8 is a highly integrated, low-power microcontroller that offers 8 Kbyte Flash memory, 512 bytes of SRAM, I^2C, SCI, SPI, 10-bit A/D, timers, and on-chip debugging. It can use an external 32.768 KHz crystal oscillator or an internal oscillator (trim-able to +/– 2%), with an on-chip frequency locked loop multiplier to 8 MHz bus clock operation. In this design, it provides push button soft power-up, software-controlled power-down, and fan and LED control. With additional microcontroller firmware, it can provide an I^2C real-time clock and EEPROM emulation capability, thermal measurement, IR remote control, and other advanced features. The main connection to the MPC8349E is I^2C (1), but an alternative UART (2) connection is also available.

1.2.17 COP/JTAG Port

The common on-chip processor (COP) is part of the MPC8349E JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the Ethernet port, USB port, parallel port, RS-232, and so on. A typical setup using a USB port emulator is shown in Figure 15.

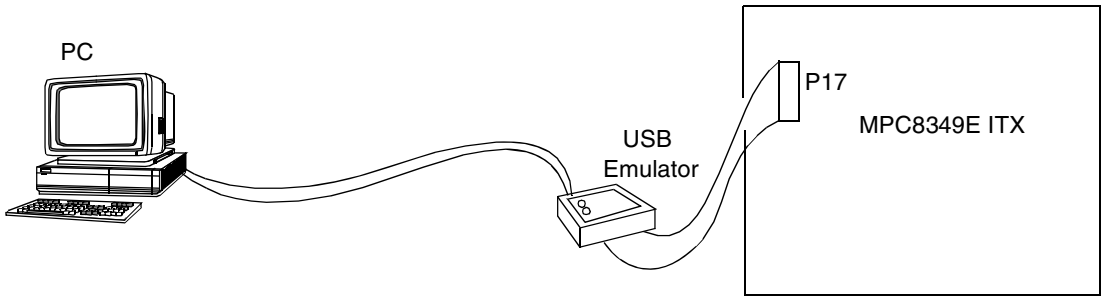

Figure 15. Connecting the MPC8349E-mITXE Board to A Parallel Emulator

The 16-pin generic header connector carries the COP/JTAG signals and the additional signals for system debugging. The pinout of this connector is shown in Figure 16.

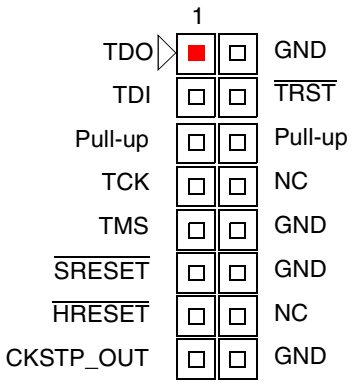

Figure 16. MPC8349E-mITXE Board COP Connector

1.3 MPC8349E-mITXE Assembly

The MPC8349E-mITX board PCB top view is shown in Figure 17, with the references of LEDs, jumpers, headers, and switches.

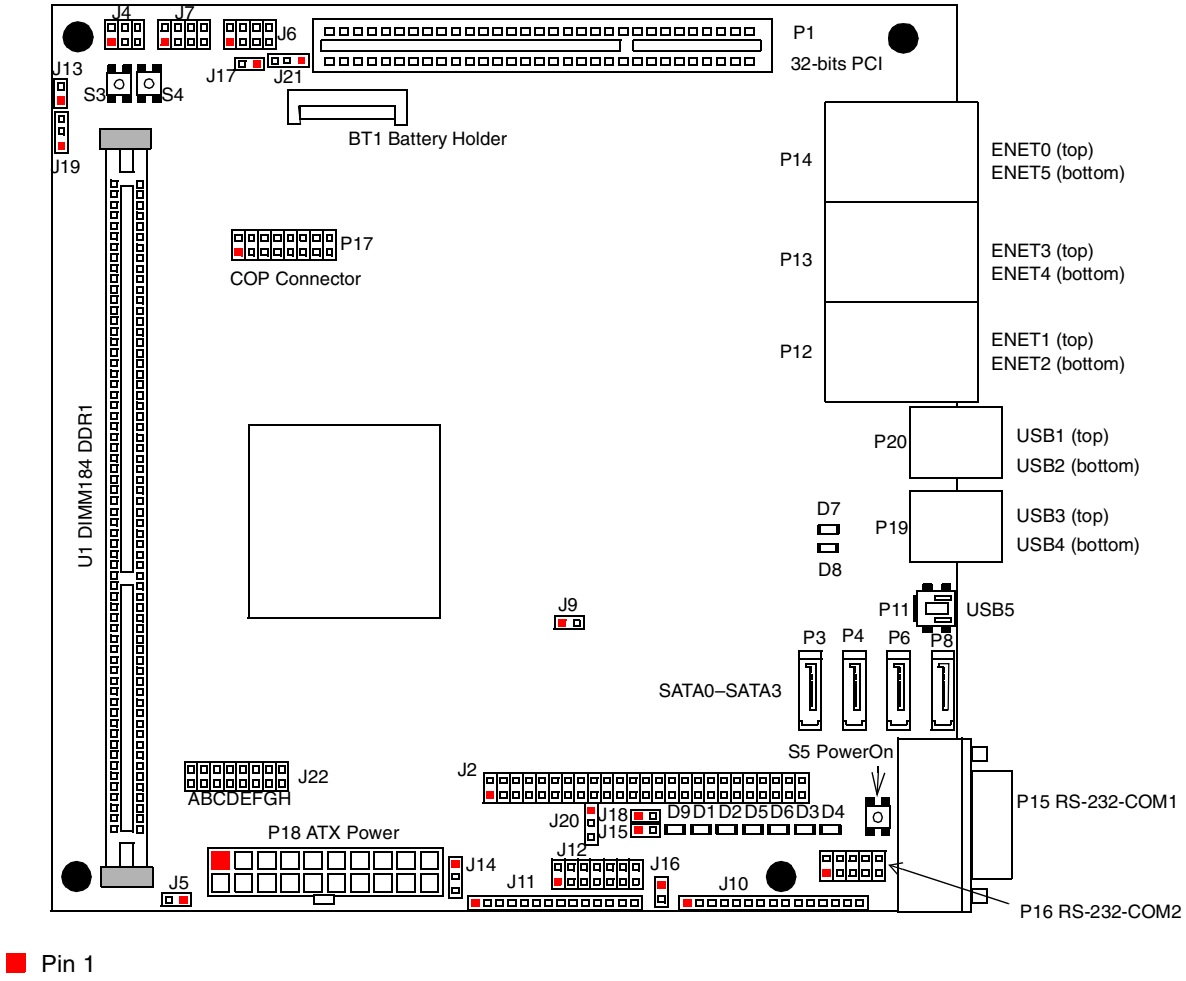

Figure 17. MPC8349E-mITX Top View

The MPC8349E-mITXE board bottom view is shown in Figure 18.

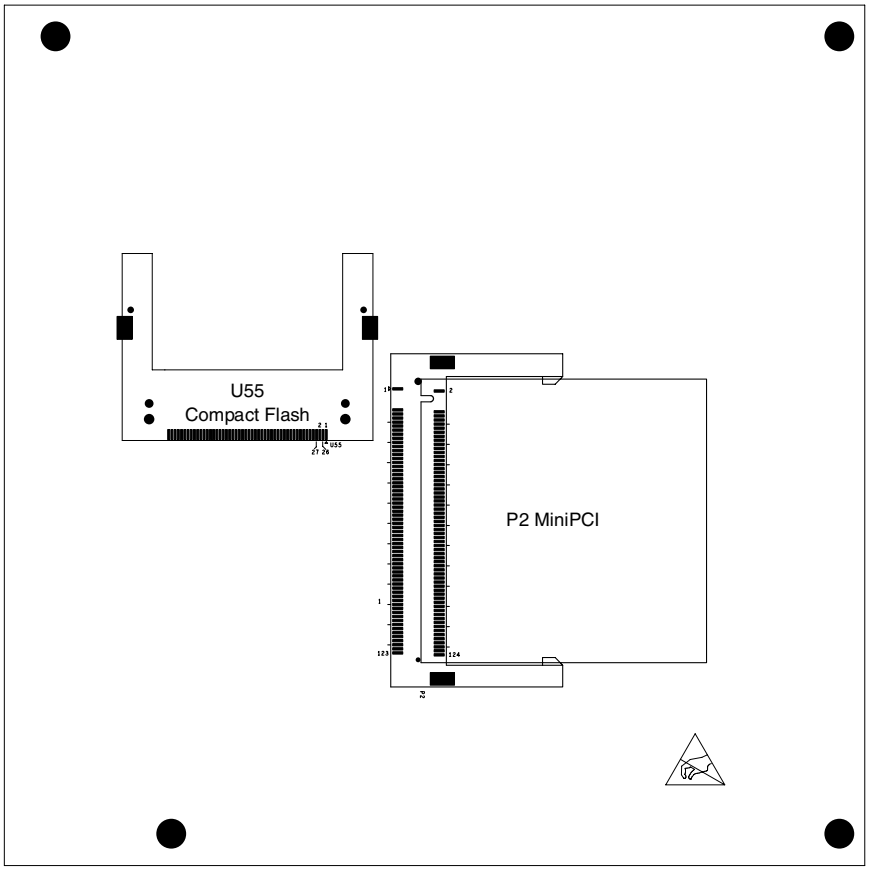

Figure 18. MPC8349E-mITXE Bottom View

CAUTION

Use Compact Flash 3.3 V only. Powerdown before insertion or removal.

CAUTION

Use Mini-PCI 3.3 V only. Powerdown before insertion or removal

1.4 Connectors

This section describes the MPC8349E-mITXE connectors and their pin assignments.

1.4.1 Case Connector

The case connector (J10) connects to the case power switch, power LED, reset switch, and hard disk LED.

- PWR_SW can connect to the 2-pin power push button on the front panel.
- PWR_LED lights when the system is turned ON.
- RST_SW can connect to the 2-pin reset push button on the front panel.
- HD[0:3] are the hard disk LEDs that show activity on each hard disk.

Table 10 lists the pin assignments of the case connector.

Table 10. Case Connector J10 Pin Assignments

Pin	Signal
1	Power LED K
2	Power LED A
3	Power LED A
4	GND
5	Power On
6	GND
7	RESET
8	HD0 LED K
9	HD0 LED A
10	HD1 LED K
11	HD1 LED A
12	HD2 LED K
13	HD2 LED A
14	HD3 LED K
15	HD3 LED A

1.4.2 COP Connector

The COP connector (P17) allows the user to connect a COP/JTAG-based debugger to the MPC8349E-mITXE board for debugging. Table 11 lists the pin assignments of the COP connector.

Table 11. COP Connector Pin Assignments

Pin	Signal	Pin	Signal
1	TDO	2	GND
3	TDI	4	$\overline{\text{TRST}}$
5	$\overline{\text{QREQ}}$	6	VDD_SENSE
7	TCK	8	$\overline{\text{CHKSTOP\_IN}}$
9	TMS	10	NC
11	$\overline{\text{SRESET}}$	12	NC
13	$\overline{\text{HRESET}}$	14	GND

1.4.3 RS-232 Connectors

Serial interface COM1 is available at connector P15, and another serial port connection COM2 is available through a 10-pin connector P16 with pin assignment as shown in Table 12.

Table 12. COM2 Connector Pin Description

Pin	Signal	Pin	Signal
1	GND	2	TXD
3	RXD	4	NC
5	NC	6	GND
7	CTS	8	RTS
9	NC	10	NC

1.4.4 Serial ATA (SATA) Connectors

The SATA connectors (P3, P4, P6, P8) connect to the serial ATA hard disks through serial ATA cables. P3 corresponds to harddisk0, and P4, P6, P8 correspond to harddisk1, harddisk2, and harddisk3, respectively.

1.4.5 Local Bus Expansion Connector

The local bus expansion connector (J2) provides 16-bit data and 9-bit addressing capability for external modules controlled by a single chip-select signal ($\overline{CS2}$). It has six GPIO pins, two IRQs, and one SPI interface. The pin assignments are listed in Table 8 in Section 1.2.10, “Local Bus Expansion Connector.”

1.4.6 PCI Slot

The MPC8349E-mITXE board has one 32-bit 3.3 V PCI expansion slot (P1) for an expansion card.

WARNING

Only the 3.3 V PCI Card is supported. Turn OFF power during insertion and removal of PCI card.

3.3 V PCI cards can be identified by the key position on the PCI card, as shown in Figure 19.

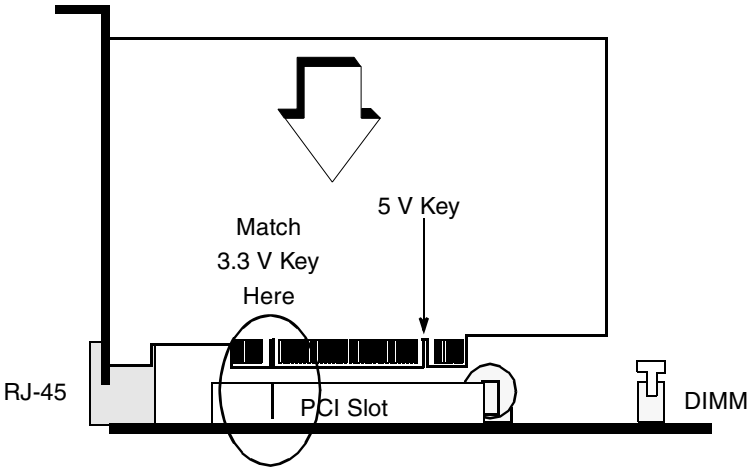

Figure 19. 3.3 V Key on a Typical 3.3 V PCI Card

1.4.7 Fan Connectors

There are two fan connectors on the MPC8349E-mITXE board, one for powering a 5 V fan (J9) and the other for powering a 12 V fan (J5). For typical fans, the red wire is always positive (+) and the black wire is always negative (–).

1.4.8 MiniPCI Connector

A MiniPCI connector (P2) for MiniPCI card installation is located on the rear side of the board. Figure 20 shows how to install a MiniPCI card.

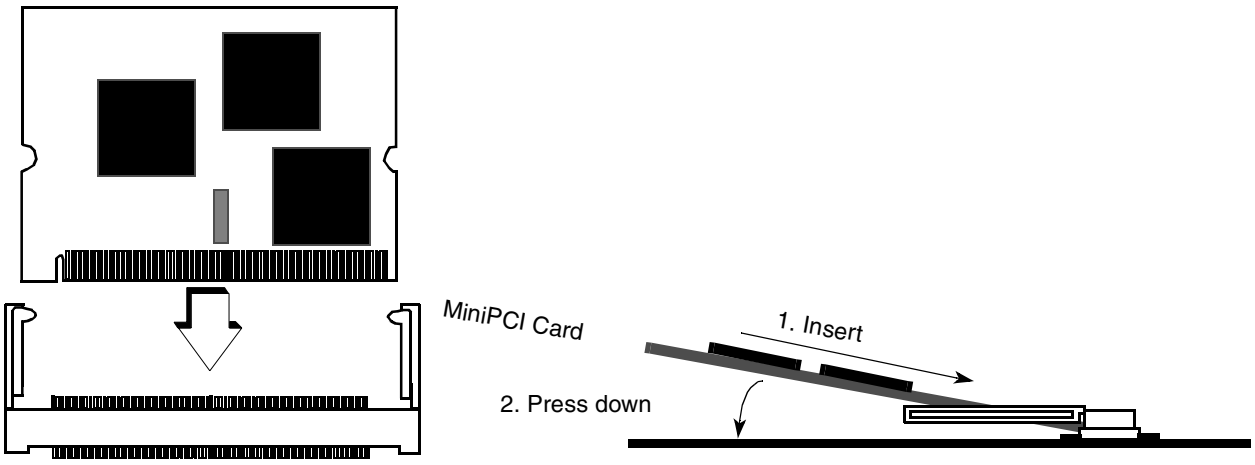

Figure 20. Installation of MiniPCI Card