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Freescale Semiconductor
Technical Data

MPC8349EA PowerQUICC II Pro Integrated Host Processor Hardware Specifications

The MPC8349EA PowerQUICC II Pro is a next generation PowerQUICC II integrated host processor. The MPC8349EA contains a processor core built on Power Architecture® technology with system logic for networking, storage, and general-purpose embedded applications. For functional characteristics of the processor, refer to the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.

To locate published errata or updates for this document, refer to the MPC8349EA product summary page on our website, as listed on the back cover of this document, or contact your local Freescale sales office.

Contents

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NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications.*

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

1   Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8349EA.
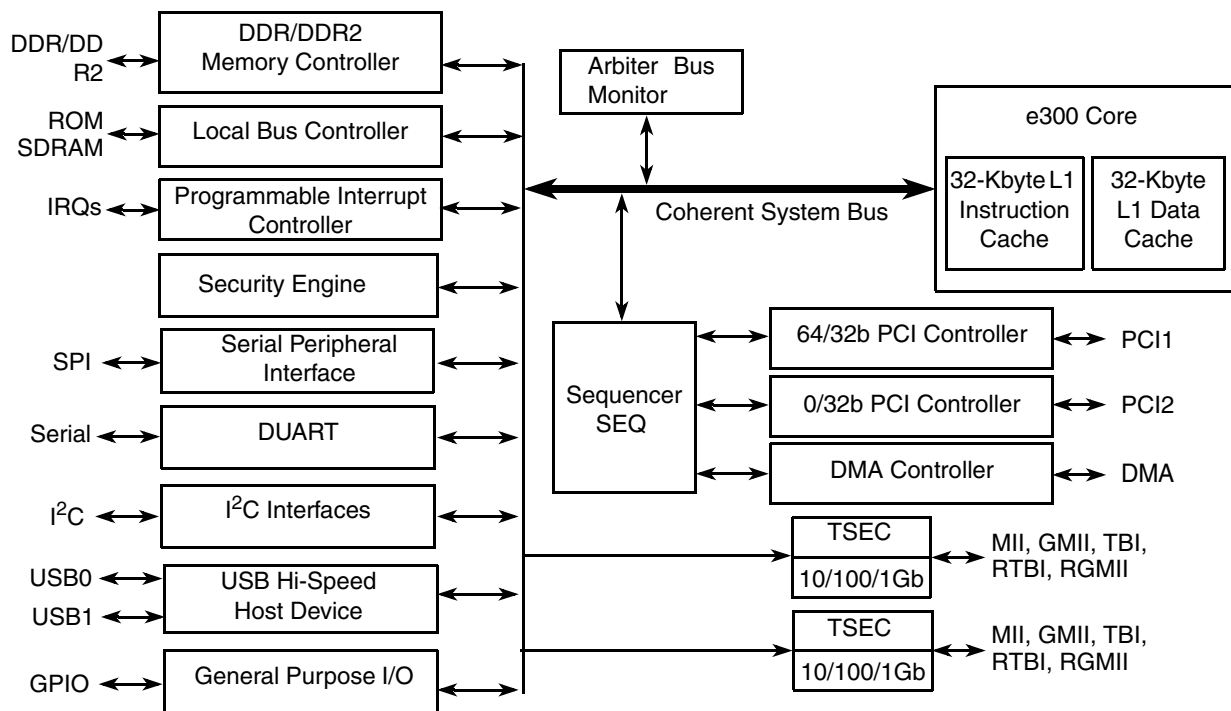

Figure 1. MPC8349EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology

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- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- or 64-bit data interface, up to 400 MHz data rate
  - Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
  - DRAM chip configurations from 64 Mbits to 1 Gbit with ×8/×16 data ports
  - Full error checking and correction (ECC) support
  - Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep-mode support for SDRAM self refresh
  - Auto refresh
  - On-the-fly power management using CKE
  - Registered DIMM support
  - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ac™ standards
  - Ethernet physical interfaces:
    - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- Dual PCI interfaces
  - Designed to comply with *PCI Specification Revision 2.3*
  - Data bus width options:
    - Dual 32-bit data PCI interfaces operating at up to 66 MHz
    - Single 64-bit data PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities on both interfaces
  - PCI agent mode on PCI1 interface
  - PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Posting of processor-to-PCI and PCI-to-memory writes

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- — On-chip arbitration supporting five masters on PCI1, three masters on PCI2
- — Accesses to all PCI address spaces
- — Parity supported
- — Selectable hardware-enforced coherency
- — Address translation units for address mapping between host and peripheral
- — Dual address cycle for target
- — Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
  - — Public key execution unit (PKEU) :
    - – RSA and Diffie-Hellman algorithms
    - – Programmable field size up to 2048 bits
    - – Elliptic curve cryptography
    - – F2m and F(p) modes
    - – Programmable field size up to 511 bits
  - — Data encryption standard (DES) execution unit (DEU)
    - – DES and 3DES algorithms
    - – Two key (K1, K2) or three key (K1, K2, K3) for 3DES
    - – ECB and CBC modes for both DES and 3DES
  - — Advanced encryption standard unit (AESU)
    - – Implements the Rijndael symmetric-key cipher
    - – Key lengths of 128, 192, and 256 bits
    - – ECB, CBC, CCM, and counter (CTR) modes
  - — XOR parity generation accelerator for RAID applications
  - — ARC four execution unit (AFEU)
    - – Stream cipher compatible with the RC4 algorithm
    - – 40- to 128-bit programmable key
  - — Message digest execution unit (MDEU)
    - – SHA with 160-, 224-, or 256-bit message digest
    - – MD5 with 128-bit message digest
    - – HMAC with either algorithm
  - — Random number generator (RNG)
  - — Four crypto-channels, each supporting multi-command descriptor chains
    - – Static and/or dynamic assignment of crypto-execution units through an integrated controller
    - – Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
  - — USB on-the-go mode with both device and host functionality

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- — Complies with USB specification Rev. 2.0
- — Can operate as a stand-alone USB device
  - – One upstream facing port
  - – Six programmable USB endpoints
- — Can operate as a stand-alone USB host controller
  - – USB root hub with one downstream-facing port
  - – Enhanced host controller interface (EHCI) compatible
  - – High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- — External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
  - — Can operate as a stand-alone USB host controller
    - – USB root hub with one or two downstream-facing ports
    - – Enhanced host controller interface (EHCI) compatible
    - – Complies with *USB Specification Rev. 2.0*
  - — High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - — Direct connection to a high-speed device without an external hub
  - — External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
  - — Multiplexed 32-bit address and data operating at up to 133 MHz
  - — Eight chip selects for eight external slaves
  - — Up to eight-beat burst transfers
  - — 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - — Three protocol engines on a per chip select basis:
    - – General-purpose chip select machine (GPCM)
    - – Three user-programmable machines (UPMs)
    - – Dedicated single data rate SDRAM controller
  - — Parity support
  - — Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - — Functional and programming compatibility with the MPC8260 interrupt controller
  - — Support for 8 external and 35 internal discrete interrupt sources
  - — Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - — Programmable highest priority request
  - — Four groups of interrupts with programmable priority
  - — External and internal interrupts directed to host processor
  - — Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  - — Unique vector number for each interrupt source

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- Dual industry-standard I^{2}C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I^{2}C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from I^{2}C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Handshaking (external control) signals for all channels: $\overline{\text{DMA\_DREQ}}$[0:3], $\overline{\text{DMA\_DACK}}$[0:3], $\overline{\text{DMA\_DDONE}}$[0:3]
  - All channels accessible to local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
  - 64 parallel I/O pins multiplexed on various chip interfaces
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8349EA. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Parameter		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	−0.3 to 1.32 (1.36 max for 667-MHz core frequency)	V	—
PLL supply voltage		AV_{DD}	−0.3 to 1.32 (1.36 max for 667-MHz core frequency)	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	−0.3 to 2.75 −0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	−0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	−0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV_{IN}	−0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	−0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	−0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	−0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	−0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	−55 to 150	°C	—

Notes:

[1] Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

[2] **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

[3] **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

[4] **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

[5] (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

[6] OVIN on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

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2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8349EA. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Recommended Value	Unit	Notes
Core supply voltage for 667-MHz core frequency	V_{DD}	1.3 V ± 60 mV	V	1
Core supply voltage	V_{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage for 667-MHz core frequency	AV_{DD}	1.3 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I²C, and JTAG I/O voltage	OV_{DD}	3.3 V ± 330 mV	V	—

Note:

[1] GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8349EA.
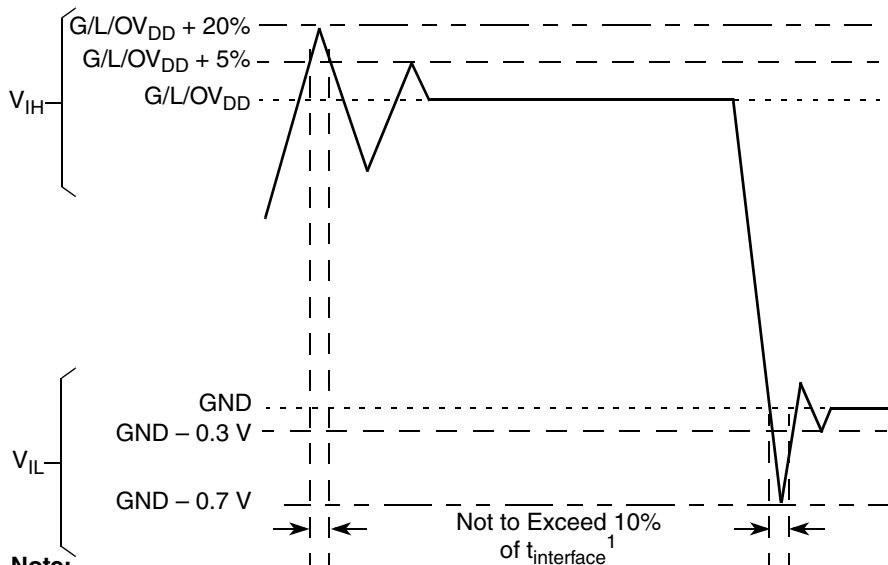
Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}/LV_{DD}

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8349EA for the 3.3-V signals, respectively.
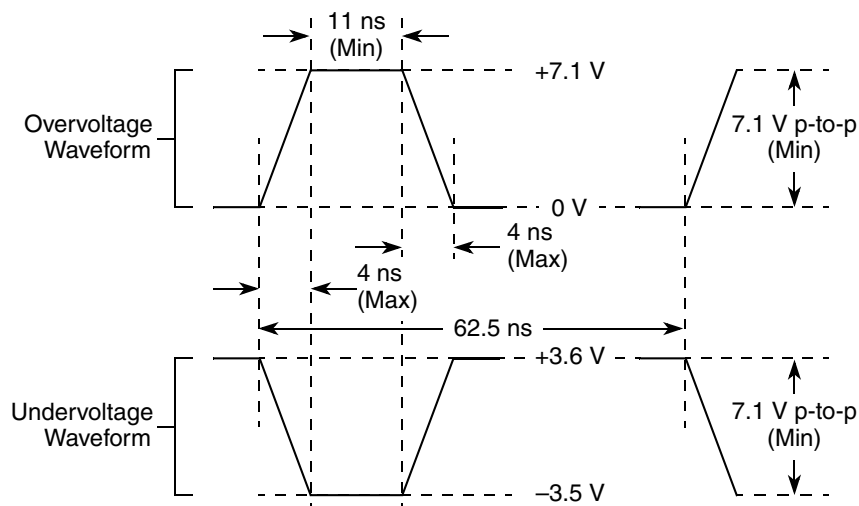

Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3   Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV_{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV_{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV_{DD} = 1.8 V
TSEC/10/100 signals	40	LV_{DD} = 2.5/3.3 V
DUART, system control, I^{2}C, JTAG, USB	40	OV_{DD} = 3.3 V
GPIO signals	40	OV_{DD} = 3.3 V, LV_{DD} = 2.5/3.3 V

2.2   Power Sequencing

This section details the power sequencing considerations for the MPC8349EA.

2.2.1   Power-Up Sequencing

MPC8349EA does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power

supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}, LV_{DD}, and OV_{DD}) and assert $\overline{PORESET}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 4.
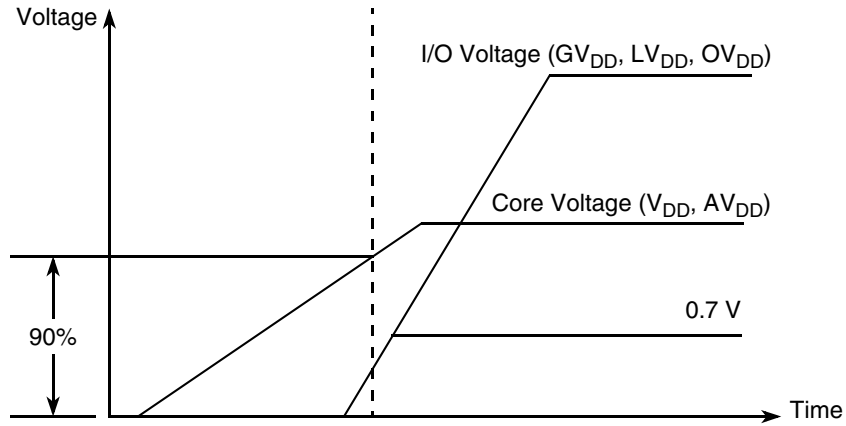
Figure 4. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

3   Power Characteristics

The estimated typical power dissipation for the MPC8349EA device is shown in Table 4.

Table 4. MPC8349EA Power Dissipation[1]

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at T_J = 65	Typical[2, 3]	Maximum[4]	Unit
TBGA	333	333	2.0	3.0	3.2	W
		166	1.8	2.8	2.9	W
	400	266	2.1	3.0	3.3	W
		133	1.9	2.9	3.1	W
	450	300	2.3	3.2	3.5	W
		150	2.1	3.0	3.2	W
	500	333	2.4	3.3	3.6	W
		166	2.2	3.1	3.4	W
	533	266	2.4	3.3	3.6	W
		133	2.2	3.1	3.4	W
	667[5, 6]	333	3.5	4.6	5	W

[1] The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 5.

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2 Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.

3 Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.

4 Maximum power is based on a voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

5 Typical power is based on a voltage of V_{DD} = 1.3 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.

6 Maximum power is based on a voltage of V_{DD} = 1.3 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

Table 5 shows the estimated typical I/O power dissipation for MPC8349EA.

Table 5. MPC8349EA Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V Rs = 20 Ω Rt = 50 Ω 2 pair of clocks	200 MHz, 32 bits	0.31	0.42	—	—	—	W	—
	200 MHz, 64 bits	0.42	0.55	—	—	—	W	—
	266 MHz, 32 bits	0.35	0.5	—	—	—	W	—
	266 MHz, 64 bits	0.47	0.66	—	—	—	W	—
	300 MHz, 32 bits	0.37	0.54	—	—	—	W	—
	300 MHz, 64 bits	0.50	0.7	—	—	—	W	—
	333 MHz, 32 bits	0.39	0.58	—	—	—	W	—
	333 MHz, 64 bits	0.53	0.76	—	—	—	W	—
	400 MHz, 32 bits	0.44	—	—	—	—	—	—
	400 MHz, 64 bits	0.59	—	—	—	—	—	—
PCI I/O load = 30 pF	33 MHz, 64 bits	—	—	0.08	—	—	W	—
	66 MHz, 64 bits	—	—	0.14	—	—	W	—
	33 MHz, 32 bits	—	—	0.04	—	—	W	Multiply by 2 if using 2 ports.
	66 MHz, 32 bits	—	—	0.07	—	—	W	
Local bus I/O load = 25 pF	133 MHz, 32 bits	—	—	0.27	—	—	W	—
	83 MHz, 32 bits	—	—	0.17	—	—	W	—
	66 MHz, 32 bits	—	—	0.14	—	—	W	—
	50 MHz, 32 bits	—	—	0.11	—	—	W	—
TSEC I/O load = 25 pF	MII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.06	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
USB	12 MHz	—	—	0.01	—	—	W	Multiply by 2 if using 2 ports.
	480 MHz	—	—	0.2	—	—	W	
Other I/O		—	—	0.01	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8349EA.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	−0.3	0.4	V
CLKIN input current	$0\ V \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0\ V \leq V_{IN} \leq 0.5\ V$ or $OV_{DD} - 0.5\ V \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5\ V \leq V_{IN} \leq OV_{DD} - 0.5\ V$	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8349EA can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 50 KHz modulation rate regardless of input frequency.

4.3   TSEC Gigabit Reference Clock Timing

Table 8 provides the TSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	45 47	—	55 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.

2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.4, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5   RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8349EA.

5.1   RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8349EA.

Table 9. RESET Pins DC Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage[2]	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V

Table 9. RESET Pins DC Electrical Characteristics[1] (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:

1. This table applies for pins $\overline{PORESET}$, $\overline{HRESET}$, $\overline{SRESET}$, and $\overline{QUIESCE}$.
2. $\overline{HRESET}$ and $\overline{SRESET}$ are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 RESET AC Electrical Characteristics

Table 10 provides the reset initialization AC timing specifications of the MPC8349EA.

Table 10. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{HRESET}$ or $\overline{SRESET}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{PORESET}$ with stable clock applied to CLKIN when the MPC8349EA is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{PORESET}$ with stable clock applied to PCI_SYNC_IN when the MPC8349EA is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{HRESET}$/$\overline{SRESET}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{HRESET}$ negation to $\overline{SRESET}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{PORESET}$ when the MPC8349EA is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{PORESET}$ when the MPC8349EA is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{HRESET}$	0	—	ns	—
Time for the MPC8349EA to turn off POR configuration signals with respect to the assertion of $\overline{HRESET}$	—	4	ns	3
Time for the MPC8349EA to turn on POR configuration signals with respect to the negation of $\overline{HRESET}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."

6   DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8349EA. Note that DDR SDRAM is $GV_{DD}(typ) = 2.5$ V and DDR2 SDRAM is $GV_{DD}(typ) = 1.8$ V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

> **NOTE**
>
> The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications.* See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

6.1   DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8349EA when $GV_{DD}(typ) = 1.8$ V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 1.8$ V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	−0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	−9.9	9.9	μA	4
Output high current ($V_{OUT} = 1.420$ V)	I_{OH}	−13.4	—	mA	—

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV$_{DD}$(typ) = 1.8 V (continued)

Output low current (V$_{OUT}$ = 0.280 V)	I$_{OL}$	13.4	—	mA	—

Notes:

1. GV$_{DD}$ is expected to be within 50 mV of the DRAM GV$_{DD}$ at all times.

2. MV$_{REF}$ is expected to equal 0.5 × GV$_{DD}$, and to track GV$_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MV$_{REF}$ cannot exceed ±2% of the DC value.

3. V$_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV$_{REF}$. This rail should track variations in the DC level of MV$_{REF}$.

4. Output leakage is measured with all outputs disabled, 0 V ≤ V$_{OUT}$ ≤ GV$_{DD}$.

Table 13 provides the DDR2 capacitance when GV$_{DD}$(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for GV$_{DD}$(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C$_{IO}$	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C$_{DIO}$	—	0.5	pF	1

Note:

1. This parameter is sampled. GV$_{DD}$ = 1.8 V ± 0.090 V, f = 1 MHz, T$_A$ = 25°C, V$_{OUT}$ = GV$_{DD}$/2, V$_{OUT}$ (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when GV$_{DD}$(typ) = 2.5 V.

Table 14. DDR SDRAM DC Electrical Characteristics for GV$_{DD}$(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV$_{DD}$	2.375	2.625	V	1
I/O reference voltage	MV$_{REF}$	0.49 × GV$_{DD}$	0.51 × GV$_{DD}$	V	2
I/O termination voltage	V$_{TT}$	MV$_{REF}$ − 0.04	MV$_{REF}$ + 0.04	V	3
Input high voltage	V$_{IH}$	MV$_{REF}$ + 0.18	GV$_{DD}$ + 0.3	V	—
Input low voltage	V$_{IL}$	−0.3	MV$_{REF}$ − 0.18	V	—
Output leakage current	I$_{OZ}$	−9.9	−9.9	μA	4
Output high current (V$_{OUT}$ = 1.95 V)	I$_{OH}$	−15.2	—	mA	—
Output low current (V$_{OUT}$ = 0.35 V)	I$_{OL}$	15.2	—	mA	—

Notes:

1. GV$_{DD}$ is expected to be within 50 mV of the DRAM GV$_{DD}$ at all times.

2. MV$_{REF}$ is expected to be equal to 0.5 × GV$_{DD}$, and to track GV$_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MV$_{REF}$ may not exceed ±2% of the DC value.

3. V$_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV$_{REF}$. This rail should track variations in the DC level of MV$_{REF}$.

4. Output leakage is measured with all outputs disabled, 0 V ≤ V$_{OUT}$ ≤ GV$_{DD}$.

Table 15 provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 15. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5$ V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5$ V ± 0.125 V, f = 1 MHz, $T_A = 25°C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:

1. The voltage regulator for MV_{REF} must supply up to 500 μA current.

6.2   DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1   DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ) = 1.8$ V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V	—

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5$ V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
400 MHz		−600	600		3
333 MHz		−750	750		—
266 MHz		−750	750		—
200 MHz		−750	750		—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: $t_{DISKEW} = \pm (T/4 - abs (t_{CISKEW}))$; where T is the clock period and abs (t_{CISKEW}) is the absolute value of t_{CISKEW}.

3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.
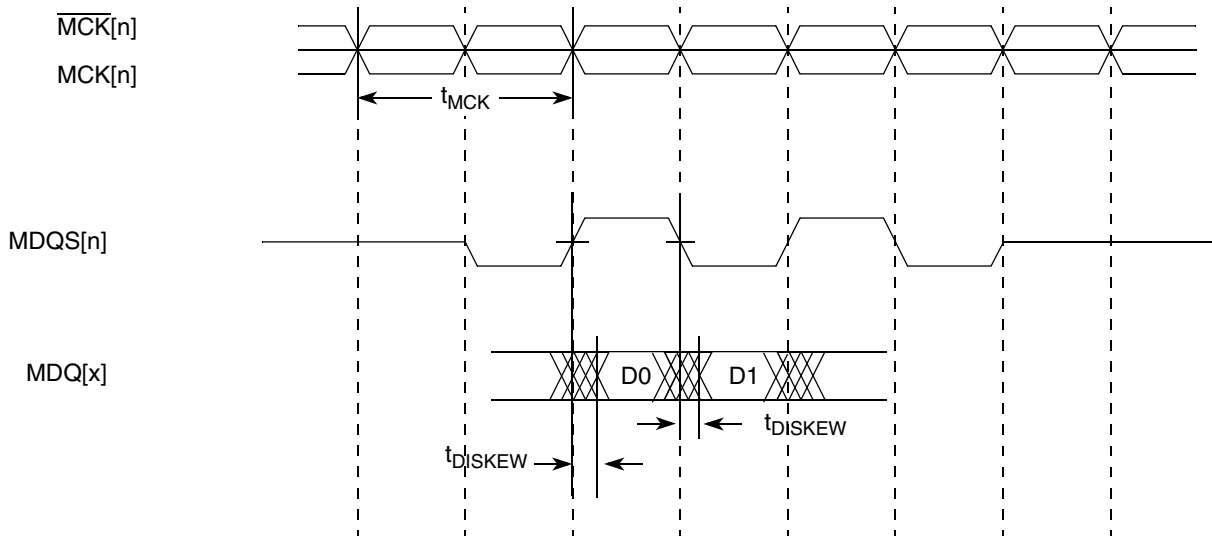

Figure 5. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
ADDR/CMD/MODT output setup with respect to MCK	t_{DDKHAS}		—	ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
ADDR/CMD/MODT output hold with respect to MCK	t_{DDKHAX}		—	ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
$\overline{MCS}$(n) output setup with respect to MCK	t_{DDKHCS}		—	ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
$\overline{MCS}$(n) output hold with respect to MCK	t_{DDKHCX}		—	ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCK to MDQS Skew	t_{DDKHMH}	−0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	$t_{DDKHDS},$ t_{DDKLDS}			ps	5
400 MHz		700	—		
333 MHz		775	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQ/MECC/MDM output hold with respect to MDQS	$t_{DDKHDX},$ t_{DDKLDX}			ps	5
400 MHz		700	—		
333 MHz		900	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	−0.6	0.6	ns	6

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.

2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.

3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for the timing modifications enabled by use of these bits.

5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.

6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).
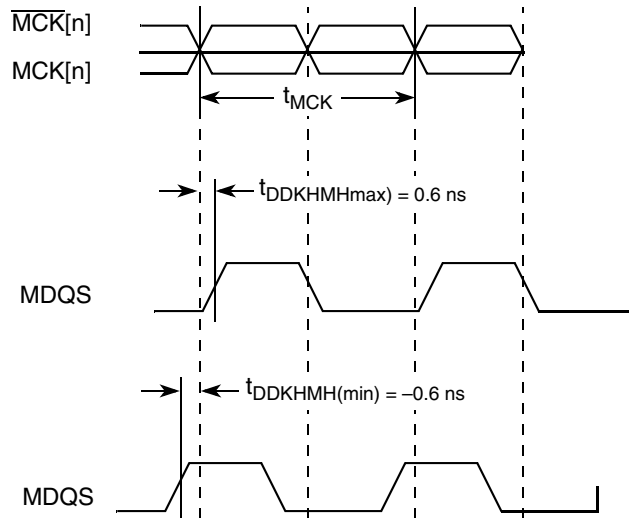

Figure 6. Timing Diagram for t_{DDKHMH}

Figure 7 shows the DDR SDRAM output timing diagram.
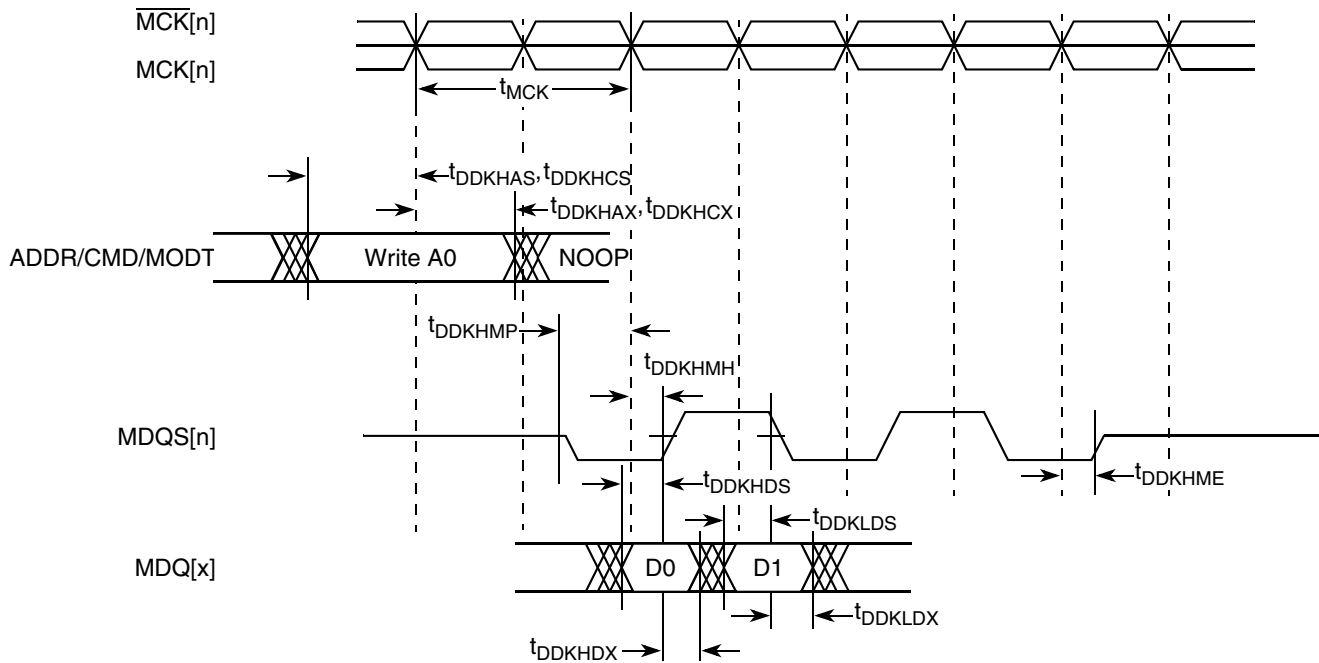

Figure 7. DDR SDRAM Output Timing Diagram

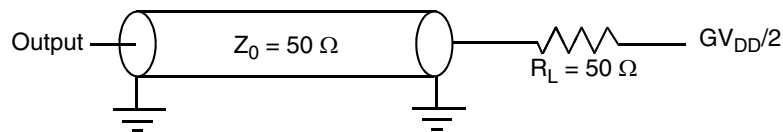Figure 8 provides the AC test load for the DDR bus.

Figure 8. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8349EA.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface of the MPC8349EA.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	−0.3	0.8	V
Input current (0.8 V ≤ V_{IN} ≤ 2 V)	I_{IN}	—	±5	μA

Table 21. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
High-level output voltage, $I_{OH} = -100\ \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100\ \mu A$	V_{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8349EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1   TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}[2]	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0$ mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	$I_{OL} = 4.0$ mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	−0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	40	μA
Input low current	I_{IL}	V_{IN}[1] = GND		−600	—	μA

Notes:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.
2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0$ mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	$I_{OL} = 1.0$ mA	LV_{DD} = Min	GND − 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	−0.3	0.70	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	10	μA
Input low current	I_{IL}	V_{IN}[1] = GND		−15	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2   GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1   GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.1.1   GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

Table 25. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK clock rise time (20%–80%)	t_{GTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t_{GTXF}	—	—	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

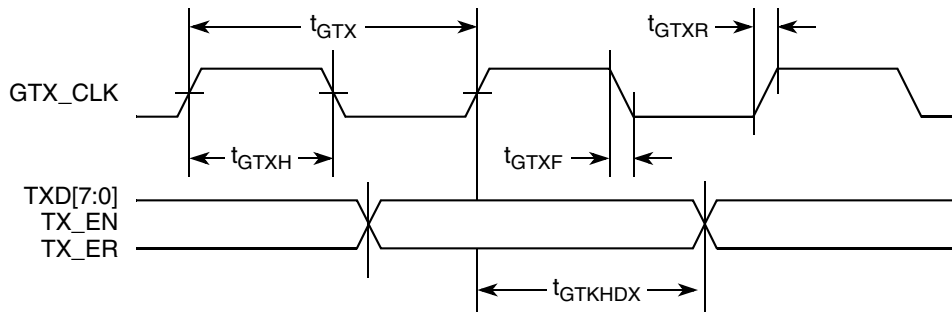Figure 9 shows the GMII transmit AC timing diagram.

Figure 9. GMII Transmit AC Timing Diagram

8.2.1.2   GMII Receive AC Timing Specifications

Table 26 provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns

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Table 26. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV$_{DD}$/OV$_{DD}$ of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock rise (20%–80%)	t$_{GRXR}$	—	—	1.0	ns
RX_CLK clock fall time (80%–20%)	t$_{GRXF}$	—	—	1.0	ns

Note:

1. The symbols for timing specifications follow the pattern of t$_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and t$_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t$_{GRDVKH}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t$_{RX}$ clock reference (K) going to the high state (H) or setup time. Also, t$_{GRDXKL}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t$_{GRX}$ clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t$_{GRX}$ represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the GMII receive AC timing diagram.
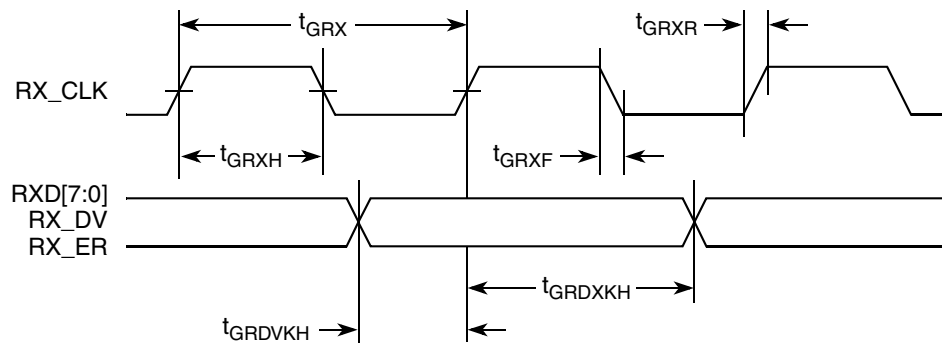
Figure 10. GMII Receive AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 27 provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Timing Specifications

At recommended operating conditions with LV$_{DD}$/OV$_{DD}$ of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t$_{MTX}$	—	400	—	ns
TX_CLK clock period 100 Mbps	t$_{MTX}$	—	40	—	ns
TX_CLK duty cycle	t$_{MTXH}$/t$_{MTX}$	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t$_{MTKHDX}$	1	5	15	ns