



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



MPC8358E

PowerQUICC II Pro Processor

Revision 2.1 PBGA Silicon

Hardware Specifications

This document provides an overview of the MPC8358E PowerQUICC II Pro processor revision 2.1 PBGA features, including a block diagram showing the major functional components. This device is a cost-effective, highly integrated communications processor that addresses the needs of the networking, wireless infrastructure, and telecommunications markets. Target applications include next generation DSLAMs, network interface cards for 3G base stations (Node Bs), routers, media gateways, and high end IADs. The device extends current PowerQUICC II Pro offerings, adding higher CPU performance, additional functionality, faster interfaces, and robust interworking between protocols while addressing the requirements related to time-to-market, price, power, and package size. This device can be used for the control plane and also has data plane functionality.

For functional characteristics of the processor, refer to the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*, Rev. 3.

To locate any updates for this document, refer to the MPC8360E product summary page on our website listed on the back cover of this document or contact your Freescale sales office.

Contents

1. Overview	2
2. Electrical Characteristics	7
3. Power Characteristics	12
4. Clock Input Timing	13
5. RESET Initialization	15
6. DDR and DDR2 SDRAM	18
7. DUART	25
8. UCC Ethernet Controller: Three-Speed Ethernet, MII Management	25
9. Local Bus	39
10. JTAG	45
11. I ² C	49
12. PCI	51
13. Timers	53
14. GPIO	54
15. IPIC	55
16. SPI	55
17. TDM/SI	57
18. UTOPIA/POS	59
19. HDLC, BISYNC, Transparent, and Synchronous UART	61
20. USB	64
21. Package and Pin Listings	65
22. Clocking	73
23. Thermal	84
24. System Design Information	89
25. Ordering Information	92
26. Document Revision History	94

1 Overview

This section describes a high-level overview including features and general operation of the MPC8358E PowerQUICC II Pro processor. A major component of this device is the e300 core, which includes 32 Kbytes of instruction and data cache and is fully compatible with the Power Architecture™ 603e instruction set. The new QUICC Engine module provides termination, interworking, and switching between a wide range of protocols including ATM, Ethernet, HDLC, and POS. The QUICC Engine module's enhanced interworking eases the transition and reduces investment costs from ATM to IP based systems. The MPC8358E has a single DDR SDRAM memory controller. The MPC8358E also offers a 32-bit PCI controller, a flexible local bus, and a dedicated security engine.

Figure 1 shows the MPC8358E block diagram.

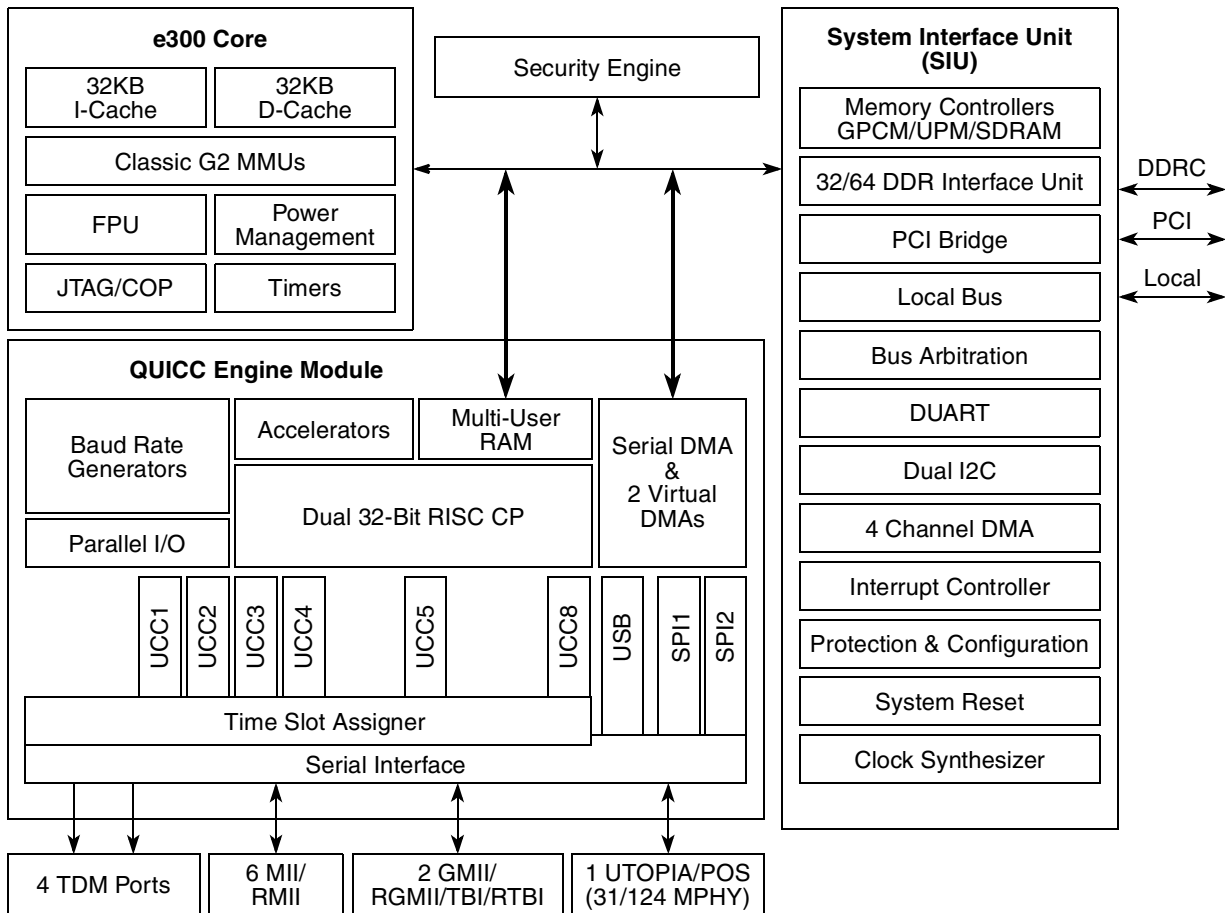


Figure 1. MPC8358E Block Diagram

Major features of the MPC8358E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
 - Operates at up to 400 MHz (for the MPC8358E)
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units

- 32-Kbyte instruction cache, 32-Kbyte data cache
- Lockable portion of L1 cache
- Dynamic power management
- Software-compatible with the Freescale processor families implementing the Power Architecture™ technology
- QUICC Engine unit
 - Two 32-bit RISC controllers for flexible support of the communications peripherals, each operating up to 400 MHz (for the MPC8358E)
 - Serial DMA channel for receive and transmit on all serial channels
 - QUICC Engine module peripheral request interface (for SEC, PCI, IEEE Std. 1588™)
 - Six UCCs on the MPC8358E supporting the following protocols and interfaces (not all of them simultaneously):
 - IEEE 1588 protocol supported
 - 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)¹
 - 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
 - 9.6-Kbyte jumbo frames
 - ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
 - ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
 - ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
 - ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
 - IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
 - ATM Transmission Convergence layer support in accordance with ITU-T I.432
 - ATM OAM handling features compatible with ITU-T I.610
 - PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
 - IP support for IPv4 packets including TOS, TTL, and header checksum processing
 - Ethernet over first mile IEEE 802.3ah
 - Shim header
 - Ethernet-to-Ethernet/AAL5/AAL2 inter-working
 - L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q™ VLAN tags

¹.SMII or SGMII media-independent interface is not currently supported.

- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels
- One UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management
- Four TDM interfaces on the MPC8358E with 1-bit mode for E3/T3 rates in clear channel
- Sixteen independent baud rate generators and 30 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as four 32-bit timers
- Interworking functionality:
 - Layer 2 10/100-Base T Ethernet switch
 - ATM-to-ATM switching (AAL0, 2, 5)
 - Ethernet-to-ATM switching with L3/L4 support
 - PPP interworking
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs).
 - Public key execution unit (PKEU) supporting the following:
 - RSA and Diffie-Hellman
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard execution unit (DEU)
 - DES, 3DES
 - Two key (K1, K2) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES

- Advanced encryption standard unit (AESU)
- Implements the Rijndael symmetric key cipher
- Key lengths of 128, 192, and 256 bits, two key
 - ECB, CBC, CCM, and counter modes
- ARC four execution unit (AFEU)
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either SHA or MD5 algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units via an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Storage/NAS XOR parity generation accelerator for RAID applications
- DDR SDRAM memory controller on the MPC8358E
 - Programmable timing supporting both DDR1 and DDR2 SDRAM
 - On the MPC8358E, the DDR bus can be configured as a 32- or 64-bit bus
 - 32- or 64-bit data interface, up to 266 MHz (for the MPC8358E) data rate
 - Four banks of memory, each up to 1 Gbyte
 - DRAM chip configurations from 64 Mbits to 1 Gigabit with $\times 8/\times 16$ data ports
 - Full ECC support
 - Page mode support (up to 16 simultaneous open pages for DDR1, up to 32 simultaneous open pages for DDR2)
 - Contiguous or discontinuous memory mapping
 - Read-modify-write support
 - Sleep mode support for self refresh SDRAM
 - Supports auto refreshing
 - Supports source clock mode
 - On-the-fly power management using CKE
 - Registered DIMM support
 - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
 - External driver impedance calibration
 - On-die termination (ODT)
- PCI interface
 - PCI Specification Revision 2.3 compatible

- Data bus widths:
 - Single 32-bit data PCI interface that operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- PCI host bridge capabilities on both interfaces
- PCI agent mode supported on PCI interface
- Support for PCI-to-memory and memory-to-PCI streaming
- Memory prefetching of PCI read accesses and support for delayed read transactions
- Support for posting of processor-to-PCI and PCI-to-memory writes
- On-chip arbitration, supporting five masters on PCI
- Support for accesses to all PCI address spaces
- Parity support
- Selectable hardware-enforced coherency
- Address translation units for address mapping between host and peripheral
- Dual address cycle supported when the device is the target
- Internal configuration registers accessible from PCI
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
 - Functional and programming compatibility with the MPC8260 interrupt controller
 - Support for 8 external and 35 internal discrete interrupt sources
 - Support for one external (optional) and seven internal machine checkstop interrupt sources
 - Programmable highest priority request
 - Four groups of interrupts with programmable priority
 - External and internal interrupts directed to communication processor
 - Redirects interrupts to external $\overline{\text{INTA}}$ pin when in core disable mode
 - Unique vector number for each interrupt source
- Dual industry-standard I²C interfaces
 - Two-wire interface

- Multiple master support
- Master or slave I²C mode support
- On-chip digital filtering rejects spikes on the bus
- System initialization data is optionally loaded from I²C-1 EPROM by boot sequencer embedded hardware
- DMA controller
 - Four independent virtual channels
 - Concurrent execution across multiple channels with programmable bandwidth control
 - All channels accessible by local core and remote PCI masters
 - Misaligned transfer capability
 - Data chaining and direct mode
 - Interrupt on completed segment and chain
 - DMA external handshake signals: $\overline{\text{DMA_DREQ}}[0:3]/\overline{\text{DMA_DACK}}[0:3]/\overline{\text{DMA_DONE}}[0:3]$. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
 - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
 - Periodic interrupt timer
 - Real-time clock
 - Software watchdog timer
 - Eight general-purpose timers
- IEEE Std. 1149.1™-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8358E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	-0.3 to 1.32	V	—
PLL supply voltage		AV_{DD}	-0.3 to 1.32	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	-0.3 to 2.75 -0.3 to 1.89	V	—
		DDR DDR2			
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	-0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I ² C, SPI, and JTAG I/O voltage		OV_{DD}	-0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV_{IN}	-0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	DDR DRAM reference	MV_{REF}	-0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	-0.3 to ($LV_{DD} + 0.3$)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I ² C, SPI, and JTAG signals	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	3, 5
	PCI	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	6
Storage temperature range		T_{STG}	-55 to 150	°C	—

Notes:

- Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- (M,L,O) V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	$1.2\text{ V} \pm 60\text{ mV}$	V	1
PLL supply voltage	AV_{DD}	$1.2\text{ V} \pm 60\text{ mV}$	V	1
DDR and DDR2 DRAM I/O supply voltage	GV_{DD}	$2.5\text{ V} \pm 125\text{ mV}$ $1.8\text{ V} \pm 90\text{ mV}$	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD0}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD1}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD2}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	—
PCI, local bus, DUART, system control and power management, I ² C, SPI, and JTAG I/O voltage	OV_{DD}	$3.3\text{ V} \pm 330\text{ mV}$	V	—
Junction temperature	T_J	0 to 105 -40 to 105	°C	—

Notes:

1. GV_{DD} , LV_{DD} , OV_{DD} , AV_{DD} , and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the overshoot and overshoot voltages at the interfaces of the device.

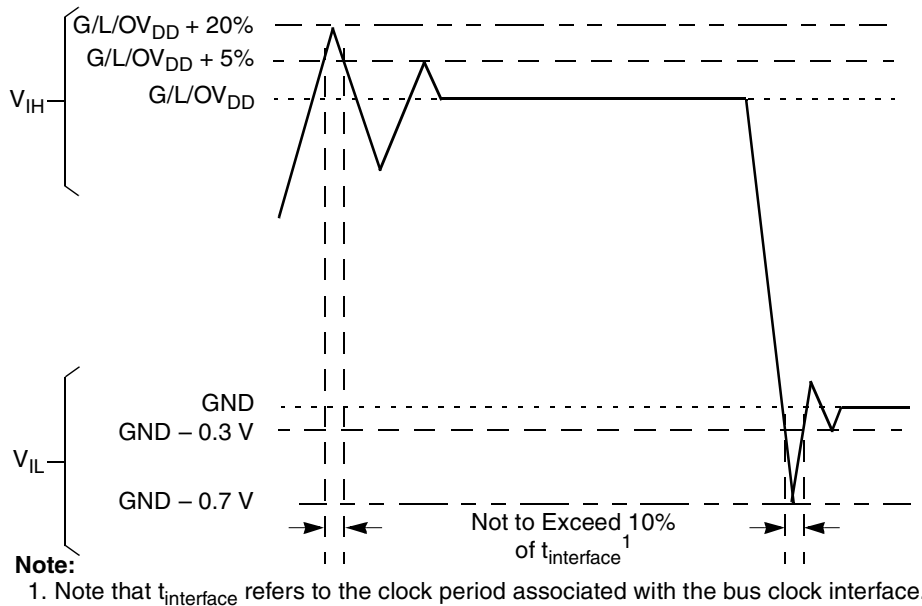


Figure 2. Overshoot/Undershoot Voltage for $G_{V_{DD}}/O_{V_{DD}}/L_{V_{DD}}$

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.

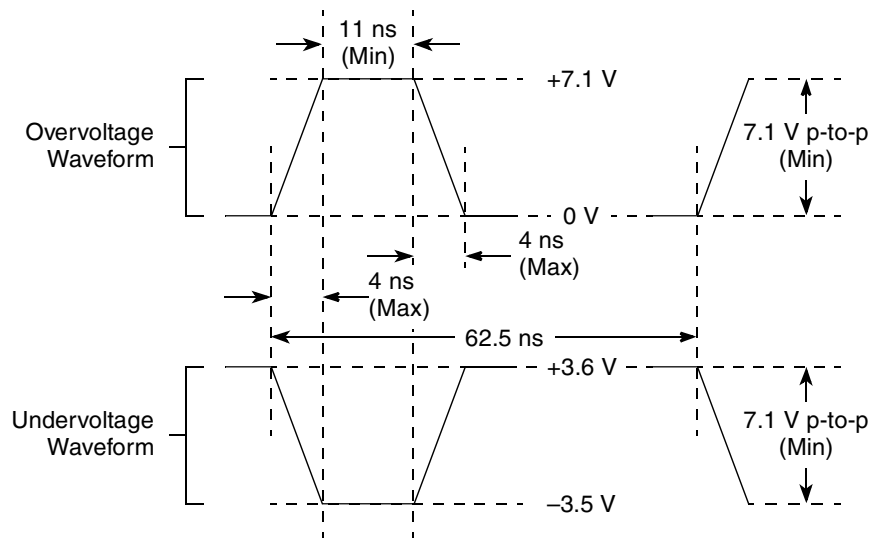


Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	$OV_{DD} = 3.3\text{ V}$
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode) ¹	$GV_{DD} = 2.5\text{ V}$
DDR2 signal	18 36 (half-strength mode) ¹	$GV_{DD} = 1.8\text{ V}$
10/100/1000 Ethernet signals	42	$LV_{DD} = 2.5/3.3\text{ V}$
DUART, system control, I ² C, SPI, JTAG	42	$OV_{DD} = 3.3\text{ V}$
GPIO signals	42	$OV_{DD} = 3.3\text{ V}$ $LV_{DD} = 2.5/3.3\text{ V}$

¹ DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8358E.

2.2.1 Power-Up Sequencing

MPC8358E does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD} , LV_{DD} , and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} , LV_{DD} , and OV_{DD}) and assert $\overline{PORESET}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 4.

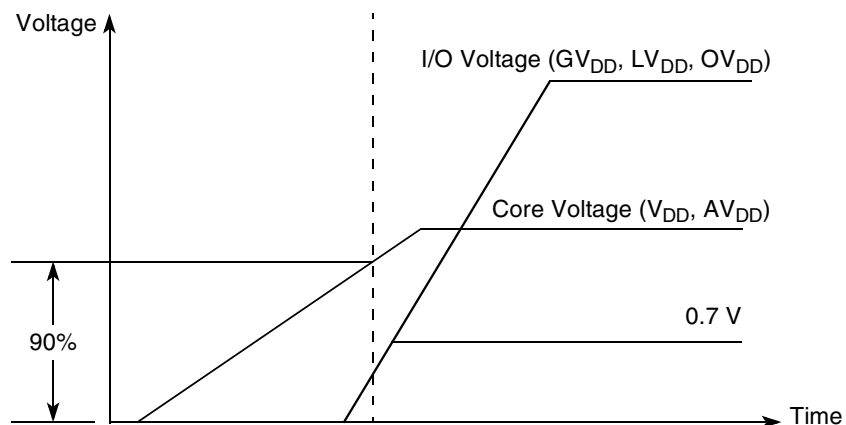


Figure 4. Power Sequencing Example

I/O voltage supplies (GV_{DD} , LV_{DD} , and OV_{DD}) do not have any ordering requirements with respect to one another.

2.2.2 Power-Down Sequencing

The MPC8358E does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation values are shown in [Table 4](#).

Table 4. MPC8358E PBGA Core Power Dissipation¹

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	266	2.2	2.3	W	2, 3, 4
400	266	266	2.4	2.5	W	2, 3, 4
400	266	400	2.5	2.6	W	2, 3, 4

Notes:

1. The values do not include I/O supply power (OV_{DD} , LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see [Table 5](#).
2. Typical power is based on a voltage of $V_{DD} = 1.2$ V, a junction temperature of $T_J = 105^\circ\text{C}$, and a Dhrystone benchmark application.
3. Thermal solutions will likely need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of $V_{DD} = 1.2$ V, WC process, a junction $T_J = 105^\circ\text{C}$, and an artificial smoke test.

Table 5 shows the estimated typical I/O power dissipation for the device.

Table 5. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V R _s = 20 Ω R _t = 50 Ω 2 pairs of clocks	200 MHz, 1x32 bits	0.3	0.46	—	—	—	W	—
	200 MHz, 1x64 bits	0.4	0.58	—	—	—	W	—
	200 MHz, 2x32 bits	0.6	0.92	—	—	—	W	—
	266 MHz, 1x32 bits	0.35	0.56	—	—	—	W	—
	266 MHz, 1x64 bits	0.46	0.7	—	—	—	W	—
	266 MHz, 2x32 bits	0.7	1.11	—	—	—	W	—
Local Bus I/O Load = 25 pF 3 pairs of clocks	133 MHz, 32 bits	—	—	0.22	—	—	W	—
	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	—
	50 MHz, 32 bits	—	—	0.09	—	—	W	—
PCI I/O Load = 30 pF	33 MHz, 32 bits	—	—	0.05	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000 Ethernet I/O Load = 20 pF	MII or RMII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.04	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	—	—	—	0.1	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8358E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD}; fall time refers to transitions from 90% to 10% of V_{DD}.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

Table 6. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	-0.3	0.4	V
CLKIN input current	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 10	μA
PCI_SYNC_IN input current	$0\text{ V} \leq V_{IN} \leq 0.5\text{V}$ or $OV_{DD} - 0.5\text{V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 10	μA
PCI_SYNC_IN input current	$0.5\text{ V} \leq V_{IN} \leq OV_{DD} - 0.5\text{ V}$	I_{IN}	—	± 100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	± 150	ps	4, 5

Notes:

- Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

4.3 Gigabit Reference Clock Input Timing

Table 8 provides the Gigabit reference clocks (GTX_CLK125) AC timing specifications.

Table 8. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with $V_{DD} = 2.5 \pm 0.125$ mV/ $3.3 \text{ V} \pm 165$ mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
GTX_CLK rise and fall time $V_{DD} = 2.5$ V $V_{DD} = 3.3$ V	t_{G125R}/t_{G125F}	—	—	0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t_{G125H}/t_{G125L}	45 47	—	55 53	%	2
GTX_CLK125 jitter	—	—	—	± 150	ps	2

Notes:

- Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for $V_{DD} = 2.5$ V and from 0.6 and 2.7 V for $V_{DD} = 3.3$ V.
- GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See Section 8.2.2, "MII AC Timing Specifications," Section 8.2.3, "RMII AC Timing Specifications," and Section 8.2.5, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8358E.

5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the device.

Table 9. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	—	—	± 10	μ A
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V

Table 9. RESET Pins DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

Notes:

1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 RESET AC Electrical Characteristics

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. [Table 10](#) provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{\text{PCI_SYNC_IN}}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

1. $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is in PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 provides the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See [Section 22, “Clocking,”](#) for more information.

5.3 QUICC Engine Block Operating Frequency Limitations

This section specifies the limits of the AC electrical characteristics for the operation of the QUICC Engine block’s communication interfaces.

NOTE

The settings listed below are required for correct hardware interface operation. Each protocol by itself requires a minimal QUICC Engine block operating frequency setting for meeting the performance target. Because the performance is a complex function of all the QUICC Engine block settings, the user should make use of the QUICC Engine block performance utility tool provided by Freescale to validate their system.

Table 12 lists the maximal QUICC Engine block I/O frequencies and the minimal QUICC Engine block core frequency for each interface.

Table 12. QUICC Engine Block Operating Frequency Limitations

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency ¹ (MHz)	Notes
Ethernet Management: MDC/MDIO	10 (max)	10	20	—
MII	25 (typ)	100	50	—
RMII	50 (typ)	100	50	—
GMII/RGMII/TBI/RTBI	125 (typ)	1000	250	—
SPI (master/slave)	10 (max)	10	20	—
UCC through TDM	50 (max)	70	8 × F	2
MCC	25 (max)	16.67	16 × F	2, 4
UTOPIA L2	50 (max)	800	2 × F	2
POS-PHY L2	50 (max)	800	2 × F	2
HDLC bus	10 (max)	10	20	—
HDLC/transparent	50 (max)	50	8/3 × F	2, 3

Table 12. QUICC Engine Block Operating Frequency Limitations (continued)

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency ¹ (MHz)	Notes
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	—
USB	48 (ref clock)	12	96	—

Notes:

1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.
3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8358E.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when $GV_{DD}(\text{typ}) = 1.8 \text{ V}$.

Table 13. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(\text{typ}) = 1.8 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	—	± 10	μA	4
Output high current ($V_{OUT} = 1.420 \text{ V}$)	I_{OH}	-13.4	—	mA	—
Output low current ($V_{OUT} = 0.280 \text{ V}$)	I_{OL}	13.4	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	± 10	μA	—

Table 13. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 1.8\text{ V}$ (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input current ($0\text{ V} \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REF} is expected to equal $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 14 provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 14. DDR2 SDRAM Capacitance for $GV_{DD}(typ)=1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, \overline{DQS}	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, \overline{DQS}	C_{DIO}	—	0.5	pF	1

Note:

- This parameter is sampled. $GV_{DD} = 1.8\text{ V} \pm 0.090\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) of the device when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 15. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	—	± 10	μA	4
Output high current ($V_{OUT} = 1.95\text{ V}$)	I_{OH}	-15.2	—	mA	—
Output low current ($V_{OUT} = 0.35\text{ V}$)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	± 10	μA	—
Input current ($0\text{ V} \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 16 provides the DDR capacitance when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 16. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5\text{ V} \pm 0.125\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM interface when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 17. DDR2 SDRAM Input AC Timing Specifications for $GV_{DD}(typ) = 1.8\text{ V}$

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V	—

Table 18 provides the input AC timing specifications for the DDR SDRAM interface when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if $0 \leq n \leq 7$) or ECC (MECC[{0...7}] if $n = 8$).

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

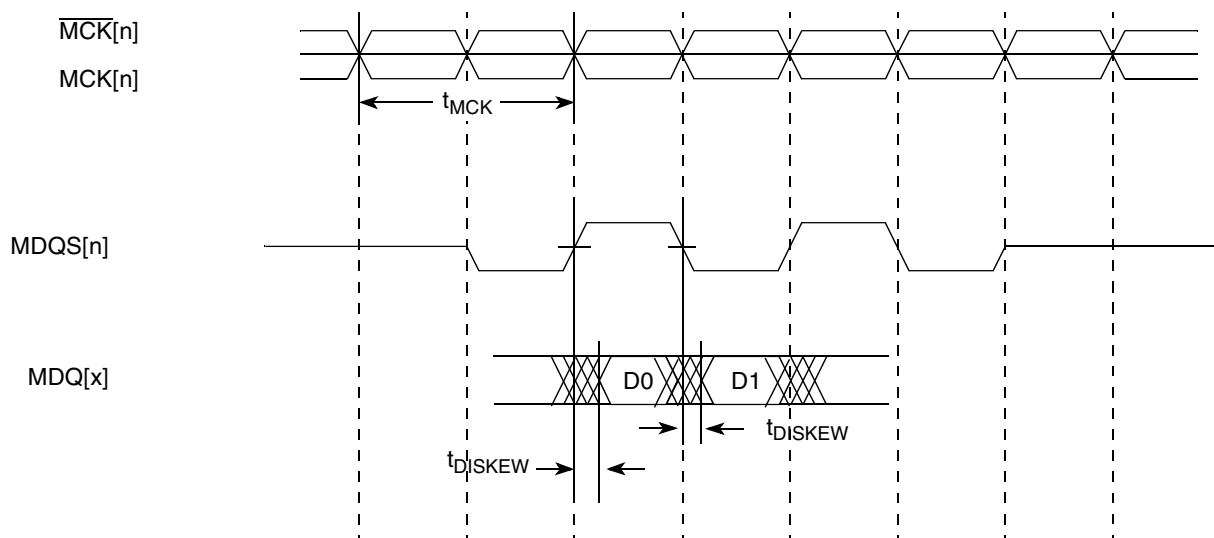
 At recommended operating conditions with GV_{DD} of $(1.8 \text{ or } 2.5 \text{ V}) \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
MDQS—MDQ/MECC input skew per byte 266 MHz 200 MHz	t_{DISKEW}	-1125 -1250	1125 1250	ps	1, 2

Notes:

- AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
- Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if $0 \leq n \leq 7$ or ECC (MECC[{0...7}] if $n = 8$).

Figure 5 shows the input timing diagram for the DDR controller.


Figure 5. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 and Table 21 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

 At recommended operating conditions with GV_{DD} of $(1.8 \text{ V or } 2.5 \text{ V}) \pm 5\%$.

Parameter ⁸	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 266 MHz 200 MHz	t_{AOSKEW}	-1.1 -1.2	0.3 0.4	ns	3

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) \pm 5%.

Parameter ⁸	Symbol ¹	Min	Max	Unit	Notes
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	2.8 3.5	—	ns	4
ADDR/CMD output hold with respect to MCK 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t_{DDKHAX}	2.6 2.8 3.5	—	ns	4
$\overline{MCS}(n)$ output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	2.8 3.5	—	ns	4
$\overline{MCS}(n)$ output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	2.7 3.5	—	ns	4
MCK to MDQS	t_{DDKMHM}	-0.75	0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	1.0 1.2	—	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	1.0 1.2	—	ns	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	7

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

 At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) $\pm 5\%$.

Parameter ⁸	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	-0.6	0.9	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/\overline{MCK} referenced measurements are made from the crossing of the two signals ± 0.1 V.
- In the source synchronous mode, MCK/\overline{MCK} can be shifted in $\frac{1}{4}$ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/\overline{MCK} , \overline{MCS} , and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.
- Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Figure 6 shows the DDR SDRAM output timing for address skew with respect to any MCK.

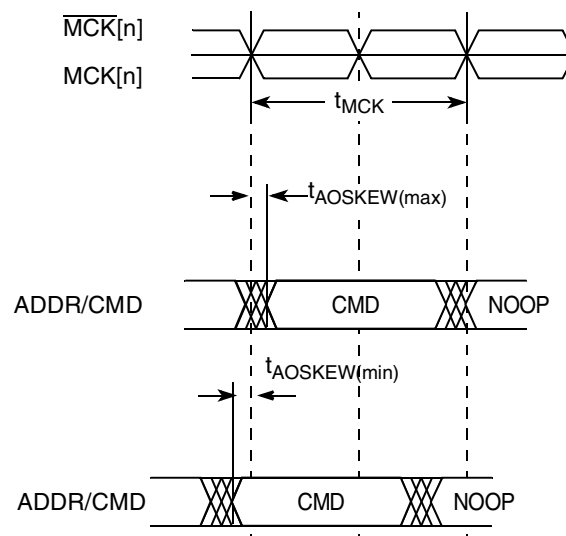

Figure 6. Timing Diagram for t_{AOSKEW} Measurement

Figure 7 provides the AC test load for the DDR bus.

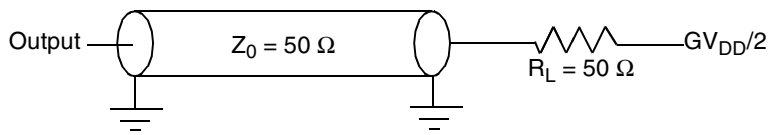


Figure 7. DDR AC Test Load

Table 21. DDR and DDR2 SDRAM Measurement Conditions

Symbol	DDR	DDR2	Unit	Notes
V_{TH}	$MV_{REF} \pm 0.31 V$	$MV_{REF} \pm 0.25 V$	V	1
V_{OUT}	$0.5 \times GV_{DD}$	$0.5 \times GV_{DD}$	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Figure 8 shows the DDR SDRAM output timing diagram for source synchronous mode.

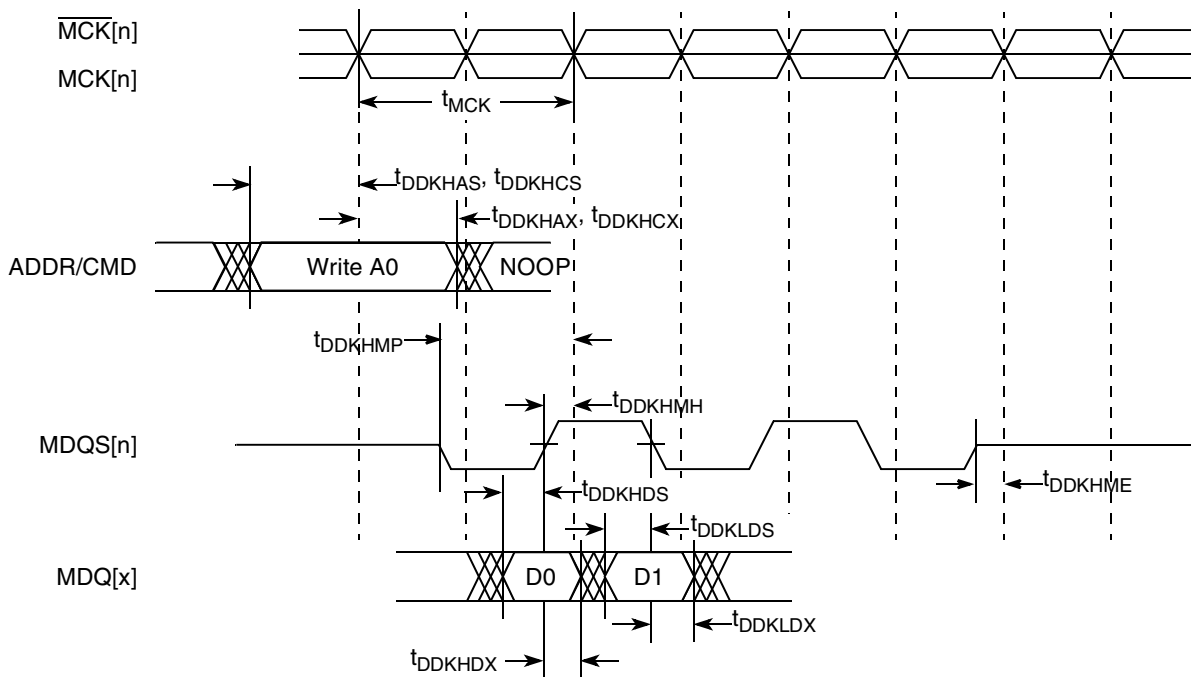


Figure 8. DDR SDRAM Output Timing Diagram for Source Synchronous Mode

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8358E.

7.1 DUART DC Electrical Characteristics

Table 22 provides the DC electrical characteristics for the DUART interface of the device.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V	—
Low-level input voltage OV_{DD}	V_{IL}	-0.3	0.8	V	—
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.4$	—	V	—
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V	—
Input current ($0 V \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	1

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 23 provides the AC timing parameters for the DUART interface of the device.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:

- Actual attainable baud rate will be limited by the latency of interrupt processing.
- The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.