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Freescale Semiconductor
Technical Data

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MPC8377E PowerQUICC II Pro Processor Hardware Specifications

This document provides an overview of the MPC8377E PowerQUICC II Pro processor features, including a block diagram showing the major functional components. This chip is a cost-effective, low-power, highly integrated host processor that addresses the requirements of several printing and imaging, consumer, and industrial applications, including main CPUs and I/O processors in printing systems, networking switches and line cards, wireless LANs (WLANs), network access servers (NAS), VPN routers, intelligent NIC, and industrial controllers. This chip extends the PowerQUICC family, adding higher CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and package size.

Contents

1 Overview

This chip incorporates the e300c4s core, which includes 32 KB of L1 instruction and data caches and on-chip memory management units (MMUs). The device offers two enhanced three-speed 10, 100, 1000 Mbps Ethernet interfaces, a DDR1/DDR2 SDRAM memory controller, a flexible, a 32-bit local bus controller, a 32-bit PCI controller, an optional dedicated security engine, a USB 2.0 dual-role controller, a programmable interrupt

controller, dual I^2C controllers, a 4-channel DMA controller, an enhanced secured digital host controller, and a general-purpose I/O port. This figure shows the block diagram of the chip.

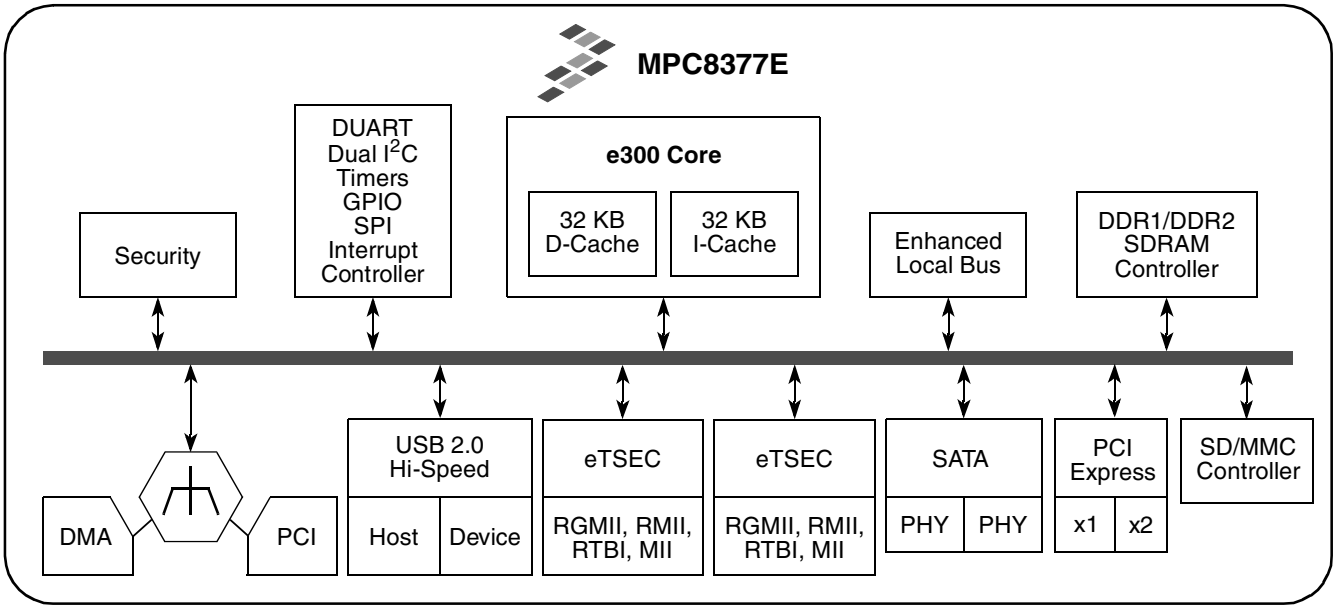


Figure 1. MPC8377E Block Diagram and Features

The following features are supported in the chip:

- e300c4s core built on Power Architecture® technology with 32 KB instruction cache and 32 KB data cache, a floating point unit, and two integer units
- DDR1/DDR2 memory controller supporting a 32/64-bit interface
- Peripheral interfaces, such as a 32-bit PCI interface with up to 66-MHz operation
- 32-bit local bus interface running up to 133-MHz
- USB 2.0 (full/high speed) support
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration
- Optional security engine provides acceleration for control and data plane security protocols

The optional security engine (SEC 3.0) is noted with the extension “E” at the end. It allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In addition to the security engine, new high-speed interfaces, such as PCI Express and SATA are included. This table compares the differences between MPC837xE derivatives and provides the number of ports available for each interface.

Table 1. High-Speed Interfaces on the MPC8377E, MPC8378E, and MPC8379E

Descriptions	MPC8377E	MPC8378E	MPC8379E
SGMII	0	2	0
PCI Express®	2	2	0
SATA	2	0	4

1.1 DDR Memory Controller

The DDR1/DDR2 memory controller includes the following features:

- Single 32- or 64-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 400-MHz data rate
- Support up to 4 chip selects
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with ×8/×16/×32 data ports (no direct ×4 support)
- Support for up to 32 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.2 USB Dual-Role Controller

The USB controller includes the following features:

- Supports USB on-the-go mode, including both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Complies with *USB Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation; low-speed operation is supported only in host mode
- Supports UTMI + low pin interface (ULPI)

1.3 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The eTSECs include the following features:

- Two enhanced Ethernet interfaces can be used for RGMII/MII/RMII/RTBI
- Two controllers conform to IEEE Std 802.3®, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3au, IEEE 802.3ab, and IEEE Std 1588™ standards
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status

1.4 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.5 Power Management Controller (PMC)

The power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI Power Management 1.2 D0, D1, D2, and D3hot states
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports Wake-on-LAN (Magic Packet), USB, GPIO, and PCI (PME input as host)
- Supports MPC8349E backward-compatibility mode

1.6 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the device to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.7 DMA Controller, Dual I^2C, DUART, Enhanced Local Bus Controller (eLBC), and Timers

The device provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two I^2C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The main component of the enhanced local bus controller (eLBC) is its memory controller, which provides a seamless interface to many types of memory devices and peripherals. The memory controller is responsible for controlling eight memory banks shared by a NAND Flash control machine (FCM), a general-purpose chip-select machine (GPCM), and up to three user-programmable machines (UPMs). As such, it supports a minimal glue logic interface to SRAM, EPROM, NOR Flash EPROM, NAND Flash, EPROM, burstable RAM, regular DRAM devices, extended data output DRAM devices, and other peripherals. The eLBC external address latch enable (LALE) signal allows multiplexing of addresses with data signals to reduce the device pin count.

The enhanced local bus controller also includes a number of data checking and protection features, such as data parity generation and checking, write protection, and a bus monitor to ensure that each bus cycle is terminated within a user-specified period. The local bus can operate at up to 133 MHz.

The system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

1.8 Security Engine

The optional security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.9 PCI Controller

The PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting 5 external masters on PCI
- Selectable hardware-enforced coherency

1.10 PCI Express Controller

The PCI Express controller includes the following features:

- PCI Express 1.0a compatible
- Two ×1 links or one ×2 link width
- Auto-detection of number of connected lanes
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated four channel descriptor-based DMA engine per interface

1.11 Serial ATA (SATA) Controllers

The serial ATA (SATA) controllers have the following features:

- Supports *Serial ATA Rev 2.5 Specification*
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot Plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- Port multiplier support
- SATA 1.5 and 3.0 Gb/s operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - — Far end/near end loopback
  - — Failed CRC error reporting
  - — Increased ALIGN insertion rates
- Scrambling and CONT override

1.12 Enhanced Secured Digital Host Controller (eSDHC)

The enhanced SD host controller (eSDHC) has the following features:

- Conforms to *SD Host Controller Standard Specification, Rev 2.0* with Test Event register support.
- Compatible with the *MMC System Specification, Rev 4.0*
- Compatible with the *SD Memory Card Specification, Rev 2.0*, and supports High Capacity SD memory cards
- Compatible with the *SDIO Card Specification Rev, 1.2*
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, MMC 4x, and RS-MMC cards
- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD and SDIO modes, 1-/4-bit MMC modes
- Supports internal DMA capabilities

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the chip. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Note
Core supply voltage	V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage (e300 core, eLBC, and system)	AV_{DD}	–0.3 to 1.1	V	—
DDR1 and DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage	LV_{DD}[1,2]	–0.3 to 3.63	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—
Local bus	LBV_{DD}	–0.3 to 3.63	V	—
SerDes	L[1,2]_nV_{DD}	–0.3 to 1.1	V	6

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 4
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 4
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	—
	PCI, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 4, 5
	Local Bus	LB_{IN}	–0.3 to (LBV_{DD} + 0.3)	V	—
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. Overshoot/undershoot by OV_{IN} on the PCI interface does not comply to the *PCI Electrical Specification* for 3.3-V operation, as shown in Figure 2.
6. L[1,2]_$n$$V_{DD}$ includes $SDAV_{DD\_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

2.1.2 Power Supply Voltage Specification

This table provides recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

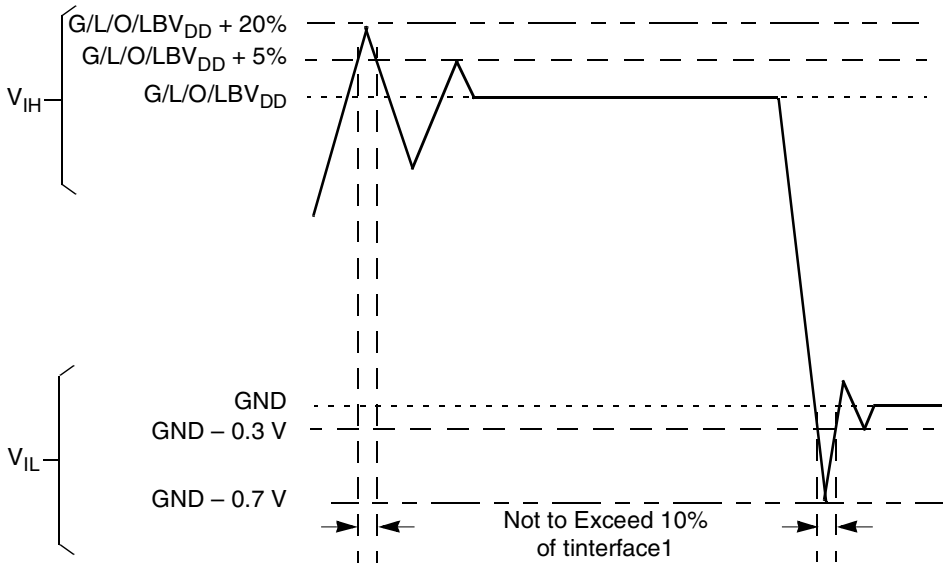
Characteristic		Symbol	Recommended Value	Unit	Note
Core supply voltage	up to 667 MHz	V_{DD}	1.0 ± 50 mV	V	1
	800 MHz		1.05 ± 50 mV	V	1
PLL supply voltage (e300 core, eLBC and system)	up to 667 MHz	AV_{DD}	1.0 ± 50 mV	V	1, 2
	800 MHz		1.05 ± 50 mV	V	1, 2
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Three-speed Ethernet I/O, MII management voltage		LV_{DD}[1,2]	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	1
Local Bus		LBV_{DD}	1.8 V ± 90 mV 2.5 V ± 125 mV 3.3 V ± 165 mV	V	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
SerDes	up to 667 MHz	L[1,2]_nV_{DD}	1.0 ± 50 mV	V	1, 3
	800 MHz		1.05 V ± 50 mV	V	1, 3
Operating temperature range	commerical	T_a T_j	T_a=0 (min)— T_j=125 (max)	°C	—
	extended temperature	T_a T_j	T_a=–40 (min)— T_j=125 (max)	°C	—

Notes:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. AV_{DD} is the input to the filter discussed in Section 25.1, "PLL Power Supply Filtering," and is not necessarily the voltage at the AVDD pin.
3. L[1,2]_nV_{DD}, $SDAV_{DD\_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



Note:
1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the *PCI Rev. 2.3 Specification* (Section 4.2.2.3).

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}

2.1.3 chipOutput Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type[1]	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	45	LBV_{DD} = 2.5 V, 3.3 V
	40	LBV_{DD} = 1.8 V
PCI signals	25	OV_{DD} = 3.3 V
DDR1 signal	18	GV_{DD} = 2.5 V
DDR2 signal	18	GV_{DD} = 1.8 V
eTSEC 10/100/1000 signals	45	LV_{DD} = 2.5 V, 3.3 V
DUART, system control, I^2C, JTAG, SPI, and USB	45	OV_{DD} = 3.3 V
GPIO signals	45	OV_{DD} = 3.3 V

Note:
1. Specialized SerDes output capabilities are described in the relevant sections of these specifications (such as PCI Express and SATA)

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current. To avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltages (V_{DD} and AV_{DD}) before the I/O voltages and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. V_{DD} and AV_{DD} must reach 90% of their nominal value before GV_{DD}, LV_{DD}, and OV_{DD} reach 10% of their value, see the following figure. I/O

voltage supplies—GV_{DD}, LV_{DD}, and OV_{DD}—do not have any ordering requirements with respect to one another.

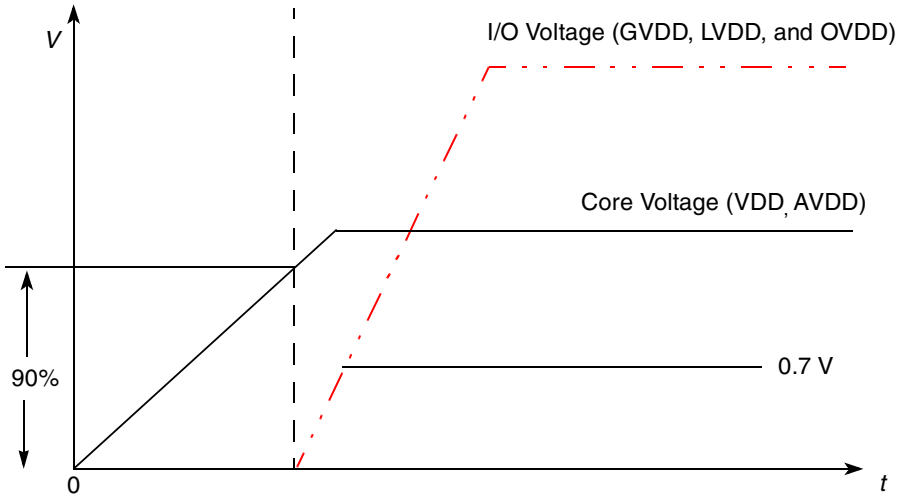


Figure 3. Power-Up Sequencing Example

Note that the SerDes power supply (L[1,2]_nV_{DD}) should follow the same timing as the core supply (V_{DD}).

The device does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation for the chip device is shown in this table.

Table 5. Power Dissipation [1]

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
333	333	1.45	1.9	3.2	3.8
	167	1.45	1.8	3.0	3.6
400	400	1.45	2.0	3.3	4.0
	266	1.45	1.9	3.1	3.8
450	300	1.45	2.0	3.2	3.8
	225	1.45	1.9	3.1	3.7
500	333	1.45	2.0	3.3	3.9
	250	1.45	1.9	3.2	3.8
533	355	1.45	2.0	3.3	4.0
	266	1.45	2.0	3.2	3.9

Table 5. Power Dissipation [1] (continued)

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
600	400	1.45	2.1	3.4	4.1
	300	1.45	2.0	3.3	4.0
667	333	1.45	2.1	3.3	4.1
	266	1.45	2.0	3.3	3.9
800	400	1.45	2.5	3.8	4.3

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
3. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
4. Maximum power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, worst case process, and running an artificial smoke test.

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	L[1,2]_$n$$V_{DD}$ (1.0 V)	Unit	Comments
DDR I/O 65% utilization 2 pair of clocks	200 MHz data rate, 32-bit	0.28	0.35	—	—	—	—	W	—
	200 MHz data rate, 64-bit	0.41	0.49	—	—	—	—	W	
	266 MHz data rate, 32-bit	0.31	0.4	—	—	—	—	W	
	266 MHz data rate, 64-bit	0.46	0.56	—	—	—	—	W	
	300 MHz data rate, 32-bit	0.33	0.43	—	—	—	—	W	
	300 MHz data rate, 64-bit	0.48	0.6	—	—	—	—	W	
	333 MHz data rate, 32-bit	0.35	0.45	—	—	—	—	W	
	333 MHz data rate, 64-bit	0.51	0.64	—	—	—	—	W	
	400 MHz data rate, 32-bit	0.38	—	—	—	—	—	W	
	400 MHz data rate, 64-bit	0.56	—	—	—	—	—	W	

Table 6. Typical I/O Power Dissipation (continued)

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	$L[1,2]\_nV_{DD}$ (1.0 V)	Unit	Comments
PCI I/O Load = 30 pf	33 MHz, 32-bit	—	—	0.04	—	—	—	W	—
	66 MHz, 32-bit	—	—	0.07	—	—	—	W	
Local Bus I/O Load = 25 pf	167 MHz, 32-bit	0.09	0.17	0.29	—	—	—	W	—
	133 MHz, 32-bit	0.07	0.14	0.24	—	—	—	W	
	83 MHz, 32-bit	0.05	0.09	0.15	—	—	—	W	
	66 MHz, 32-bit	0.04	0.07	0.13	—	—	—	W	
	50 MHz, 32-bit	0.03	0.06	0.1	—	—	—	W	
eTSEC I/O Load = 25 pf	MII or RMII	—	—	—	0.02	—	—	W	Multiply by number of interfaces used.
	RGMII or RTBI	—	—	—	—	0.05	—	W	—
USB (60MHz Clock)	12 Mbps	—	—	0.01	—	—	—	W	—
	480 Mbps	—	—	0.2	—	—	—	W	
SerDes	per lane	—	—		—	—	0.029	W	—
Other I/O	—	—	—	0.01	—	—	—	W	—

Note: The values given are for typical, and not worst case, switching.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the chip. Note that the PCI_CLK/PCI_SYNC_IN signal or CLKIN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. CLKIN is used when the device is in host mode.

4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_CLK) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit	Note
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V	1
Input low voltage	—	V_{IL}	–0.3	0.4	V	1
CLKIN Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 10	μA	—
PCI_CLK Input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA	—

Note:
1. In PCI agent mode, this specification does not comply with *PCI 2.3 Specification*.

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.666	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	40	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	± 150	ps	4, 5

Notes:
1. **Caution:** The system, core and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter-short term and long term-and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread on CLKIN/PCI_CLK up to 60 KHz.

4.3 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 9. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 47	—	 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.2, "RGMII and RTBI AC Timing Specifications," for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the chip.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

Table 10. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	± 30	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:

- This table applies for pins $\overline{\text{PORESET}}$ and $\overline{\text{HRESET}}$. The $\overline{\text{PORESET}}$ is input pin, thus stated output voltages are not relevant.
- $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pin, thus V_{OH} is not relevant for these pins.

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications of the device.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_CLK when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to start driving functional output signals multiplexed with the POR configuration signals with respect to the negation of HRESET	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:3], CFG_LBMUX, and CFG_CLKIN_DIV.

Table 12 provides the PLL lock times.

Table 12. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

Note:

- The device guarantees the PLL lock if the clock settings are within spec range. The core clock also depends on the core PLL ratio. See Section 23, “Clocking,” for more information.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR1 SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.140	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.140	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.40 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.3 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.18	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.9 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.38 V)	I_{OL}	15.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 16 provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 17. Current Draw Characteristics for MV_{REF}

Parameter	Symbol	Min	Typ	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}				μA	1, 2
DDR1		—	250	600		
DDR2		—	150	400		

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to the stated maximum current.
2. This current is divided equally between MVREF1 and MVREF2, where half the current flows through each pin.

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GVDD(typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

This table provides the input AC timing specifications for the DDR1 SDRAM when GV_{DD}(typ) = 2.5 V.

Table 19. DDR1 SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V

This table provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 20. DDR1 and DDR2 SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS-MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
400 MHz data rate		–500	500		3
333 MHz data rate		–750	750		—
266 MHz data rate		–750	750		—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS*n* and any corresponding bit that will be captured with MDQS*n*. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm[T/4 - |t_{CISKEW}|]$ where T is the MCK clock period and $|t_{CISKEW}|$ is the absolute value of t_{CISKEW}.
3. This specification applies only to DDR2 interface.

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

This table shows the DDR1 and DDR2 SDRAM output AC timing specifications.

Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK*n* cycle time, MCK*n*/$\overline{\text{MCK}n}$ crossing	t_{MCK}	5	10	ns	2
ADDR/CMD output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
ADDR/CMD output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
$\overline{\text{MCS}n}$ output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
$\overline{\text{MCS}n}$ output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
MCK to MDQS skew	t_{DDKHMH}	–0.6	0.6	ns	4, 8
MDQ//MDM output setup with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDS}, t_{DDKLDS}	 550 800 1100 1200	 — — — —	ps	5, 8
MDQ//MDM output hold with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDX}, t_{DDKLDX}	 700 800 1100 1200	 — — — —	ps	5, 8
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6, 8

Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol[1]	Min	Max	Unit	Note
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6, 8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in Note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8379E PowerQUICC II Pro Host Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data MDQ, ECC, or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK*n* at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in Note 1.
7. Clock Control register is set to adjust the memory clocks by 1/2 the applied cycle.
8. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

The minimum frequency for DDR2 is 250 MHz data rate (125 MHz clock), 167 MHz data rate (83 MHz clock) for DDR1. This figure shows the DDR1 and DDR2 SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

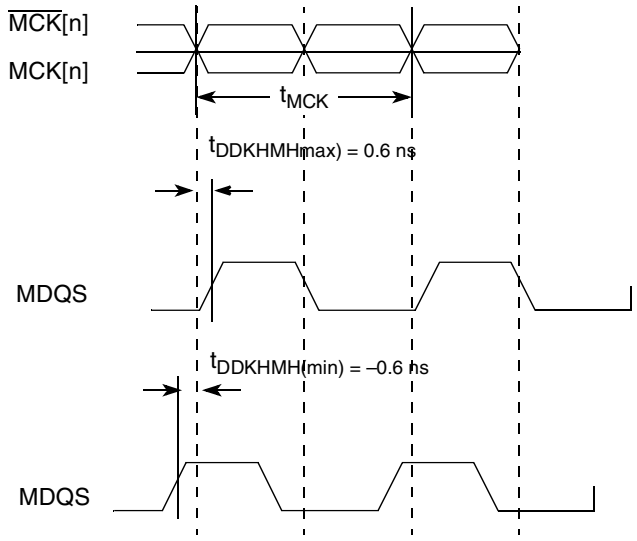


Figure 4. DDR Timing Diagram for t_{DDKHMH}

This figure shows the DDR1 and DDR2 SDRAM output timing diagram.

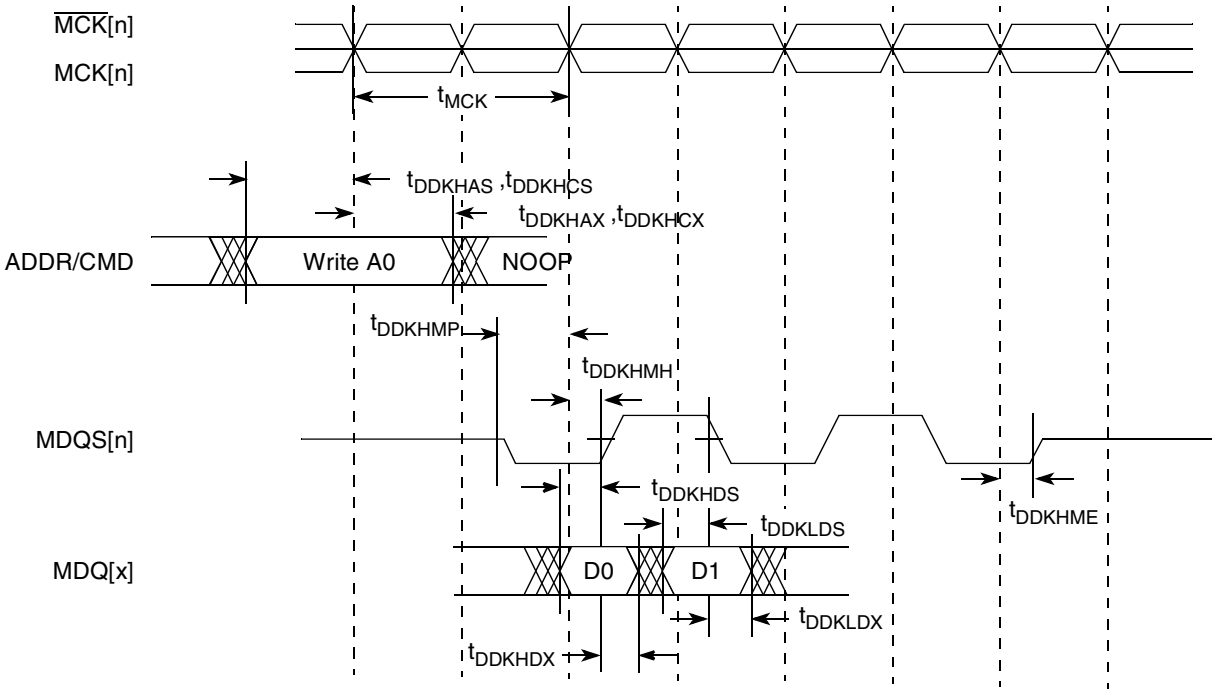


Figure 5. DDR1 and DDR2 SDRAM Output Timing Diagram

This figure provides AC test load for the DDR bus.

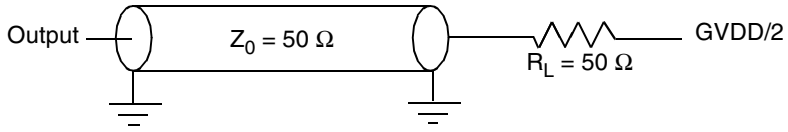


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V

Table 22. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current, (0 V ≤V_{IN} ≤ OV_{DD})	I_{IN}	—	±30	µA

Note: The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2.

7.2 DUART AC Electrical Specifications

this table provides the AC timing parameters for the DUART interface of the device.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII/RTBI/RMII DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

8.1.1 MII, RMII, RGMII, and RTBI DC Electrical Characteristics

MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals in Table 25 are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 3.3 V	LV_{DD1} LV_{DD2}	3.13	3.47	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	30	μA	1
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

Table 25. RGMII and RTBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 2.5 V	LV_{DD1} LV_{DD2}	2.37	2.63	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.7	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	–20	μA	1
Input low current (V_{IN} = GND)	I_{IL}	–20	—	μA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

8.2 MII, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RGMII, RMII, and RTBI are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 26. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

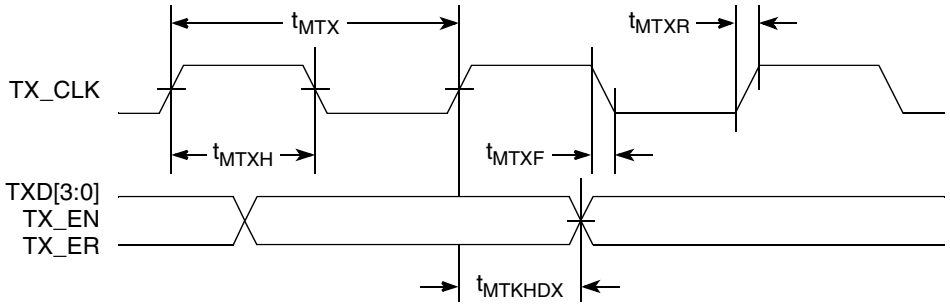


Figure 7. MII Transmit AC Timing Diagram