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Technical Data

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MPC8533E PowerQUICC III Integrated Processor Hardware Specifications

1 MPC8533E Overview

This section provides a high-level overview of MPC8533E features. Figure 1 shows the major functional units within the device.

1.1 Key Features

The following list provides an overview of the device feature set:

- High-performance, 32-bit core enhanced by resources for embedded cores defined by the Power ISA, and built on Power Architecture® technology:
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
  - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

Contents

- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte–4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 256-Kbyte L2 cache/SRAM
  - Flexible configuration
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both.
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
    - 1, 2, or 4 ways can be configured for stashing only.
  - Eight-way set-associative cache organization (32-byte cache lines)
  - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  - Global locking and flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be flash cleared separately.
  - SRAM features include the following:
    - I/O devices access SRAM regions by marking transactions as snoopable (global).
    - Regions can reside at any aligned location in the memory map.
    - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 36-bit address space.
  - Inbound and outbound ATMUs map to larger external address spaces.
    - Three inbound windows plus a configuration window on PCI and PCI Express
    - Four outbound windows plus default translation for PCI and PCI Express
- DDR/DDR2 memory controller
  - Programmable timing supporting DDR and DDR2 SDRAM
  - 64-bit data interface

- Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
- DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
- Full ECC support
- Page mode support
  - Up to 16 simultaneous open pages for DDR
  - Up to 32 simultaneous open pages for DDR2
- Contiguous or discontiguous memory mapping
- Sleep mode support for self-refresh SDRAM
- On-die termination support when using DDR2
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL_2 compatible I/O (1.8-V SSTL_1.8 for DDR2)

- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture.
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters that can generate interrupts
  - Supports a variety of other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing.
  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
  - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units via an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 2048 bits
    - Elliptic curve cryptography with F_2m and F(p) modes and programmable field size up to 511 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES

  - Two key (K1, K2, K1) or three key (K1, K2, K3)
  - ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
  - Implements the Rijndael symmetric key cipher
  - ECB, CBC, CTR, and CCM modes
  - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- MDEU—message digest execution unit
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- KEU—Kasumi execution unit
  - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications

- Dual I^2C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data bus operating at up to 133 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
  - Two protocol engines available on a per chip select basis:

  - General-purpose chip select machine (GPCM)
  - Three user programmable machines (UPMs)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)

- Two enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Two IEEE Std 802.3™, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, and IEEE 802.3ab-compliant controllers
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII.
    - 10/100 Mbps full- and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII.
  - Flexible configuration for multiple PHY interface configurations.
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over
    - Up to 16 exact-match MAC addresses supported

  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- PCI controller
  - PCI 2.2 compatible
  - One 32-bit PCI port with support for speeds from 16 to 66 MHz
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes
  - PCI 3.3-V compatible
  - Selectable hardware-enforced coherency

- Three PCI Express interfaces
  - Two ×4 link width interfaces and one ×1 link width interface
  - PCI Express 1.0a compatible
  - Auto-detection of number of connected lanes
  - Selectable operation as root complex or endpoint
  - Both 32- and 64-bit addressing
  - 256-byte maximum payload size
  - Virtual channel 0 only
  - Traffic class 0 only
  - Full 64-bit decode with 32-bit wide windows
- Power management
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compliant, JTAG boundary scan
- 783 FC-PBGA package

Figure 1 shows the MPC8533E block diagram.

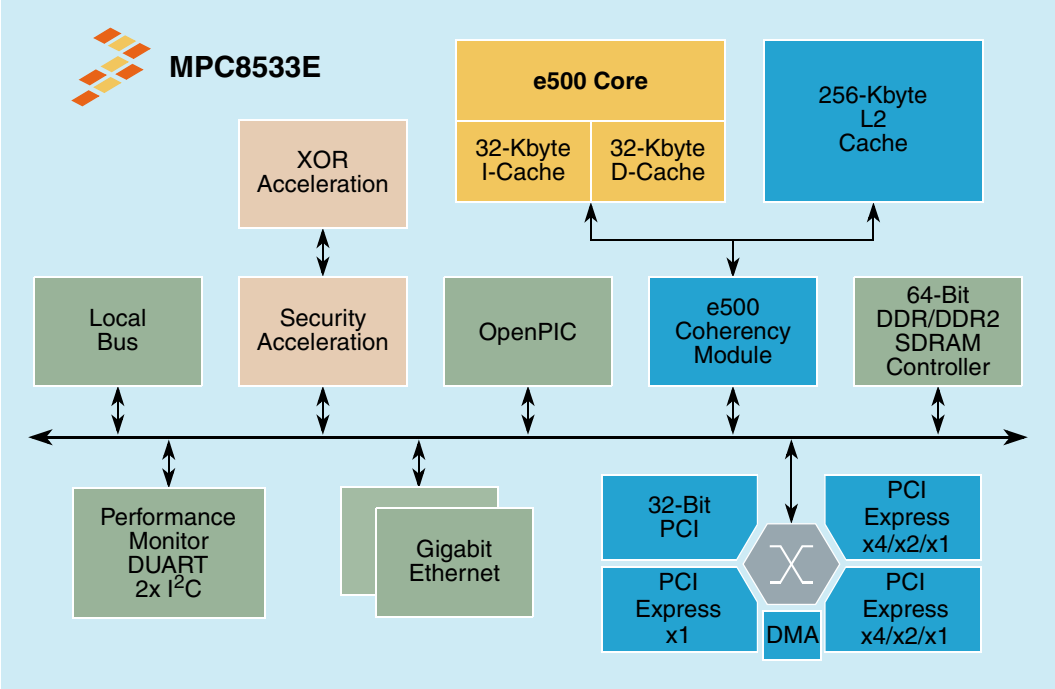


Figure 1. MPC8533E Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8533E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage	AV_{DD}	–0.3 to 1.1	V	—
Core power supply for SerDes transceivers	SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers	XV_{DD}	–0.3 to 1.1	V	—

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD} (eTSEC1)	–0.3 to 3.63 –0.3 to 2.75	V	—
		TV_{DD} (eTSEC3)	–0.3 to 3.63 –0.3 to 2.75	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2
	DDR/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	2
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause.
2. (M,L,O)V_{IN}, and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 ± 50 mV	V	—
PLL supply voltage	AV_{DD}	1.0 ± 50 mV	V	1
Core power supply for SerDes transceivers	SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers	XV_{DD}	1.0 ± 50 mV	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	2

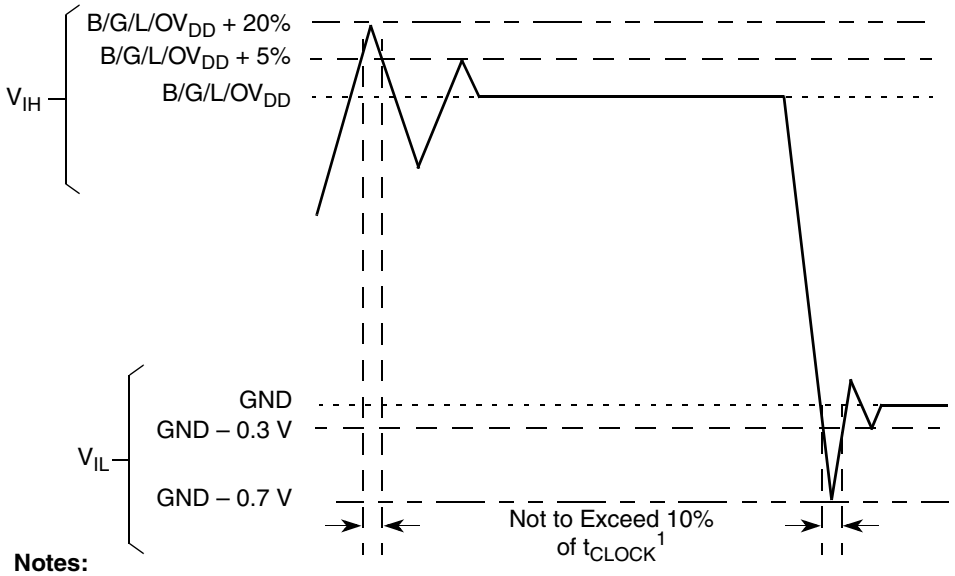
Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV_{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV_{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, PCI Express, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	3
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	5
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	2
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	5
	PCI, Local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3
Junction temperature range		T_j	0 to 90	°C	—

Notes:

1. This voltage is the input to the filter discussed in Section 21.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** T/LV_{IN} must not exceed T/ LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8533E.



Notes:
1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI_CLK or SYSCLK.
2. Please note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in Section 4.2.2.3 of the *PCI 2.2 Local Bus Specifications*.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}$

The core voltage must always be provided at nominal 1.0 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45 (default) 45 (default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI signals	25	OV_{DD} = 3.3 V	2
	42 (default)		
DDR signal	20	GV_{DD} = 2.5 V	—
DDR2 signal	16 32 (half strength mode)	GV_{DD} = 1.8 V	—
TSEC signals	42	LV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	42	OV_{DD} = 3.3 V	—
I^2C	150	OV_{DD} = 3.3 V	—

Notes:
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT1}}$ signal at reset.

2.2 Power Sequencing

The device requires its power rails to be applied in specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, LV_{DD}, SV_{DD}, OV_{DD}, TV_{DD}, XV_{DD}
2. GV_{DD}

Note that all supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, then the sequencing for GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

3 Power Characteristics

The estimated typical core power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in Table 4.

Table 4. MPC8533E Core Power Dissipation

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD} (V)	Junction Temperature (°C)	Power (W)	Notes
Typical	667	333	1.0	65	2.6	1, 2
Thermal				90	3.75	1, 3
Maximum					5.85	1, 4
Typical	800	400	1.0	65	2.9	1, 2
Thermal				90	4.0	1, 3
Maximum					6.0	1, 4
Typical	1000	400	1.0	65	3.6	1, 2
Thermal				90	4.4	1, 3
Maximum					6.2	1, 4
Typical	1067	533	1.0	65	3.9	1, 2
Thermal				90	5.0	1, 3
Maximum					6.5	1, 4

Notes:
1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.

4 Input Clocks

This section contains the following subsections:

- Section 4.1, “System Clock Timing”
- Section 4.2, “Real-Time Clock Timing”
- Section 4.3, “eTSEC Gigabit Reference Clock Timing”
- Section 4.4, “Platform to FIFO Restrictions”
- Section 4.5, “Other Input Clocks”

4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8533E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	—
SYSCLK jitter	—	—	—	±150	ps	3, 4

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. This represents the total input jitter—short- and long-term.
4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8533E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8533E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Max	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:
1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

4.2 Real-Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2 × the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8533E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD}, TV_{DD} = 2.5 V LV_{DD}, TV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TV_{DD} = 2.5 V, and from 0.6 and 2.7 V for L/TVDD = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.5.4, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency ≤ platform clock frequency ÷ 4.2

For example, if the platform frequency is 533 MHz, the FIFO Tx/Rx clock frequency should be no more than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency ≤ platform clock frequency ÷ 3.2

For example, if the platform frequency is 533 MHz, the FIFO Tx/Rx clock frequency should be no more than 167 MHz.

4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8533E. Table 8 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications[1]

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HREST}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Note:
1. SYSCLK is the primary clock input for the MPC8533E.

Table 9 provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
Core and platform PLL lock times	—	100	μs	—
Local bus PLL	—	50	μs	—
PCI bus lock time	—	50	μs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8533E. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 10 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8533E when GV_{DD}(typ) = 1.8 V.

Table 10. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.26	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.24	V	—
Output high current (V_{OUT} = 1.26 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.33 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

Table 11 provides the DDR2 I/O capacitance when GV_{DD}(typ) = 1.8 V.

Table 11. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 12 provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 12. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.3	V	—
Output high current (V_{OUT} = 1.8 V)	I_{OH}	–16.2	—	mA	—

Table 12. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current (V_{OUT} = 0.42 V)	I_{OL}	16.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

Table 13 provides the DDR I/O capacitance when GV_{DD}(typ) = 2.5 V.

Table 13. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the current draw characteristics for MV_{REF}.

Table 14. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 15 provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 1.8 V.

Table 15. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 16 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5$ V.

Table 16. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

Table 17 provides the input AC timing specifications for the DDR SDRAM interface.

Table 17. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
533 MHz		–300	300		3
400 MHz		–365	365		—
333 MHz		–390	390		—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$, where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}. See Figure 3.
3. Maximum DDR1 frequency is 400 MHz.

Figure 3 shows the DDR SDRAM input timing diagram.

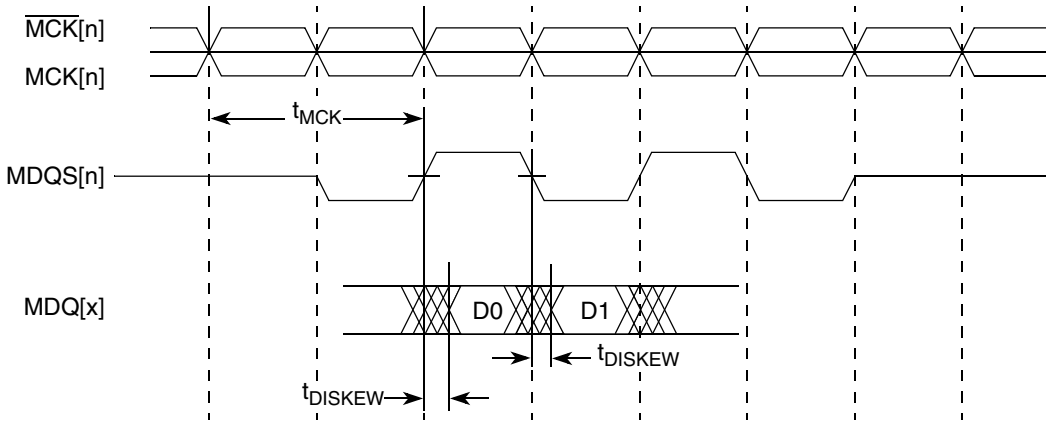


Figure 3. DDR SDRAM Input Timing Diagram (t_{DISKEW})

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 18 provides the output AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		538	—		7
400 MHz		700	—		—
333 MHz		900	—		—
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		538	—		7
400 MHz		700	—		—
333 MHz		900	—		—
MDQS preamble	t_{DDKHMP}	0.75 x tMCK	—	ns	6

Table 18. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQS postamble	t_{DDKHME}	0.4 x tMCK	0.6 x tMCK	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8533E PowerQUICC III Integrated Communications Processor Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz.

NOTE

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

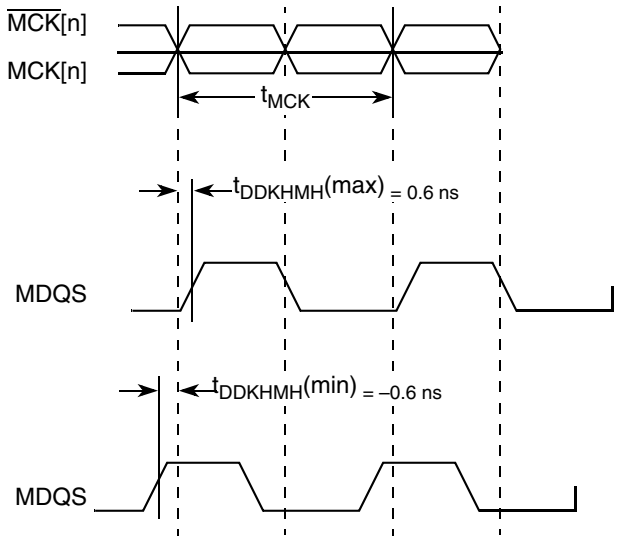


Figure 4. Timing Diagram for t_{DDKHMH}

Figure 5 shows the DDR SDRAM output timing diagram.

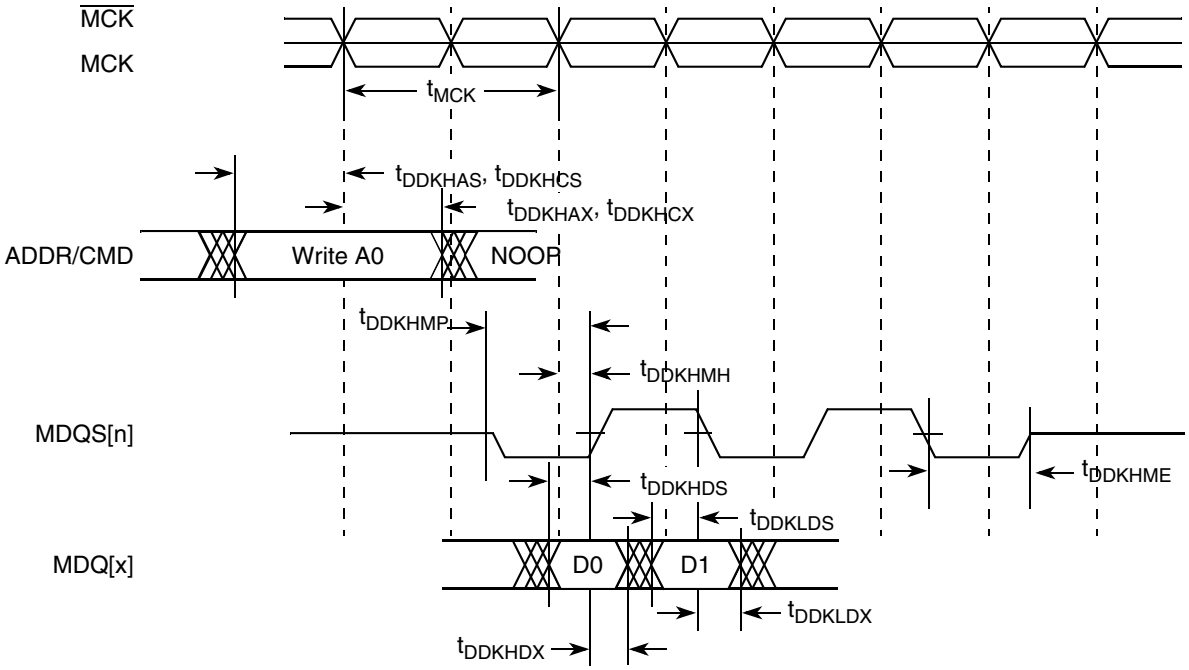


Figure 5. DDR and DDR2 SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

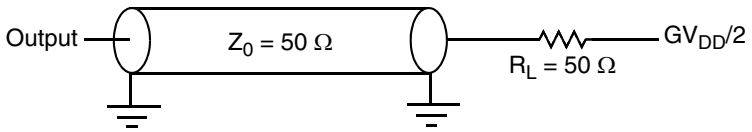


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8533E.

7.1 DUART DC Electrical Characteristics

Table 19 provides the DC electrical characteristics for the DUART interface.

Table 19. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 19. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 20 provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Notes:
1. CCB clock refers to the platform clock.
2. Actual attainable baud rate will be limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII/FIFO Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), 8-bit FIFO interface (FIFO), serial media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The 8-bit FIFO interface can operate at 3.3 or 2.5 V. The RGMII and RTBI interfaces are defined for 2.5 V, while the MII, GMII, TBI, and RMII interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical Characteristics.”

8.2 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RTBI, RMII, and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The potential applied to the input of a GMII, MII, TBI, RTBI, RMII, and FIFO receiver may exceed the potential of the receiver's power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 21. GMII, MII, TBI, RMII and FIFO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.135	3.465	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.5	V	—
Input high voltage	V_{IH}	1.95	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	μA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 22. GMII, MII, RMII, RGMII, RTBI, TBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.7	V	—
Input current (V_{IN} = 0, V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IN}	—	±15	μA	1, 2, 3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.3 FIFO, GMII,MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.3.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n* TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver.

A summary of the FIFO AC specifications appears in Table 23 and Table 24.

Table 23. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TX_CLK, GTX_CLK clock period	t_{FIT}	—	8.0	—	ns	—
TX_CLK, GTX_CLK duty cycle	t_{FITH}	45	50	55	%	—
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps	—
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns	—
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns	—
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns	1

Note:

1. Data valid t_{FITDV} to GTX_CLK Min setup time is a function of clock period and max hold time. (Min setup = Cycle time – Max hold).

Table 24. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{FIR}	—	8.0	—	ns	—
RX_CLK duty cycle	t_{FIRH}/t_{FIRH}	45	50	55	%	—
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps	—