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Freescale Semiconductor
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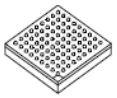
MPC8535E

MPC8535E PowerQUICC III Integrated Processor Hardware Specifications



MAPBGA–783
29 mm x 29 mm

- High-performance, 32-bit e500 core, scaling up to 1.25 GHz, that implements the Power Architecture® technology
  - 36-bit physical addressing
  - Double-precision embedded floating point APU using 64-bit operands
  - Embedded vector and scalar single-precision floating-point APUs using 32- or 64-bit operands
  - Memory management unit (MMU)
- Integrated L1/L2 cache
  - L1 cache—32-Kbyte data and 32-Kbyte instruction
  - L2 cache—512-Kbyte (8-way set associative)
- DDR2/DDR3 SDRAM memory controller with full ECC support
  - One 64-bit/32-bit data bus
  - Up to 250-MHz clock (500-MHz data rate)
  - Supporting up to 16 Gbytes of main memory
  - Using ECC, detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble
  - Invoke a level of system power management by asserting MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode
  - Both hardware and software options to support battery-backed main memory
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std 802.16e™, and 3GPP.
  - XOR engine for parity checking in RAID storage applications
- Enhanced Serial peripheral interfaces (eSPI)
  - Support boot capability from eSPI
- Two enhanced three-speed Ethernet controllers (eTSECs) with SGMII support
  - Three-speed support (10/100/1000 Mbps)
  - Two IEEE Std 802.3®, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, IEEE 802.3ab, and IEEE Std 1588™-compatible controllers
  - Support for various Ethernet physical interfaces: GMII, TBI, RTBI, RGMII, MII, RGMII, RMII, and SGMII
  - Support TCP/IP acceleration and QOS features
  - MAC address recognition and RMON statistics support
  - Support ARP parsing and generating wake-up events based on the parsing results while in deep sleep mode
  - Support accepting and storing packets while in deep sleep mode
- High-speed interfaces (multiplexed) supporting:
  - Two PCI Express interfaces
    - PCI Express 1.0a compatible
    - One x4/x2/x1 PCI Express interface
    - Two x2/x1 ports
  - One SGMII interface
  - One Serial ATA (SATA) controller supports SATA I and SATA I data rates
- PCI 2.2 compatible PCI controller
- Two universal serial bus (USB) dual-role controllers comply with USB specification revision 2.0
- 133-MHz, 32-bit, enhanced local bus (eLBC) with memory controller
- Enhanced secured digital host controller (eSDHC) used for SD/MMC card interface
  - Support boot capability from eSDHC
- Integrated four-channel DMA controller
- Dual I^2C and dual universal asynchronous receiver/transmitter (DUART) support
- Programmable interrupt controller (PIC)
- Power management, low standby power
  - Support Doze, Nap, Sleep, Jog, and Deep Sleep mode
  - PMC wake on: LAN activity, USB connection or remote wakeup, GPIO, internal timer, or external interrupt event
- System performance monitor
- IEEE Std 1149.1™-compatible, JTAG boundary scan
- 783-pin FC-PBGA package, 29 mm × 29 mm

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Table of Contents

1 Pin Assignments and Reset States 3
1.1 Pin Map 4
2 Electrical Characteristics 21
2.1 Overall DC Electrical Characteristics 21
2.2 Power Sequencing 25
2.3 Power Characteristics 26
2.4 Input Clocks 28
2.5 RESET Initialization 30
2.6 DDR2 and DDR3 SDRAM 31
2.7 eSPI 37
2.8 DUART 39
2.9 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management 39
2.10 Ethernet Management Interface Electrical Characteristics 60
2.11 USB 62
2.12 enhanced Local Bus Controller (eLBC) 65
2.13 Enhanced Secure Digital Host Controller (eSDHC) . . . 74
2.14 Programmable Interrupt Controller (PIC) 76
2.15 **JTAG** 76
2.16 Serial ATA (SATA) 78
2.17 I^2C 84
2.18 GPIO 87
2.19 PCI 88
2.20 High-Speed Serial Interfaces 90
2.21 PCI Express 99
2.23 Clocking 105
2.24 Thermal 109
3 Hardware Design Considerations 113
3.1 System Clocking 113
3.2 Power Supply Design and Sequencing 113
3.3 Pin States in Deep Sleep State 114
3.4 Decoupling Recommendations 114
3.5 SerDes Block Power Supply Decoupling Recommendations 115
3.6 Connection Recommendations 115
3.7 Pull-Up and Pull-Down Resistor Requirements 115
3.8 Output Buffer DC Impedance 115
3.9 Configuration Pin Muxing 116
3.10 JTAG Configuration Signals 117
3.11 Guidelines for High-Speed Interface Termination . . . 119
4 Ordering Information 120
4.1 Part Numbers Fully Addressed by this Document . . . 121
4.2 Part Marking 122
4.3 Part Numbering 122
5 Package Information 123
5.1 Package Parameters for the FC-PBGA 123
5.2 Mechanical Dimensions of the FC-PBGA 124
6 Product Documentation 125
7 Document Revision History 125

This figure shows the major functional units within the chip.

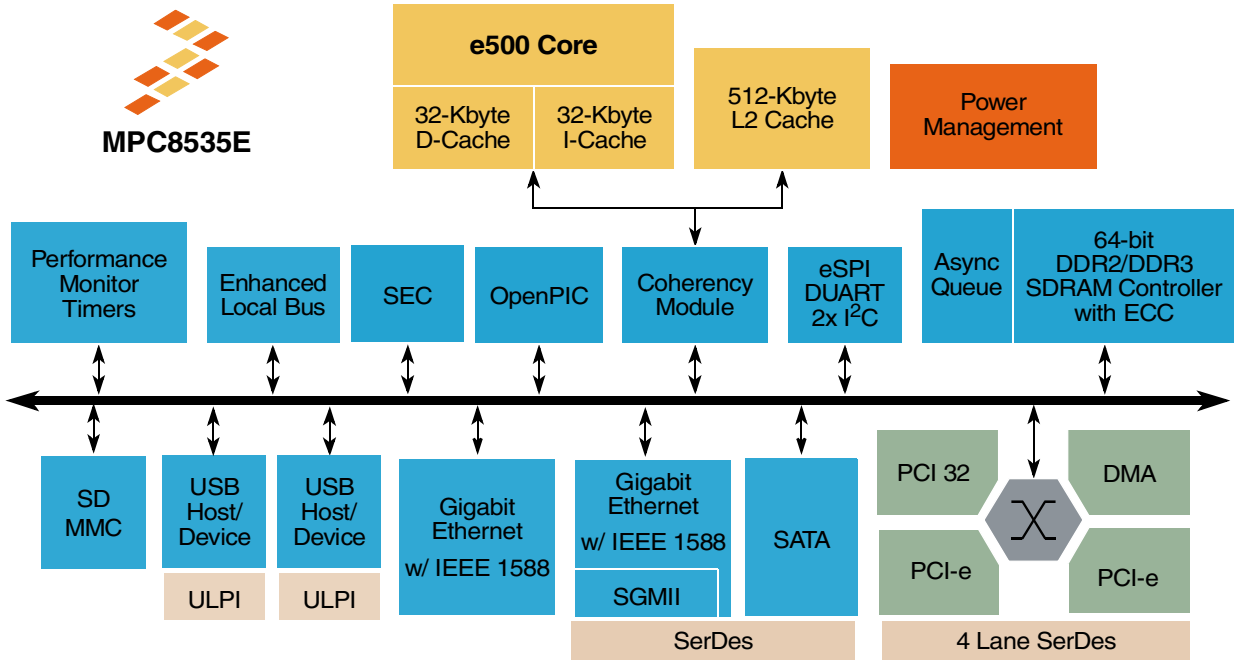


Figure 1. Chip Block Diagram

1 Pin Assignments and Reset States

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software

NOTE

The UART_SOUT[0:1] and $\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. See Table 1 for more details.

1.1 Pin Map

See Table 1 for the MPC8535E pinout, which is a subset of the MPC8536E.

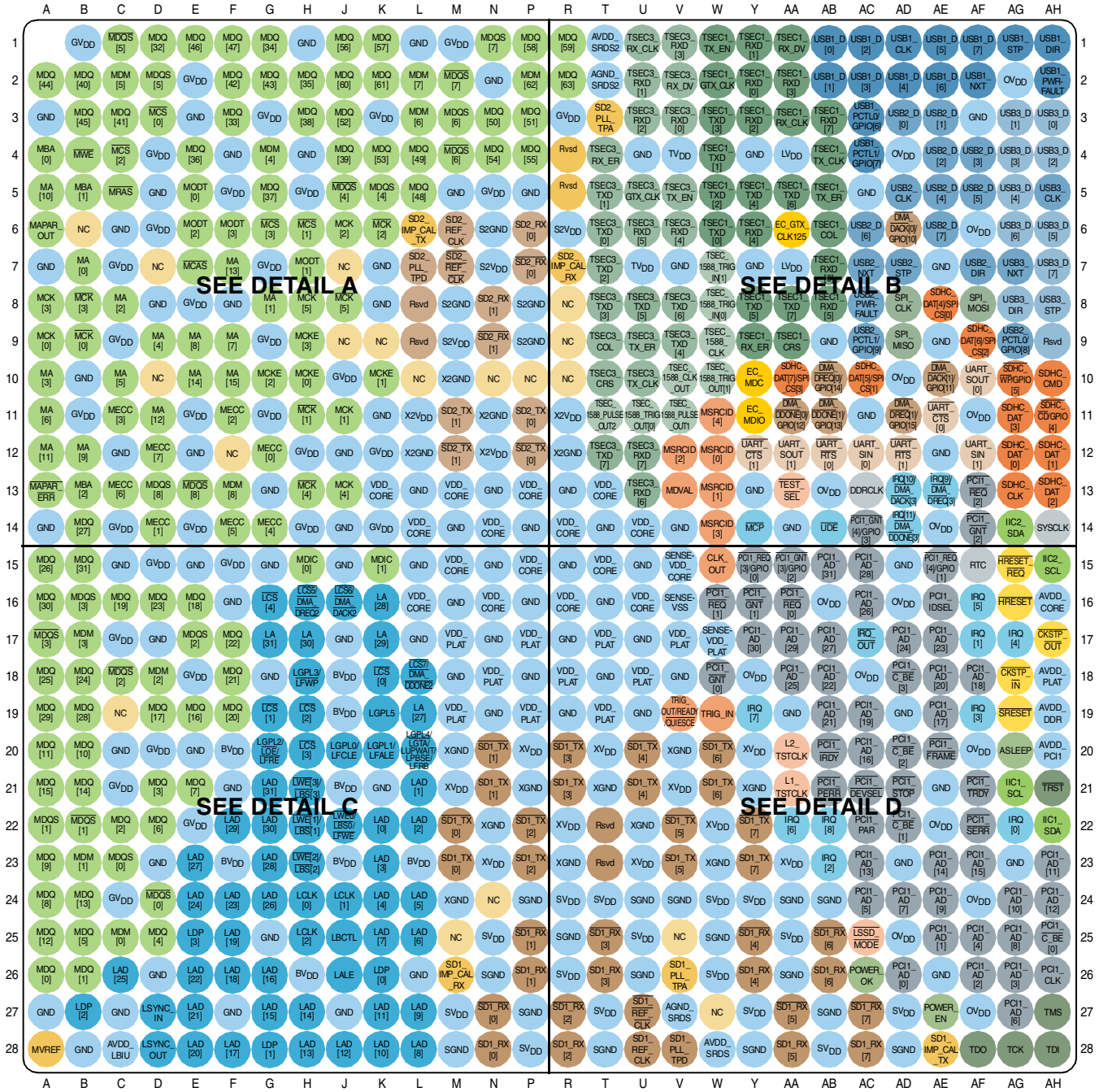
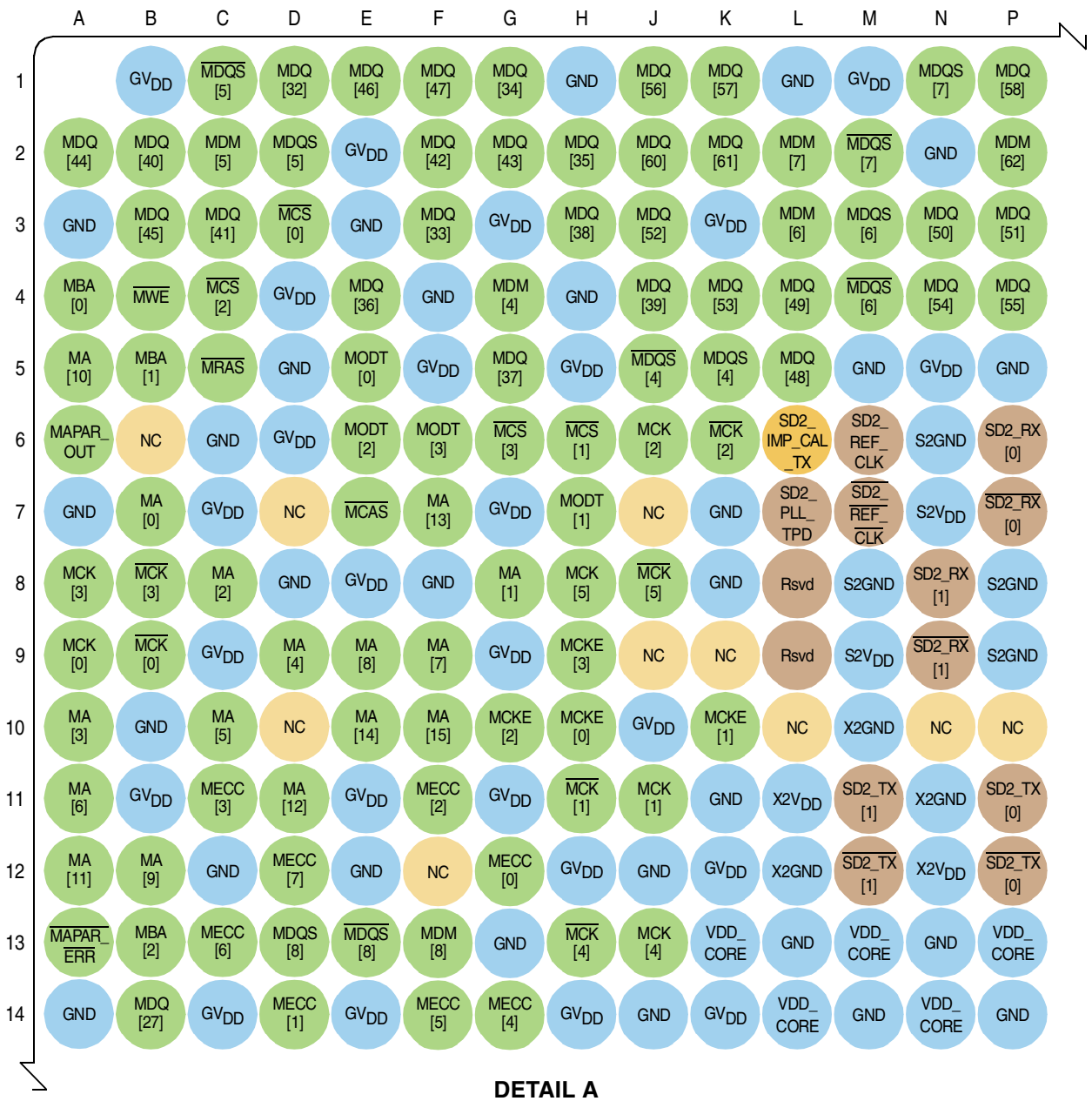
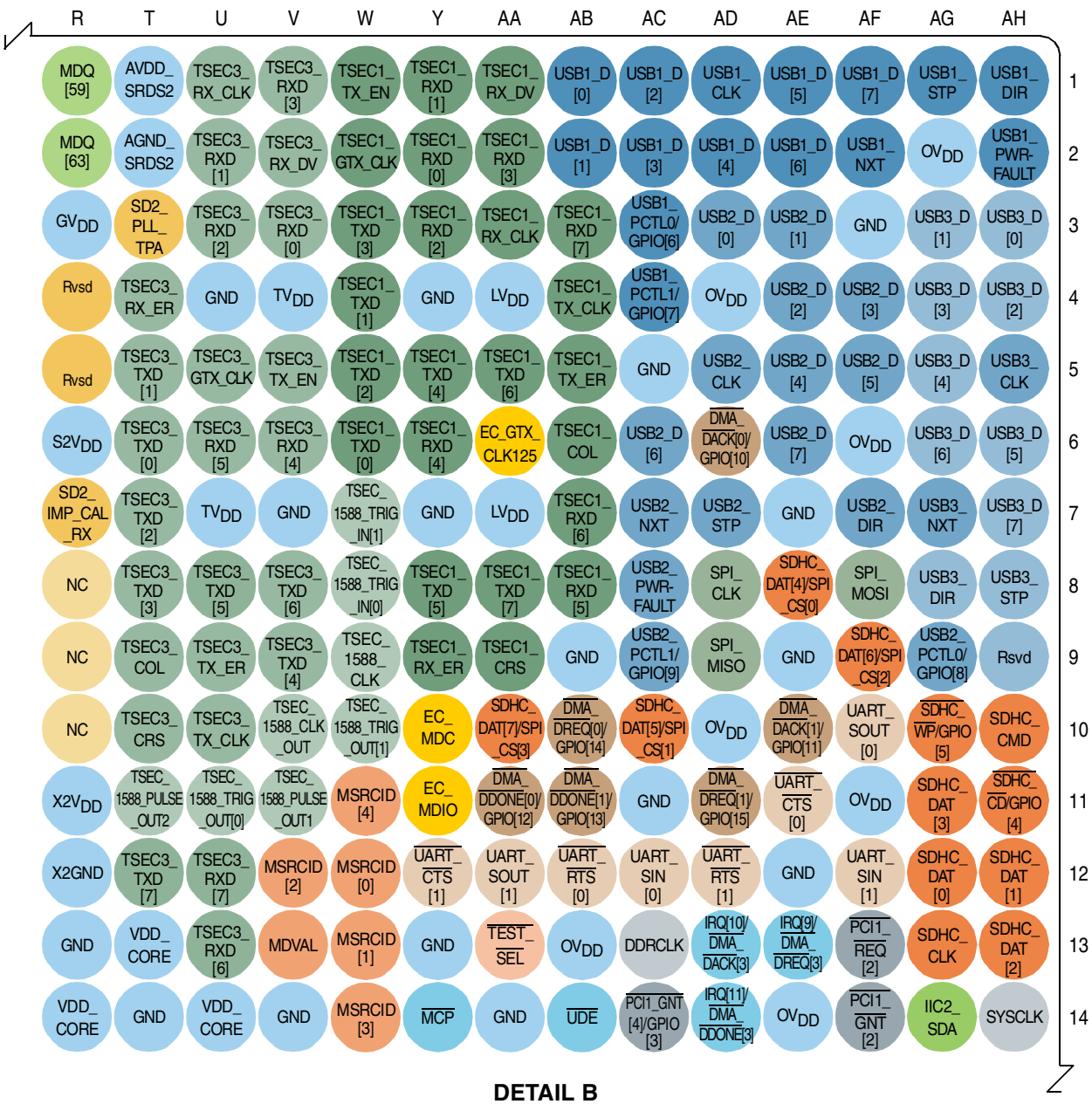


Figure 2. Chip Pin Map Bottom View



DETAIL A

Figure 3. Chip Pin Map Detail A



DETAIL B

Figure 4. Chip Pin Map Detail B

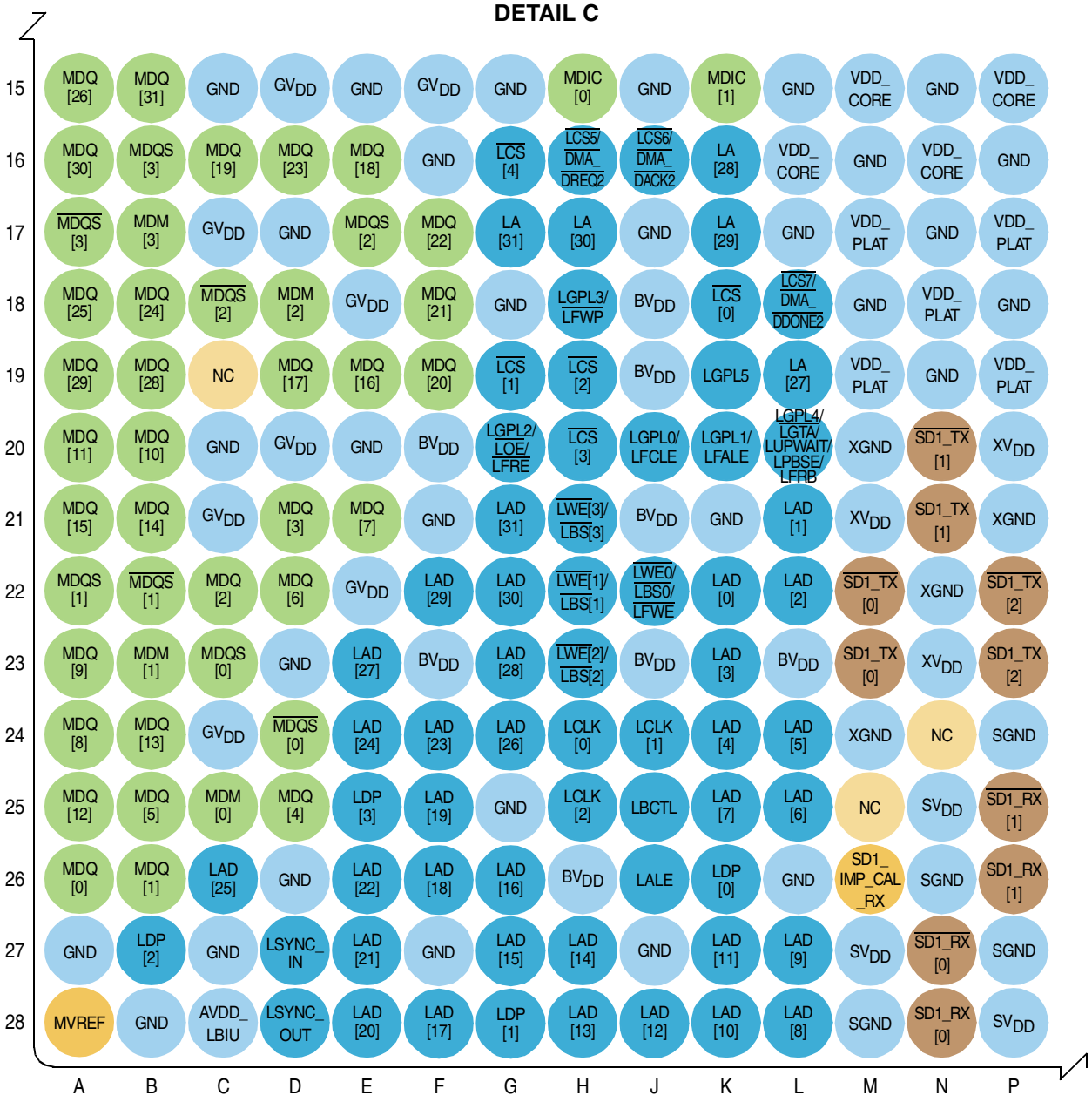


Figure 5. Chip Pin Map Detail C

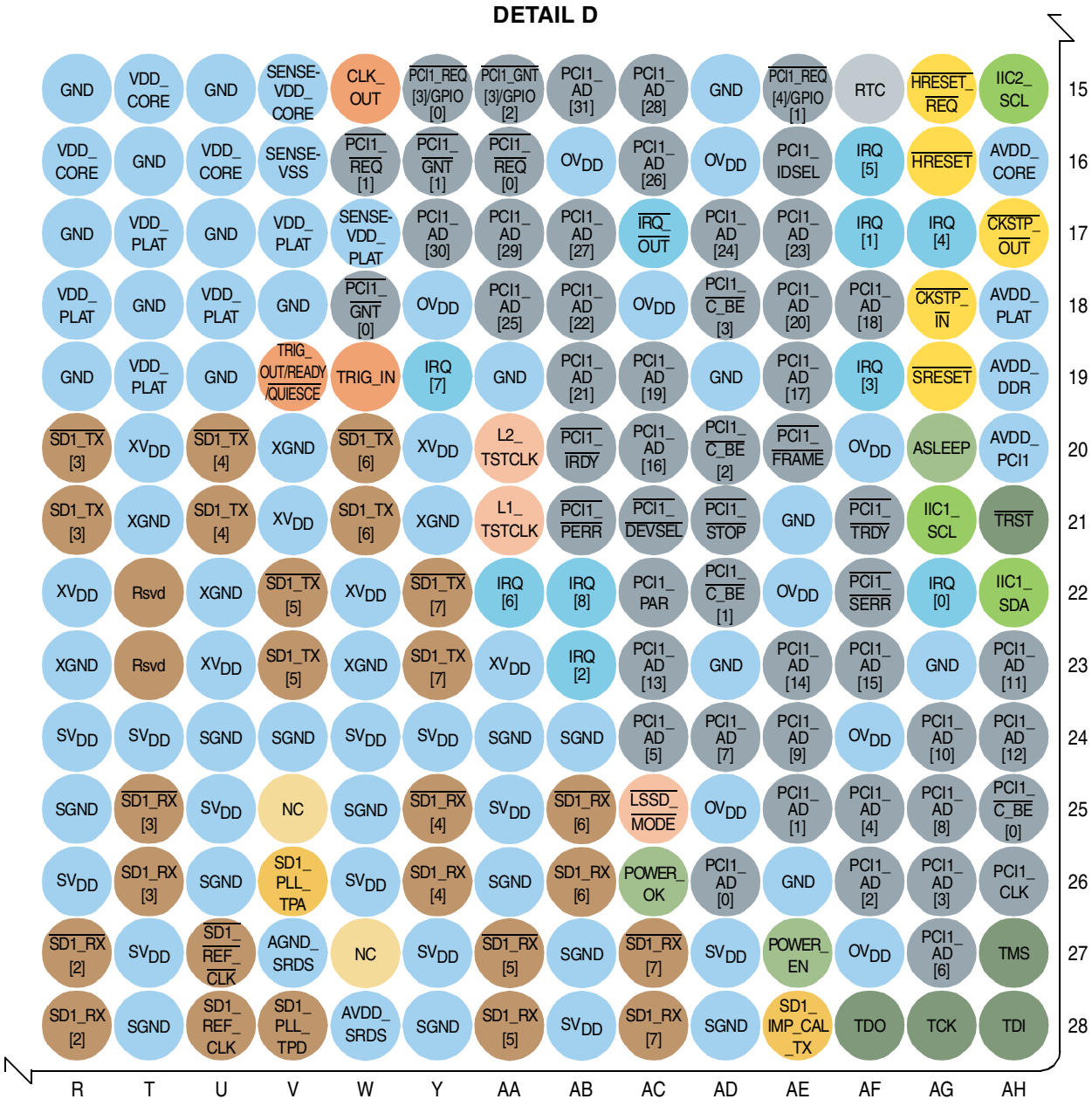


Figure 6. Chip Pin Map Detail D

This table provides the pin-out listing for the 783 FC-PBGA package.

Table 1. Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
PCI					
PCI1_AD[31:0]	Muxed Address / data	AB15,Y17,AA17,AC15, AB17,AC16,AA18, AD17,AE17,AB18, AB19,AE18,AC19, AF18,AE19,AC20, AF23,AE23,AC23, AH24,AH23,AG24, AE24,AG25,AD24, AG27,AC24,AF25, AG26,AF26,AE25, AD26	I/O	OV_{DD}	—
$\overline{\text{PCI1_C_BE[3:0]}}$	Command/Byte Enable	AD18, AD20,AD22, AH25	I/O	OV_{DD}	29
PCI1_PAR	Parity	AC22	I/O	OV_{DD}	29
$\overline{\text{PCI1_FRAME}}$	Frame	AE20	I/O	OV_{DD}	2,29
$\overline{\text{PCI1_TRDY}}$	Target Ready	AF21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1_IRDY}}$	Initiator Ready	AB20	I/O	OV_{DD}	2,29
$\overline{\text{PCI1_STOP}}$	Stop	AD21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1_DEVSEL}}$	Device Select	AC21	I/O	OV_{DD}	2,29
PCI1_IDSEL	Init Device Select	AE16	I	OV_{DD}	29
$\overline{\text{PCI1_PERR}}$	Parity Error	AB21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1_SERR}}$	System Error	AF22	I/O	OV_{DD}	2,4,29
$\overline{\text{PCI1_REQ}}$[4:3]/GPIO[1:0]	Request	AE15,Y15	I	OV_{DD}	—
$\overline{\text{PCI1_REQ}}$[2:1]	Request	AF13,W16	I	OV_{DD}	29
$\overline{\text{PCI1_REQ}}$[0]	Request	AA16	I/O	OV_{DD}	29
$\overline{\text{PCI1_GNT}}$[4:3]/GPIO[3:2]	Grant	AC14, AA15	O	OV_{DD}	
$\overline{\text{PCI1_GNT}}$[2:1]	Grant	AF14,Y16	O	OV_{DD}	5,9,25,29
$\overline{\text{PCI1_GNT}}$[0]	Grant	W18	I/O	OV_{DD}	29
PCI1_CLK	PCI Clock	AH26	I	OV_{DD}	29

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface					
MDQ[0:63]	Data	A26,B26,C22,D21,D25, B25,D22,E21,A24,A23, B20,A20,A25,B24,B21, A21,E19,D19,E16,C16, F19,F18,F17,D16,B18, A18,A15,B14,B19,A19, A16,B15,D1,F3,G1,H2, E4,G5,H3,J4,B2,C3,F2, G2,A2,B3,E1,F1,L5,L4, N3,P3,J3,K4,N4,P4,J1, K1,P1,R1,J2,K2,P2,R2	I/O	GV_{DD}	—
MECC[0:7]	Error Correcting Code	G12,D14,F11,C11, G14,F14,C13,D12	I/O	GV_{DD}	—
$\overline{\text{MAPAR_ERR}}$	Address Parity Error	A13	I	GV_{DD}	—
MAPAR_OUT	Address Parity Out	A6	O	GV_{DD}	—
MDM[0:8]	Data Mask	C25,B23,D18,B17,G4, C2,L3,L2,F13	O	GV_{DD}	—
$\overline{\text{MDQS}}$[0:8]	Data Strobe	D24,B22,C18,A17,J5, C1,M4,M2,E13	I/O	GV_{DD}	—
MDQS[0:8]	Data Strobe	C23,A22,E17,B16,K5, D2,M3,N1,D13	I/O	GV_{DD}	—
MA[0:15]	Address	B7,G8,C8,A10,D9,C10, A11,F9,E9,B12,A5, A12,D11,F7,E10,F10	O	GV_{DD}	—
MBA[0:2]	Bank Select	A4,B5,B13	O	GV_{DD}	—
$\overline{\text{MWE}}$	Write Enable	B4	O	GV_{DD}	—
$\overline{\text{MRAS}}$	Row Address Strobe	C5	O	GV_{DD}	—
$\overline{\text{MCAS}}$	Column Address Strobe	E7	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	Chip Select	D3,H6,C4,G6	O	GV_{DD}	—
MCKE[0:3]	Clock Enable	H10,K10,G10,H9	O	GV_{DD}	11
MCK[0:5]	Differential Clock 3 Pairs / DIMM	A9,J11,J6,A8,J13,H8	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	Differential Clock 3 Pairs / DIMM	B9,H11,K6,B8,H13,J8	O	GV_{DD}	—
MODT[0:3]	On Die Termination	E5,H7,E6,F6	O	GV_{DD}	—
MDIC[0:1]	Calibration	H15,K15	I/O	GV_{DD}	26
Local Bus Controller Interface					

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LAD[0:31]	Muxed data / address	K22,L21,L22,K23,K24, L24,L25,K25,L28,L27, K28,K27,J28,H28,H27, G27,G26,F28,F26,F25, E28,E27,E26,F24,E24, C26,G24,E23,G23,F22, G22,G21	I/O	BV_{DD}	5,9,29
LDP[0:3]	Data parity	K26,G28,B27,E25	I/O	BV_{DD}	29
LA[27]	Burst address	L19	O	BV_{DD}	5,9,29
LA[28:31]	Port address	K16,K17,H17,G17	O	BV_{DD}	5,7,9,29
$\overline{\text{LCS}}$[0:4]	Chip selects	K18,G19,H19,H20,G16	O	BV_{DD}	29
$\overline{\text{LCS5}}$/$\overline{\text{DMA_DREQ2}}$	Chips selects / DMA Request	H16	I/O	BV_{DD}	1,29
$\overline{\text{LCS6}}$/$\overline{\text{DMA_DACK2}}$	Chips selects / DMA Ack	J16	O	BV_{DD}	1,29
$\overline{\text{LCS7}}$/$\overline{\text{DMA_DDONE2}}$	Chips selects / DMA Done	L18	O	BV_{DD}	1,29
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LFWE}}$	Write enable / Byte select	J22	O	BV_{DD}	5,9,29
$\overline{\text{LWE[1:3]}}$/$\overline{\text{LBS[1:3]}}$	Write enable / Byte select	H22,H23,H21	O	BV_{DD}	5,9,29
LBCTL	Buffer control	J25	O	BV_{DD}	5,8,9,29
LALE	Address latch enable	J26	O	BV_{DD}	5,8,9,29
LGPL0/LFCLE	UPM general purpose line 0 / FLash command latch enable	J20	O	BV_{DD}	5,9,29
LGPL1/LFALE	UPM general purpose line 1 / Flash address latch enable	K20	O	BV_{DD}	5,9,29
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM general purpose line 2 / Output enable/Flash read enable	G20	O	BV_{DD}	5,8,9,29
LGPL3/$\overline{\text{LFWP}}$	UPM general purpose line 3 / Flash write protect	H18	O	BV_{DD}	5,9,29
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT /LPBSE/LFRB	UPM general purpose line 4 / Target Ack/Wait/SDRAM parity byte select/Flash Ready-busy	L20	I/O	BV_{DD}	29, 35
LGPL5	UPM general purpose line 5 / Amux	K19	O	BV_{DD}	5,9,29
LCLK[0:2]	Local bus clock	H24,J24,H25	O	BV_{DD}	29
LSYNC_IN	Synchronization	D27	I	BV_{DD}	29
LSYNC_OUT	Local bus DLL	D28	O	BV_{DD}	29
DMA					
$\overline{\text{DMA_DACK}}$[0:1] /GPIO[10:11]	DMA Acknowledge	AD6,AE10	O	OV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DMA_DREQ[0:1] /GPIO[14:15]	DMA Request	AB10,AD11	I	OV_{DD}	—
DMA_DDONE[0:1] /GPIO[12:13]	DMA Done	AA11,AB11	O	OV_{DD}	—
DMA_DREQ[2]/LCS[5]	Chips selects / DMA Request	H16	I/O	BV_{DD}	1,29
DMA_DACK[2]/LCS[6]	Chips selects / DMA Ack	J16	O	BV_{DD}	1,29
DMA_DDONE[2]/LCS[7]	Chips selects / DMA Done	L18	O	BV_{DD}	1,29
DMA_DREQ[3]/IRQ[9]	External interrupt/DMA request	AE13	I	OV_{DD}	1
DMA_DACK[3]/IRQ[10]	External interrupt/DMA Ack	AD13	I/O	OV_{DD}	1
DMA_DDONE[3]/IRQ[11]	External interrupt/DMA done	AD14	I/O	OV_{DD}	1
USB Port 1					
USB1_D[7:0]	USB1 Data bits	AF1,AE2,AE1,AD2, AC2,AC1,AB2,AB1	I/O	OV_{DD}	—
USB1_NXT	USB1 Next data	AF2	I	OV_{DD}	—
USB1_DIR	USB1 Data Direction	AH1	I	OV_{DD}	—
USB1_STP	USB1 Stop	AG1	O	OV_{DD}	5,9
USB1_PWRFAULT	USB1 bus power fault.	AH2	I	OV_{DD}	—
USB1_PCTL0/GPIO[6]	USB1 Port control 0	AC3	O	OV_{DD}	—
USB1_PCTL1/GPIO[7]	USB1 Port control 1	AC4	O	OV_{DD}	—
USB1_CLK	USB1 bus clock	AD1	I	OV_{DD}	—
USB Port 2					
USB2_D[7:0]	USB2 Data bits	AE6,AC6,AF5,AE5, AF4,AE4,AE3,AD3	I/O	OV_{DD}	—
USB2_NXT	USB2 Next data	AC7	I	OV_{DD}	—
USB2_DIR	USB2 Data Direction	AF7	I	OV_{DD}	—
USB2_STP	USB2 Stop	AD7	O	OV_{DD}	5,9
USB2_PWRFAULT	USB2 bus power fault.	AC8	I	OV_{DD}	—
USB2_PCTL0/GPIO[8]	USB2 Port control 0	AG9	O	OV_{DD}	—
USB2_PCTL1/GPIO[9]	USB2 Port control 1	AC9	O	OV_{DD}	—
USB2_CLK	USB2 bus clock	AD5	I	OV_{DD}	—
—					
Reserved	—	AH8	—	—	—
Reserved	—	AH7,AG6,AH6,AG5, AG4,AH4,AG3,AH3, AG7, AG8, AH9,AH5	—	—	27

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
Programmable Interrupt Controller					
$\overline{\text{MCP}}$	Machine check processor	Y14	I	OV_{DD}	—
$\overline{\text{UDE}}$	Unconditional debug event	AB14	I	OV_{DD}	—
IRQ[0:8]	External interrupts	AG22,AF17,AB23, AF19,AG17,AF16, AA22,Y19,AB22	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA_DREQ[3]}}$	External interrupt/DMA request	AE13	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA_DACK[3]}}$	External interrupt/DMA Ack	AD13	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA_DDONE[3]}}$	External interrupt/DMA done	AD14	I/O	OV_{DD}	1
$\overline{\text{IRQ_OUT}}$	Interrupt output	AC17	O	OV_{DD}	2,4
Ethernet Management Interface					
EC_MDC	Management data clock	Y10	O	OV_{DD}	5,9,22
EC_MDIO	Management data In/Out	Y11	I/O	OV_{DD}	—
Gigabit Reference Clock					
EC_GTX_CLK125	Reference clock	AA6	I	LV_{DD}	31
Three-Speed Ethernet Controller (Gigabit Ethernet 1)					
TSEC1_TXD[7:0]	Transmit data	AA8,AA5,Y8,Y5,W3, W5,W4,W6	O	LV_{DD}	5,9,22
TSEC1_TX_EN	Transmit Enable	W1	O	LV_{DD}	23
TSEC1_TX_ER	Transmit Error	AB5	O	LV_{DD}	5,9
TSEC1_TX_CLK	Transmit clock In	AB4	I	LV_{DD}	—
TSEC1_GTX_CLK	Transmit clock Out	W2	O	LV_{DD}	—
TSEC1_CRS	Carrier sense	AA9	I/O	LV_{DD}	17
TSEC1_COL	Collision detect	AB6	I	LV_{DD}	—
TSEC1_RXD[7:0]	Receive data	AB3,AB7,AB8,Y6,AA2, Y3,Y1,Y2	I	LV_{DD}	—
TSEC1_RX_DV	Receive data valid	AA1	I	LV_{DD}	—
TSEC1_RX_ER	Receive data error	Y9	I	LV_{DD}	—
TSEC1_RX_CLK	Receive clock	AA3	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)					
TSEC3_TXD[7:0]	Transmit data	T12,V8,U8,V9,T8,T7, T5,T6	O	TV_{DD}	5,9,22
TSEC3_TX_EN	Transmit Enable	V5	O	TV_{DD}	23
TSEC3_TX_ER	Transmit Error	U9	O	TV_{DD}	5,9

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TX_CLK	Transmit clock In	U10	I	TV_{DD}	—
TSEC3_GTX_CLK	Transmit clock Out	U5	O	TV_{DD}	—
TSEC3_CRS	Carrier sense	T10	I/O	TV_{DD}	17
TSEC3_COL	Collision detect	T9	I	TV_{DD}	—
TSEC3_RXD[7:0]	Receive data	U12,U13,U6,V6,V1,U3, U2,V3	I	TV_{DD}	—
TSEC3_RX_DV	Receive data valid	V2	I	TV_{DD}	—
TSEC3_RX_ER	Receive data error	T4	I	TV_{DD}	—
TSEC3_RX_CLK	Receive clock	U1	I	TV_{DD}	—
IEEE 1588					
TSEC_1588_CLK	Clock In	W9	I	LV_{DD}	29
TSEC_1588_TRIG_IN[0:1]	Trigger In	W8,W7	I	LV_{DD}	29
TSEC_1588_TRIG_OUT[0:1]	Trigger Out	U11,W10	O	LV_{DD}	5,9,29
TSEC_1588_CLK_OUT	Clock Out	V10	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT1	Pulse Out1	V11	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT2	Pulse Out2	T11	O	LV_{DD}	5,9,29
eSDHC					
SDHC_CMD	Command line	AH10	I/O	OV_{DD}	29
$\overline{\text{SDHC_CD}}$/GPIO[4]	Card detection	AH11	I	OV_{DD}	—
SDHC_DAT[0:3]	Data line	AG12,AH12,AH13, AG11	I/O	OV_{DD}	29
SDHC_DAT[4:7] / SPI_CS[0:3]	8-bit MMC Data line / SPI chip select	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
SDHC_CLK	SD/MMC/SDIO clock	AG13	I/O	OV_{DD}	29
$\overline{\text{SDHC_WP}}$/GPIO[5]	Card write protection	AG10	I	OV_{DD}	1, 32
eSPI					
SPI_MOSI	Master Out Slave In	AF8	I/O	OV_{DD}	29
SPI_MISO	Master In Slave Out	AD9	I	OV_{DD}	29
SPI_CLK	eSPI clock	AD8	I/O	OV_{DD}	29
SPI_CS[0:3] / SDHC_DAT[4:7]	eSPI chip select / SDHC 8-bit MMC data	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
DUART					
$\overline{\text{UART_CTS}}$[0:1]	Clear to send	AE11,Y12	I	OV_{DD}	29
$\overline{\text{UART_RTS}}$[0:1]	Ready to send	AB12,AD12	O	OV_{DD}	29
UART_SIN[0:1]	Receive data	AC12,AF12	I	OV_{DD}	29

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
UART_SOUT[0:1]	Transmit data	AF10,AA12	O	OV_{DD}	5,9,22, 10,29
I^2C interface					
IIC1_SCL	Serial clock	AG21	I/O	OV_{DD}	4,21,29
IIC1_SDA	Serial data	AH22	I/O	OV_{DD}	4,21,29
IIC2_SCL	Serial clock	AH15	I/O	OV_{DD}	4,21,29
IIC2_SDA	Serial data	AG14	I/O	OV_{DD}	4,21,29
SerDes1(x4)					
SD1_TX[7:4]	Transmit Data (+)	Y23,W21,V23,U21	O	XV_{DD}	—
$\overline{\text{SD1_TX}}$[7:4]	Transmit Data(-)	Y22,W20,V22,U20	O	XV_{DD}	—
SD1_RX[7:4]	Receive Data(+)	AC28,AB26,AA28,Y26	I	XV_{DD}	—
$\overline{\text{SD1_RX}}$[7:4]	Receive Data(–)	AC27,AB25,AA27,Y25	I	XV_{DD}	—
Reserved	—	R21,P23,N21,M23, R20,P22,N20,M22	—	—	18
Reserved	—	T26,R28,P26,N28, T25,R27,P25,N27	—	—	33
SD1_PLL_TPD	PLL test point Digital	V28	O	XV_{DD}	18
SD1_REF_CLK	PLL Reference clock	U28	I	XV_{DD}	—
$\overline{\text{SD1_REF_CLK}}$	PLL Reference clock complement	U27	I	XV_{DD}	—
Reserved	—	T22	—	—	18
Reserved	—	T23	—	—	18
SerDes2(x1)					
SD2_TX[0]	Transmit data(+)	P11	O	$X2V_{DD}$	—
$\overline{\text{SD2_TX[0]}}$	Transmit data(-)	P12	O	$X2V_{DD}$	—
SD2_RX[0]	Receive data(+)	P6	I	$X2V_{DD}$	—
$\overline{\text{SD2_RX[0]}}$	Receive data(-)	P7	I	$X2V_{DD}$	—
Reserved	—	M11,M12	—	—	18
Reserved	—	N8, N9	—	—	34
SD2_PLL_TPD	PLL test point Digital	L7	O	$X2V_{DD}$	18
SD2_REF_CLK	PLL Reference clock	M6	I	$X2V_{DD}$	—
$\overline{\text{SD2_REF_CLK}}$	PLL Reference clock complement	M7	I	$X2V_{DD}$	—
Reserved	—	L8	—	$X2V_{DD}$	18
Reserved	—	L9	—	$X2V_{DD}$	18

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
General-Purpose Input/Output					
GPIO[0:1]/PCI1_REQ[3:4]	GPIO/PCI request	Y15,AE15	I/O	OV_{DD}	—
GPIO[2:3]/PCI1_GNT[3:4]	GPIO/PCI grant	AA15,AC14	I/O	OV_{DD}	—
GPIO[4]/SDHC_CD	GPIO/SDHC card detection	AH11	I/O	OV_{DD}	—
GPIO[5]/SDHC_WP	GPIO/SDHC write protection	AG10	I/O	OV_{DD}	32
GPIO[6]/USB1_PCTL0	GPIO/USB1 PCTL0	AC3	I/O	OV_{DD}	—
GPIO[7]/USB1_PCTL1	GPIO/USB1 PCTL1	AC4	I/O	OV_{DD}	—
GPIO[8]/USB2_PCTL0	GPIO/USB2 PCTL0	AG9	I/O	OV_{DD}	—
GPIO[9]/USB2_PCTL1	GPIO/USB2 PCTL1	AC9	I/O	OV_{DD}	—
GPIO[10:11] /DMA_DACK[0:1]	GPIO/DMA Ack	AD6,AE10	I/O	OV_{DD}	—
GPIO[12:13] /DMA_DDONE[0:1]	GPIO/DMA done	AA11,AB11	I/O	OV_{DD}	—
GPIO[14:15] /DMA_DREQ[0:1]	GPIO/DMA request	AB10,AD11	I/O	OV_{DD}	—
System Control					
HRESET	Hard reset	AG16	I	OV_{DD}	—
HRESET_REQ	Hard reset - request	AG15	O	OV_{DD}	22
SRESET	Soft reset	AG19	I	OV_{DD}	—
CKSTP_IN	CheckStop in	AG18	I	OV_{DD}	—
CKSTP_OUT	CheckStop Output	AH17	O	OV_{DD}	2,4
Debug					
TRIG_IN	Trigger in	W19	I	OV_{DD}	—
TRIG_OUT/READY /QUIESCE	Trigger out/Ready/Quiesce	V19	O	OV_{DD}	22
MSRCID[0:1]	Memory debug source port ID	W12,W13	O	OV_{DD}	6,9
MSRCID[2:4]	Memory debug source port ID	V12, W14,W11	O	OV_{DD}	6,9,22
MDVAL	Memory debug data valid	V13	O	OV_{DD}	6,22
CLK_OUT	Clock Out	W15	O	OV_{DD}	11
Clock					
RTC	Real time clock	AF15	I	OV_{DD}	—
SYSCLK	System clock / PCI clock	AH14	I	OV_{DD}	—
DDRCLK	DDR clock	AC13	I	OV_{DD}	30
JTAG					

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TCK	Test clock	AG28	I	OV_{DD}	—
TDI	Test data in	AH28	I	OV_{DD}	12
TDO	Test data out	AF28	O	OV_{DD}	11
TMS	Test mode select	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test reset	AH21	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 test clock	AA21	I	OV_{DD}	19
L2_TSTCLK	L2 test clock	AA20	I	OV_{DD}	19
$\overline{\text{LSSD_MODE}}$	LSSD Mode	AC25	I	OV_{DD}	19
$\overline{\text{TEST_SEL}}$	Test select	AA13	I	OV_{DD}	19
Power Management					
ASLEEP	Asleep	AG20	O	OV_{DD}	9,16,22
POWER_OK	Power OK	AC26	I	OV_{DD}	—
POWER_EN	Power enable	AE27	O	OV_{DD}	—
Power and Ground Signals					
OVDD	General I/O supply	Y18,AG2,AD4,AB16, AF6,AC18,AB13,AD10, AE14,AD16,AD25, AF27,AE22,AF11, AF20,AF24	—	OV_{DD}	—
LVDD	GMAC 1 I/O supply	AA7, AA4	Power for TSEC1 interfaces	LV_{DD}	—
TVDD	GMAC 3 I/O supply	V4,U7	Power for TSEC3 interfaces	TV_{DD}	—
GVDD	SSTL2 DDR supply	B1,B11,C7,C9,C14, C17,D4,D6,R3,D15,E2, E8,C24,E18,F5,E14, C21,G3,G7,G9,G11, H5,H12,E22,F15,J10, K3,K12,K14,H14,D20, E11,M1,N5	Power for DDR DRAM I/O	GV_{DD}	—
BVDD	Local bus I/O supply	L23,J18,J23,J19,F20, F23,H26,J21	Power for Local Bus	BV_{DD}	—
SVDD	SerDes 1 core logic supply	M27,N25,P28,R24, R26,T24,T27,U25, W24,W26,Y24,Y27, AA25,AB28,AD27	—	SV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
XVDD	SerDes 1 transceiver supply	M21,N23,P20,R22,T20, U23,V21,W22,Y20, AA23	—	XV_{DD}	—
S2VDD	SerDes 2 core logic supply	R6,N7,M9	—	$S2V_{DD}$	—
X2VDD	SerDes 2 transceiver supply	R11,N12,L11	—	$X2V_{DD}$	—
VDD_CORE	Core, L2 logic supply	P13,U16,L16,M15,N14, R14,P15,N16,M13, U14,T13,L14,T15,R16, K13	—	V_{DD_CORE}	—
VDD_PLAT	Platform logic supply	T19,T17,V17,U18,R18, N18,M19,P19,P17,M17	—	V_{DD_PLAT}	—
AVDD_CORE	CPU PLL supply	AH16	—	AV_{DD_CORE}	20,28
AVDD_PLAT	Platform PLL supply	AH18	—	AV_{DD_PLAT}	20
AVDD_DDR	DDR PLL supply	AH19	—	AV_{DD_DDR}	20
AVDD_LBIU	Local Bus PLL supply	C28	—	AV_{DD_LBIU}	20
AVDD_PCI1	PCI PLL supply	AH20	—	AV_{DD_PCI1}	20
AVDD_SRDS	SerDes 1 PLL supply	W28	—	AV_{DD_SRDS}	20
AVDD_SRDS2	SerDes 2 PLL supply	T1	—	AV_{DD_SRDS2}	20
SENSEVDD_CORE	—	V15	—	V_{DD_CORE}	13
SENSEVDD_PLAT	—	W17	—	V_{DD_PLAT}	13
GND	Ground	D5,AE7,F4,D26,D23, C12,C15,E20,D8,B10, AF3,E3,J14,K21,F8,A3, F16,E12,E15,D17,L1, F21,H1,G13,G15,G18, C6,A14,A7,G25,H4, C20,J12,J15,J17,F27, M5,J27,K11,L26,K7, K8,T14,V14,M16,M18, P14,N15,N17,N19,N2, P5,P16,P18,M14,R15, R17,R19,T16,T18,L17, U15,U17,U19,V18,C27, Y13,AE26,AA19,AE21, B28,AC11,AD19,AD23, L15,AD15,AG23,AE9, A27,V7,Y7,AC5,U4,Y4, AE12,AB9,AA14,N13, R13,L13	—	—	—
XGND	SerDes 1Transceiver pad GND (xpadvss)	M20,M24,N22,P21, R23,T21,U22,V20, W23, Y21	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND	SerDes 1 Transceiver core logic GND (xcorevss)	M28,N26,P24,P27, R25,T28,U24,U26,V24, W25,Y28,AA24,AA26, AB24,AB27,AD28	—	—	—
X2GND	SerDes 2 Transceiver pad GND (xpadvss)	R12,M10,N11,L12	—	—	—
S2GND	SerDes 2 Transceiver core logic GND (xcorevss)	P8,P9,N6,M8	—	—	—
AGND_SRDS	SerDes 1 PLL GND	V27	—	—	—
AGND_SRDS2	SerDes 2 PLL GND	T2	—	—	—
SENSEVSS	GND Sensing	V16	—	—	13
Analog Signals					
MVREF	SSTL2 reference voltage	A28	Reference voltage for DDR	GVDD/2	—
SD1_IMP_CAL_RX	Rx impedance calibration	M26	—	200Ω (±1%) to GND	—
SD1_IMP_CAL_TX	Tx impedance calibration	AE28	—	100Ω (±1%) to GND	—
SD1_PLL_TPA	PLL test point analog	V26	—	AVDD_SRDS analog	18
SD2_IMP_CAL_RX	Rx impedance calibration	R7	—	200Ω (±1%) to GND	—
SD2_IMP_CAL_TX	Tx impedance calibration	L6	—	100Ω (±1%) to GND	—
SD2_PLL_TPA	PLL test point analog	T3	—	AVDD_SRDS2 analog	18
Reserved	—	R4	—	—	—
Reserved	—	R5	—	—	—
No Connect Pins					
NC	—	C19,D7,D10,L10,R10, B6,F12,J7,P10,M25, W27,N24,N10,R8,J9, K9,V25,R9	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes

Notes:

1. All multiplexed signals may be listed only once and may not re-occur.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
3. This pin must always be pulled-high.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 22.2, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 22.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. For proper state of these signals during reset, UART_SOUT[1] must be pulled down to GND through a resistor. UART_SOUT[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on UART_SOUT[0].
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD_CORE}/V_{DD_PLAT}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
15. These pins have other manufacturing or debug test functions. It's recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.
16. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
17. This pin is only an output in FIFO mode when used as Rx Flow Control.
18. Do not connect.
19. These must be pulled up (100 Ω- 1 kΩ) to OVDD.
20. Independent supplies derived from board VDD.
21. Recommend a pull-up resistor (1 KΩ) be placed on this pin to OV_{DD}.
22. The following pins must NOT be pulled down during power-on reset: MDVAL, UART_SOUT[0], EC_MDC, TSEC1_TXD[3], TSEC3_TXD[7], HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP.
23. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
24. General-Purpose POR configuration of user system.

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes

25. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as “No Connect” or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
26. When operating in DDR2 mode, connect MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and connect MDIC[1] to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect MDIC[0] to ground through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor, and connect MDIC[1] to GVDD through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
27. Connect to GND through a pull down 1 kΩ resistor.
28. It must be the same as VDD_CORE
29. The output pads are tristated and the receivers of pad inputs are disabled during the Deep Sleep state when GCR[DEEPSLEEP_Z] =1.
30. DDRCLK input is only required when the DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the *MPC8536E PowerQUICC III Integrated Host Processor Family Reference Manual* , Table 4-3 in section 4.2.2 “Clock Signals”, section 4.4.3.2 “DDR PLL Ratio” and Table 4-10 “DDR Complex Clock PLL Ratio” for more detailed description regarding DDR controller operation in asynchronous and synchronous modes.
31. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
32. $\overline{\text{SDHC_WP}}$ is active low signal, which follows SDHC Host controller specification. However, it is reversed polarity for SD/MMC card specification.
33. Must connect to XGND.
34. Must connect to X2GND
35. For systems which boot from Local Bus(GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required.

2 Electrical Characteristics

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD_CORE}	–0.3 to 1.21	V	—
Platform supply voltage		V_{DD_PLAT}	–0.3 to 1.1	V	—
PLL core supply voltage		AV_{DD_CORE}	–0.3 to 1.21	V	—
PLL other supply voltage		AV_{DD}	–0.3 to 1.1	V	—
Core power supply for SerDes transceivers		SV_{DD}, $S2V_{DD}$	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}, $X2V_{DD}$	–0.3 to 1.1	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	–0.3 to 1.98	V	—
	DDR3 SDRAM Interface		–0.3 to 1.65		
Three-speed Ethernet I/O		LV_{DD} (eTSEC1)	–0.3 to 3.63 –0.3 to 2.75	V	2
		TV_{DD} (eTSEC3)	–0.3 to 3.63 –0.3 to 2.75	V	2
PCI, DUART, system control and power management, I^2C, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	3
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
Storage temperature range		T_{STG}	–55 to 150	^{0}C	—

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect chip reliability or cause permanent damage to the chip.
2. The 3.63-V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 2.9.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,” for details on the recommended operating conditions per protocol.
3. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip. Note that the values in this table are the recommended and tested operating conditions. Proper chip operation outside these conditions is not guaranteed.

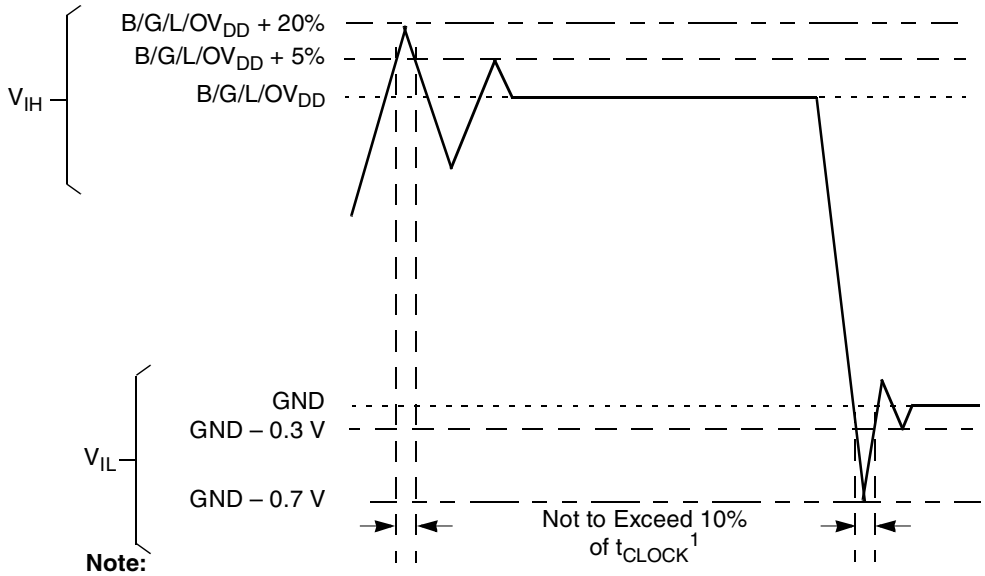
Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD_CORE}	1.0 ± 50 mV	V	—
Platform supply voltage		V_{DD_PLAT}	1.0 ± 50 mV	V	—
PLL core supply voltage		AV_{DD_CORE}	1.0 ± 50 mV	V	2
PLL other supply voltage		AV_{DD}	1.0 ± 50 mV	V	2
Core power supply for SerDes transceivers		SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}	1.0 ± 50 mV	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	1.8 V ± 90 mV	V	3
	DDR3 SDRAM Interface		1.5 V ± 75 mV		
Three-speed Ethernet I/O voltage		LV_{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	5
		TV_{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, system control and power management, I^2C, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage		OV_{DD}	3.3 V ± 165 mV	V	4
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 SDRAM Interface signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 and DDR3 SDRAM Interface reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	5
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, Local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	4
Operating Temperature range	Commercial	T_A T_J	T_A= 0 (min) to T_J= 90(max)	°C	6
	Industrial standard temperature range		T_A= 0 (min) to T_J= 105 (max)		
	Extended temperature range		T_A= -40 (min) to T_J= 105 (max)		

Notes:

2. This voltage is the input to the filter discussed in Section 3.2.1, "PLL Power Supply Filtering," and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.
3. **Caution**: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution**: L/TVIN must not exceed L/TVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For eLBC, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI1_CLK or SYSCLK.

2. With the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

Figure 7. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The core voltage must always be provided at nominal 1.0 V . (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied MVREF*n* signal (nominally set to GVDD/2) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45(default) 45(default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI signals	25	OV_{DD} = 3.3 V	2
	42 (default)		
DDR2 signal	16 32 (half strength mode)	GV_{DD} = 1.8 V	3
DDR3 signal	20 40 (half strength mode)	GV_{DD} = 1.5 V	2
TSEC signals	42	LV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	42	OV_{DD} = 3.3 V	—
I^2C	150	OV_{DD} = 3.3 V	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI1_GNT1}}$ signal at reset.
3. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_j = 105°C and at GV_{DD} (min)

2.2 Power Sequencing

The chip requires its power rails to be applied in a specific sequence in order to ensure proper chip operation. These requirements are as follows for power up:

1. V_{DD_PLAT}, V_{DD_CORE} (if POWER_EN is not used to control V_{DD_CORE}), AV_{DD}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD},$S2V_{DD}$, TV_{DD}, XV_{DD} and $X2V_{DD}$
2. [Wait for POWER_EN to assert], then V_{DD_CORE} (if POWER_EN is used to control V_{DD_CORE})
3. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD platform supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the chip.

During the Deep Sleep state, the VDD core supply is removed. But all other power supplies remain applied. Therefore, there is no requirement to apply the VDD core supply before any other power rails when the silicon waking from Deep Sleep.