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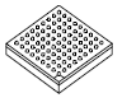
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MPC8569EEC
Rev. 2, 10/2013

MPC8569E

MPC8569E PowerQUICC III Integrated Processor Hardware Specifications



- High-performance, 32-bit e500 core, scaling up to 1.33 GHz, that implements the Power Architecture® technology
  - 2799 MIPS at 1.33 GHz (estimated Dhrystone 2.1)
  - 36-bit physical addressing
  - Double-precision embedded floating point APU using 64-bit operands
  - Embedded vector and scalar single-precision floating-point APUs using 32- or 64-bit operands
  - Memory management unit (MMU)
- Integrated L1/L2 cache
  - L1 cache—32-Kbyte data and 32-Kbyte instruction
  - L2 cache—512-Kbyte (8-way set associative)
- Two DDR2/DDR3 SDRAM memory controllers with full ECC support
  - One 64-bit or two 32-bit data bus configuration
  - Up to 400 MHz clock (800 MHz data rate)
  - Supporting up to 16 Gbytes of main memory
  - Using ECC, detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble
  - Invoke a level of system power management by asserting MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode
  - Both hardware and software options to support battery-backed main memory
  - Initialization bypass feature that allow system designers to prevent re-initialization of main memory during system power on following abnormal shutdown
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std 802.11i™, IEEE Std 802.16™ (WiMAX), IEEE 802.1ae™ (MACSec), 3GPP, A5/3 for GSM and EDGE, and GEA3 for GPRS.
  - XOR engine for parity checking in RAID storage applications
  - Four crypto-channels, each supporting multi-command descriptor chains
  - Cryptographic execution units for PKEU, DEU, AESU, AFEU, MDEU, KEU, CRCU, RNG and SEU- SNOW
- QUICC Engine technology
  - Four 32-bit RISC cores
  - Supports Ethernet, ATM, POS, and T1/E1 along with associated interworking
    - Four Gigabit Ethernet interfaces (up to two with SGMII)
    - Up to eight 10/100-Mbps Ethernet interfaces
    - Up to 16 T1/E1 TDM links (512 × 64 channels)
    - Multi-PHY UTOPIA/POS-PHY L2 interface (16-bit)
  - IEEE Std 1588™ v2 support
  - SPI and Ethernet PHY management interface
  - One full-/low-speed USB interface supporting USB 2.0
  - General-purpose I/O signals
- High-speed interfaces (multiplexed) supporting:
  - Two 1× Serial RapidIO interfaces (with message unit) or one 4x interface
  - ×4/×2/×1 PCI Express interface
  - Two SGMII interfaces
- On-chip network switch fabric
- 133 MHz, 16-bit, 3.3 V I/O, enhanced local bus (eLBC) with memory controller
- Enhanced secured digital host controller (eSDHC) used for SD/MMC card interface
- Integrated four-channel DMA controller
- Dual I^2C and dual universal asynchronous receiver/transmitter (DUART) support
- Programmable interrupt controller (PIC)
- IEEE Std 1149.1™ JTAG test access port
- 1.0-V and 1.1-V core voltages with 3.3-V, 2.5-V, 1.8-V, 1.5-V and 1.0-V I/O
- 783-pin FC-PBGA package, 29 mm × 29 mm

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

Table of Contents

NOTE

The MPC8569E is also available without a security engine in a configuration known as the MPC8569. All specifications other than those relating to security apply to the MPC8569 exactly as described in this document.

The following figure shows the major functional units within the MPC8569E.

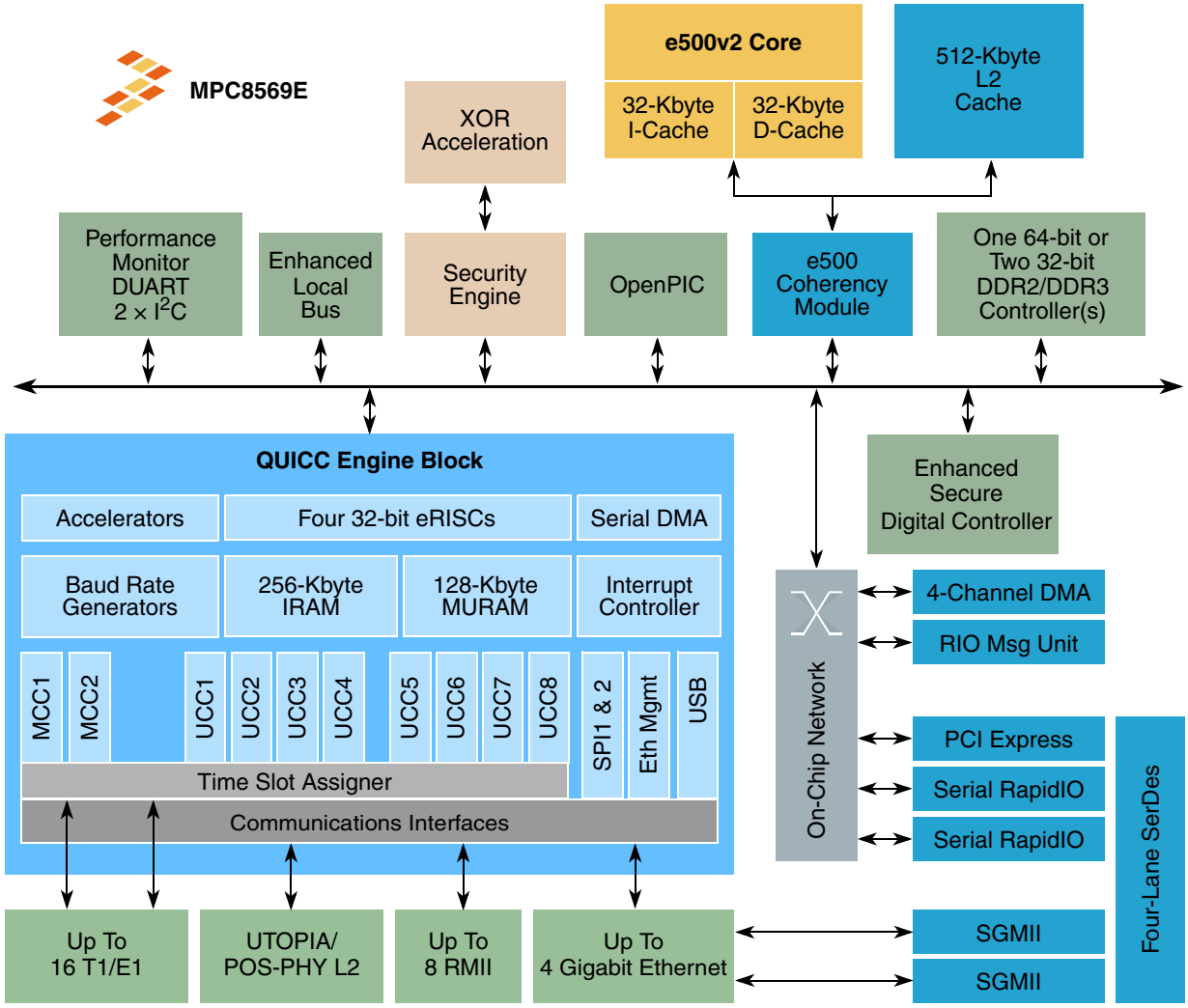


Figure 1. MPC8569E Block Diagram

1 Pin Assignments and Reset States

1.1 Ball Layout Diagrams

The following figure shows the top view of the MPC8569E 783-pin BGA ball map diagram.

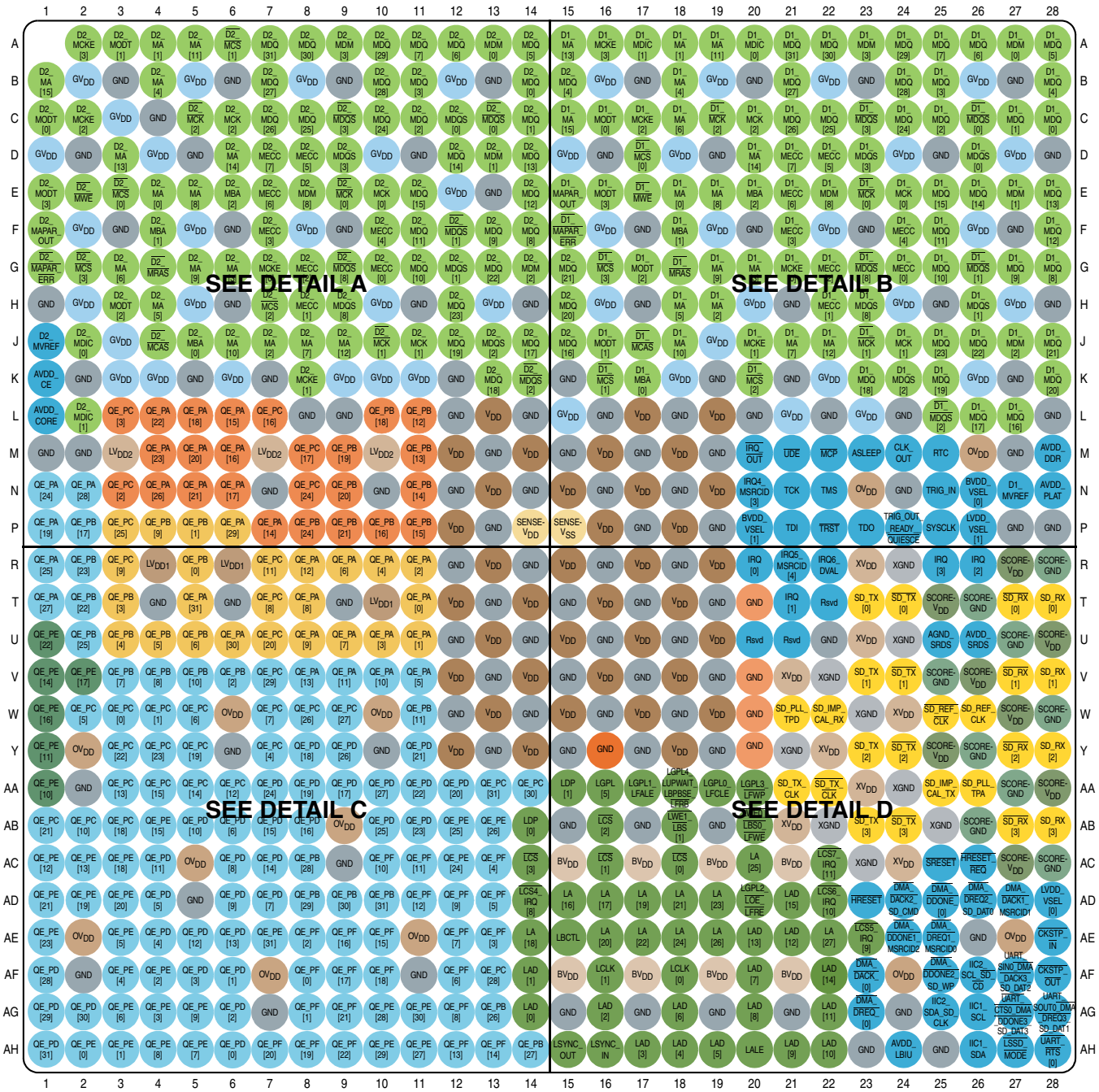
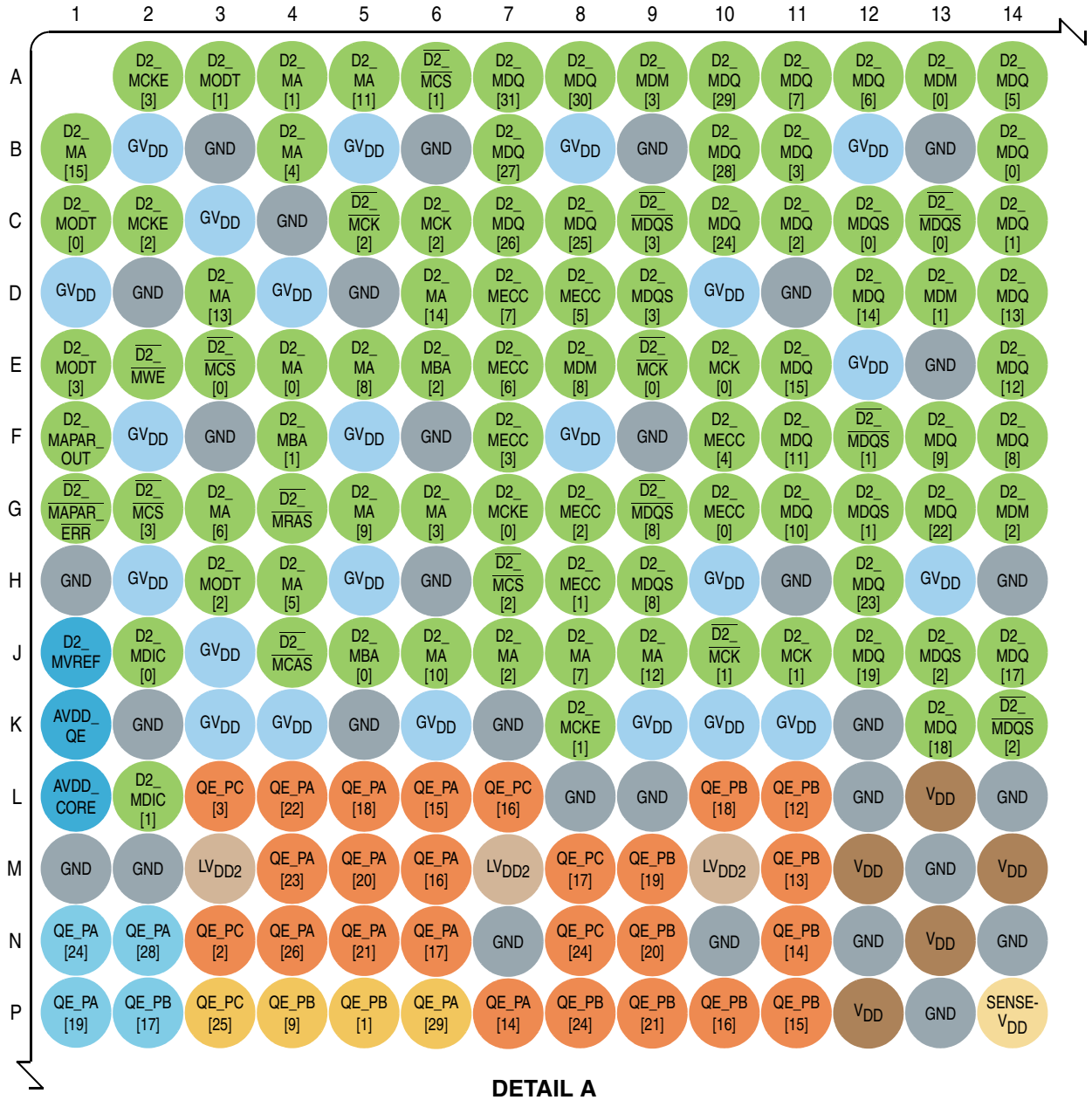


Figure 2. MPC8569E Top View Ballmap

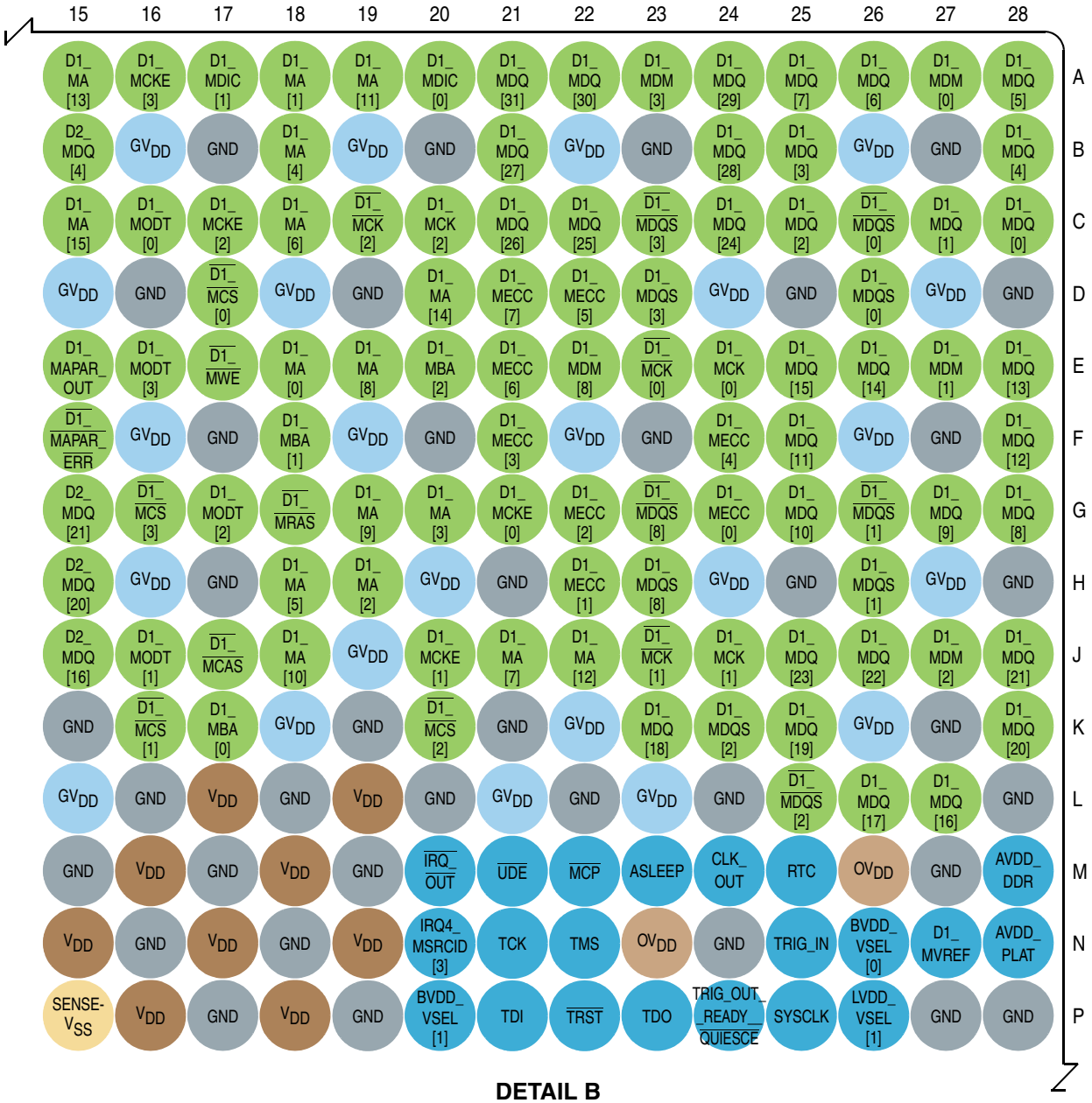
The following figure provides detailed view A of the MPC8569E 783-pin BGA ball map diagram.



DETAIL A

Figure 3. MPC8569E Detail A Ball Map

The following figure provides detailed view B of the MPC8569E 783-pin BGA ball map diagram.



DETAIL B

Figure 4. MPC8569E Detail B Ball Map

The following figure provides detailed view C of the MPC8569E 783-pin BGA ball map diagram.

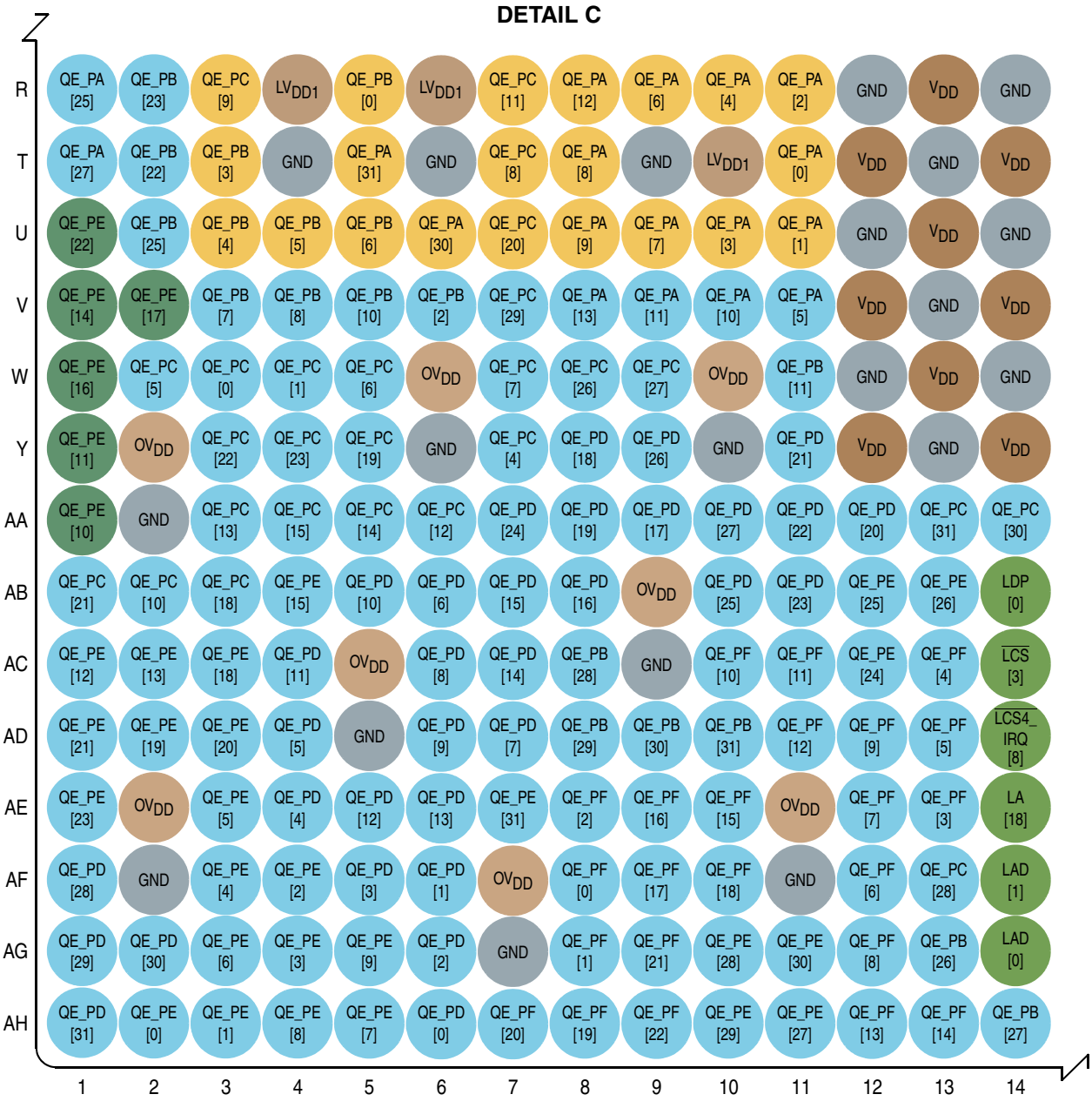


Figure 5. MPC8569E Detail C Ball Map

The following figure provides detailed view D of the MPC8569E 783-pin BGA ball map diagram.

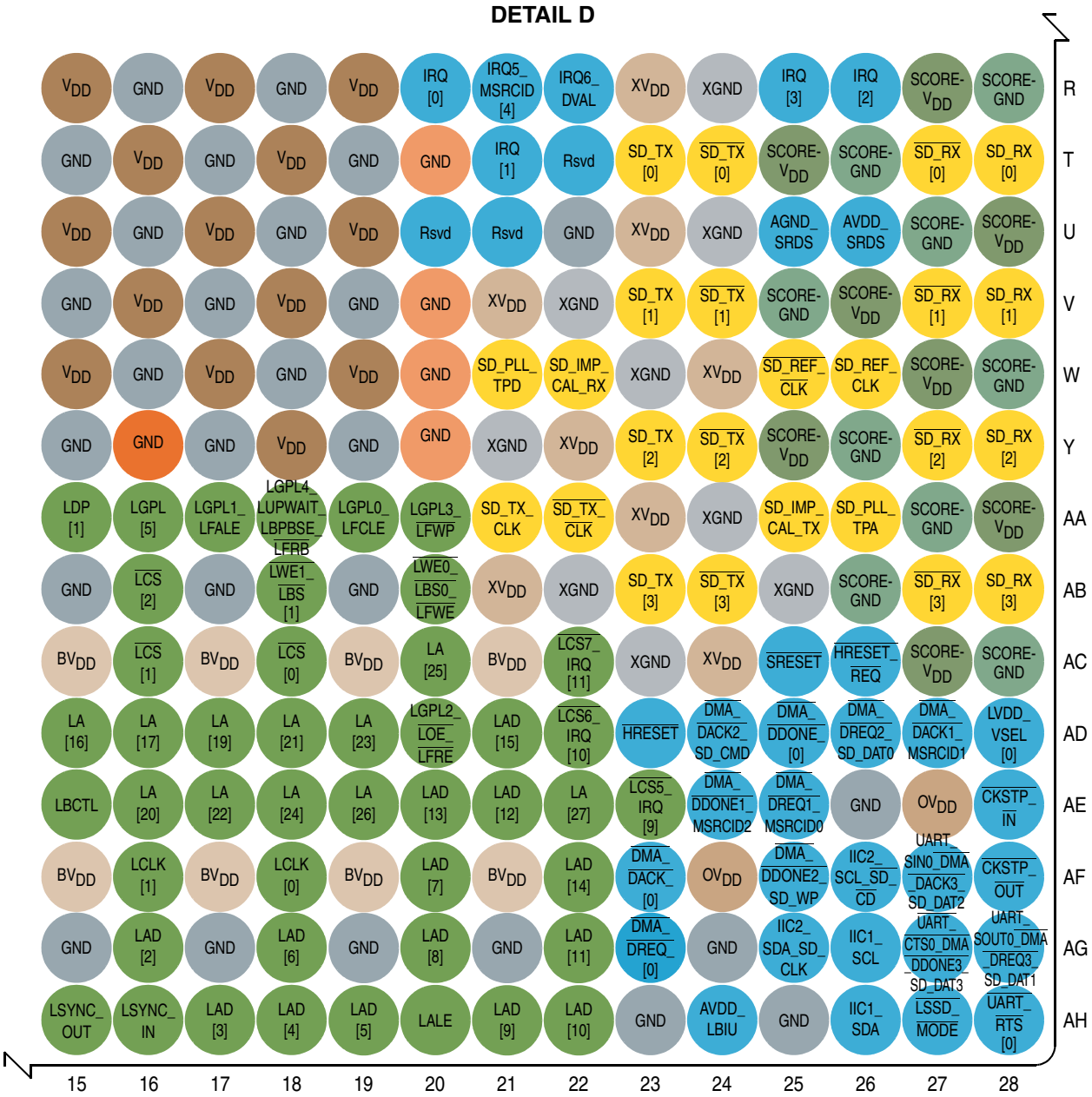


Figure 6. MPC8569E Detail D Ball Map

1.2 Pinout List

The following table provides the pinout listing for the MPC8569E 783 FC-PBGA package.

Table 1. MPC8569E Pinout Listing

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
Clocks				
RTC	M25	I	OV_{DD}	—
SYSCLK	P25	I	OV_{DD}	—
DDR SDRAM Memory Interface				
D1_MA0	E18	O	GV_{DD}	—
D1_MA1	A18	O	GV_{DD}	—
D1_MA2	H19	O	GV_{DD}	—
D1_MA3	G20	O	GV_{DD}	—
D1_MA4	B18	O	GV_{DD}	—
D1_MA5	H18	O	GV_{DD}	—
D1_MA6	C18	O	GV_{DD}	—
D1_MA7	J21	O	GV_{DD}	—
D1_MA8	E19	O	GV_{DD}	—
D1_MA9	G19	O	GV_{DD}	—
D1_MA10	J18	O	GV_{DD}	—
D1_MA11	A19	O	GV_{DD}	—
D1_MA12	J22	O	GV_{DD}	—
D1_MA13	A15	O	GV_{DD}	—
D1_MA14	D20	O	GV_{DD}	—
D1_MA15	C15	O	GV_{DD}	—
D1_MBA0	K17	O	GV_{DD}	—
D1_MBA1	F18	O	GV_{DD}	—
D1_MBA2	E20	O	GV_{DD}	—
$\overline{\text{D1\_MCAS}}$	J17	O	GV_{DD}	—
D1_MCK0	E24	O	GV_{DD}	—
$\overline{\text{D1\_MCK0}}$	E23	O	GV_{DD}	—
D1_MCK1	J24	O	GV_{DD}	—
$\overline{\text{D1\_MCK1}}$	J23	O	GV_{DD}	—
D1_MCK2	C20	O	GV_{DD}	—
$\overline{\text{D1\_MCK2}}$	C19	O	GV_{DD}	—
D1_MCKE0	G21	O	GV_{DD}	—
D1_MCKE1	J20	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MCKE2	C17	O	GV_{DD}	—
D1_MCKE3	A16	O	GV_{DD}	—
$\overline{\text{D1\_MCS0}}$	D17	O	GV_{DD}	—
$\overline{\text{D1\_MCS1}}$	K16	O	GV_{DD}	—
$\overline{\text{D1\_MCS2}}$	K20	O	GV_{DD}	—
$\overline{\text{D1\_MCS3}}$	G16	O	GV_{DD}	—
D1_MDIC0	A20	I/O	GV_{DD}	27
D1_MDIC1	A17	I/O	GV_{DD}	27
D1_MDM0	A27	I/O	GV_{DD}	—
D1_MDM1	E27	I/O	GV_{DD}	—
D1_MDM2	J27	I/O	GV_{DD}	—
D1_MDM3	A23	I/O	GV_{DD}	—
D1_MDM8	E22	I/O	GV_{DD}	—
D1_MDQ0	C28	I/O	GV_{DD}	—
D1_MDQ1	C27	I/O	GV_{DD}	—
D1_MDQ2	C25	I/O	GV_{DD}	—
D1_MDQ3	B25	I/O	GV_{DD}	—
D1_MDQ4	B28	I/O	GV_{DD}	—
D1_MDQ5	A28	I/O	GV_{DD}	—
D1_MDQ6	A26	I/O	GV_{DD}	—
D1_MDQ7	A25	I/O	GV_{DD}	—
D1_MDQ8	G28	I/O	GV_{DD}	—
D1_MDQ9	G27	I/O	GV_{DD}	—
D1_MDQ10	G25	I/O	GV_{DD}	—
D1_MDQ11	F25	I/O	GV_{DD}	—
D1_MDQ12	F28	I/O	GV_{DD}	—
D1_MDQ13	E28	I/O	GV_{DD}	—
D1_MDQ14	E26	I/O	GV_{DD}	—
D1_MDQ15	E25	I/O	GV_{DD}	—
D1_MDQ16	L27	I/O	GV_{DD}	—
D1_MDQ17	L26	I/O	GV_{DD}	—
D1_MDQ18	K23	I/O	GV_{DD}	—
D1_MDQ19	K25	I/O	GV_{DD}	—
D1_MDQ20	K28	I/O	GV_{DD}	—
D1_MDQ21	J28	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQ22	J26	I/O	GV_{DD}	—
D1_MDQ23	J25	I/O	GV_{DD}	—
D1_MDQ24	C24	I/O	GV_{DD}	—
D1_MDQ25	C22	I/O	GV_{DD}	—
D1_MDQ26	C21	I/O	GV_{DD}	—
D1_MDQ27	B21	I/O	GV_{DD}	—
D1_MDQ28	B24	I/O	GV_{DD}	—
D1_MDQ29	A24	I/O	GV_{DD}	—
D1_MDQ30	A22	I/O	GV_{DD}	—
D1_MDQ31	A21	I/O	GV_{DD}	—
D1_MDQS0	D26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	C26	I/O	GV_{DD}	—
D1_MDQS1	H26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	G26	I/O	GV_{DD}	—
D1_MDQS2	K24	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	L25	I/O	GV_{DD}	—
D1_MDQS3	D23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	C23	I/O	GV_{DD}	—
D1_MDQS8	H23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS8}}$	G23	I/O	GV_{DD}	—
D1_MECC0	G24	I/O	GV_{DD}	—
D1_MECC1	H22	I/O	GV_{DD}	—
D1_MECC2	G22	I/O	GV_{DD}	—
D1_MECC3	F21	I/O	GV_{DD}	—
D1_MECC4	F24	I/O	GV_{DD}	—
D1_MECC5	D22	I/O	GV_{DD}	—
D1_MECC6	E21	I/O	GV_{DD}	—
D1_MECC7	D21	I/O	GV_{DD}	—
D1_MODT0	C16	O	GV_{DD}	—
D1_MODT1	J16	O	GV_{DD}	—
D1_MODT2	G17	O	GV_{DD}	—
D1_MODT3	E16	O	GV_{DD}	—
D1_MAPAR_OUT	E15	O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	F15	I	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	G18	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{D1\_MWE}}$	E17	O	GV_{DD}	—
D2_MA0	E4	O	GV_{DD}	—
D2_MA1	A4	O	GV_{DD}	—
D2_MA2	J7	O	GV_{DD}	—
D2_MA3	G6	O	GV_{DD}	—
D2_MA4	B4	O	GV_{DD}	—
D2_MA5	H4	O	GV_{DD}	—
D2_MA6	G3	O	GV_{DD}	—
D2_MA7	J8	O	GV_{DD}	—
D2_MA8	E5	O	GV_{DD}	—
D2_MA9	G5	O	GV_{DD}	—
D2_MA10	J6	O	GV_{DD}	—
D2_MA11	A5	O	GV_{DD}	—
D2_MA12	J9	O	GV_{DD}	—
D2_MA13	D3	O	GV_{DD}	—
D2_MA14	D6	O	GV_{DD}	—
D2_MA15	B1	O	GV_{DD}	—
D2_MBA0	J5	O	GV_{DD}	—
D2_MBA1	F4	O	GV_{DD}	—
D2_MBA2	E6	O	GV_{DD}	—
$\overline{\text{D2\_MCAS}}$	J4	O	GV_{DD}	—
D2_MCK0	E10	O	GV_{DD}	—
$\overline{\text{D2\_MCK0}}$	E9	O	GV_{DD}	—
D2_MCK1	J11	O	GV_{DD}	—
$\overline{\text{D2\_MCK1}}$	J10	O	GV_{DD}	—
D2_MCK2	C6	O	GV_{DD}	—
$\overline{\text{D2\_MCK2}}$	C5	O	GV_{DD}	—
D2_MCKE0	G7	O	GV_{DD}	—
D2_MCKE1	K8	O	GV_{DD}	—
D2_MCKE2	C2	O	GV_{DD}	—
D2_MCKE3	A2	O	GV_{DD}	—
$\overline{\text{D2\_MCS0}}$	E3	O	GV_{DD}	—
$\overline{\text{D2\_MCS1}}$	A6	O	GV_{DD}	—
$\overline{\text{D2\_MCS2}}$	H7	O	GV_{DD}	—
$\overline{\text{D2\_MCS3}}$	G2	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDIC0	J2	I/O	GV_{DD}	27
D2_MDIC1	L2	I/O	GV_{DD}	27
D2_MDM0/D1_MDM4	A13	I/O	GV_{DD}	—
D2_MDM1/D1_MDM5	D13	I/O	GV_{DD}	—
D2_MDM2/D1_MDM6	G14	I/O	GV_{DD}	—
D2_MDM3/D1_MDM7	A9	I/O	GV_{DD}	—
D2_MDM8	E8	I/O	GV_{DD}	—
D2_MDQ0/D1_MDQ32	B14	I/O	GV_{DD}	—
D2_MDQ1/D1_MDQ33	C14	I/O	GV_{DD}	—
D2_MDQ2/D1_MDQ34	C11	I/O	GV_{DD}	—
D2_MDQ3/D1_MDQ35	B11	I/O	GV_{DD}	—
D2_MDQ4/D1_MDQ36	B15	I/O	GV_{DD}	—
D2_MDQ5/D1_MDQ37	A14	I/O	GV_{DD}	—
D2_MDQ6/D1_MDQ38	A12	I/O	GV_{DD}	—
D2_MDQ7/D1_MDQ39	A11	I/O	GV_{DD}	—
D2_MDQ8/D1_MDQ40	F14	I/O	GV_{DD}	—
D2_MDQ9/D1_MDQ41	F13	I/O	GV_{DD}	—
D2_MDQ10/D1_MDQ42	G11	I/O	GV_{DD}	—
D2_MDQ11/D1_MDQ43	F11	I/O	GV_{DD}	—
D2_MDQ12/D1_MDQ44	E14	I/O	GV_{DD}	—
D2_MDQ13/D1_MDQ45	D14	I/O	GV_{DD}	—
D2_MDQ14/D1_MDQ46	D12	I/O	GV_{DD}	—
D2_MDQ15/D1_MDQ47	E11	I/O	GV_{DD}	—
D2_MDQ16/D1_MDQ48	J15	I/O	GV_{DD}	—
D2_MDQ17/D1_MDQ49	J14	I/O	GV_{DD}	—
D2_MDQ18/D1_MDQ50	K13	I/O	GV_{DD}	—
D2_MDQ19/D1_MDQ51	J12	I/O	GV_{DD}	—
D2_MDQ20/D1_MDQ52	H15	I/O	GV_{DD}	—
D2_MDQ21/D1_MDQ53	G15	I/O	GV_{DD}	—
D2_MDQ22/D1_MDQ54	G13	I/O	GV_{DD}	—
D2_MDQ23/D1_MDQ55	H12	I/O	GV_{DD}	—
D2_MDQ24/D1_MDQ56	C10	I/O	GV_{DD}	—
D2_MDQ25/D1_MDQ57	C8	I/O	GV_{DD}	—
D2_MDQ26/D1_MDQ58	C7	I/O	GV_{DD}	—
D2_MDQ27/D1_MDQ59	B7	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDQ28/D1_MDQ60	B10	I/O	GV_{DD}	—
D2_MDQ29/D1_MDQ61	A10	I/O	GV_{DD}	—
D2_MDQ30/D1_MDQ62	A8	I/O	GV_{DD}	—
D2_MDQ31/D1_MDQ63	A7	I/O	GV_{DD}	—
D2_MDQS0/D1_MDQS4	C12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS0}}$/$\overline{\text{D1\_MDQS4}}$	C13	I/O	GV_{DD}	—
D2_MDQS1/D1_MDQS5	G12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS1}}$/$\overline{\text{D1\_MDQS5}}$	F12	I/O	GV_{DD}	—
D2_MDQS2/D1_MDQS6	J13	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS2}}$/$\overline{\text{D1\_MDQS6}}$	K14	I/O	GV_{DD}	—
D2_MDQS3/D1_MDQS7	D9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS3}}$/$\overline{\text{D1\_MDQS7}}$	C9	I/O	GV_{DD}	—
D2_MDQS8	H9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS8}}$	G9	I/O	GV_{DD}	—
D2_MECC0	G10	I/O	GV_{DD}	—
D2_MECC1	H8	I/O	GV_{DD}	—
D2_MECC2	G8	I/O	GV_{DD}	—
D2_MECC3	F7	I/O	GV_{DD}	—
D2_MECC4	F10	I/O	GV_{DD}	—
D2_MECC5	D8	I/O	GV_{DD}	—
D2_MECC6	E7	I/O	GV_{DD}	—
D2_MECC7	D7	I/O	GV_{DD}	—
D2_MODT0	C1	O	GV_{DD}	—
D2_MODT1	A3	O	GV_{DD}	—
D2_MODT2	H3	O	GV_{DD}	—
D2_MODT3	E1	O	GV_{DD}	—
D2_MAPAR_OUT	F1	O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	G1	I	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	G4	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	E2	O	GV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK0}}$	AF23	O	OV_{DD}	2
$\overline{\text{DMA\_DACK1}}$/MSRCID1	AD27	O	OV_{DD}	11
$\overline{\text{DMA\_DACK2}}$/SD_CMD	AD24	O	OV_{DD}	—
$\overline{\text{DMA\_DDONE0}}$	AD25	O	OV_{DD}	2

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
DMA_DDONE1/MSRCID2	AE24	O	OV_{DD}	2
DMA_DDONE2/SD_WP	AF25	O	OV_{DD}	—
DMA_DREQ0	AG23	I	OV_{DD}	—
DMA_DREQ1/MSRCID0	AE25	I	OV_{DD}	—
DMA_DREQ2/SD_DAT0	AD26	I	OV_{DD}	—
DUART				
UART_SOUT0/DMA_DREQ3/SD_DAT1	AG28	O	OV_{DD}	2
UART_SIN0/DMA_DACK3/SD_DAT2	AF27	I	OV_{DD}	—
UART_CTS0/DMA_DDONE3/SD_DAT3	AG27	I	OV_{DD}	—
UART_RTS0	AH28	O	OV_{DD}	—
Enhanced Local Bus Controller Interface				
LA16	AD15	O	BV_{DD}	2
LA17	AD16	O	BV_{DD}	2
LA18	AE14	O	BV_{DD}	2
LA19	AD17	O	BV_{DD}	2
LA20	AE16	O	BV_{DD}	2
LA21	AD18	O	BV_{DD}	2
LA22	AE17	O	BV_{DD}	11
LA23	AD19	O	BV_{DD}	2
LA24	AE18	O	BV_{DD}	18
LA25	AC20	O	BV_{DD}	18
LA26	AE19	O	BV_{DD}	18
LA27	AE22	O	BV_{DD}	18
LAD0	AG14	I/O	BV_{DD}	23
LAD1	AF14	I/O	BV_{DD}	23
LAD2	AG16	I/O	BV_{DD}	23
LAD3	AH17	I/O	BV_{DD}	23
LAD4	AH18	I/O	BV_{DD}	23
LAD5	AH19	I/O	BV_{DD}	23
LAD6	AG18	I/O	BV_{DD}	23
LAD7	AF20	I/O	BV_{DD}	23
LAD8	AG20	I/O	BV_{DD}	23
LAD9	AH21	I/O	BV_{DD}	23
LAD10	AH22	I/O	BV_{DD}	23
LAD11	AG22	I/O	BV_{DD}	23

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
LAD12	AE21	I/O	BV_{DD}	23
LAD13	AE20	I/O	BV_{DD}	23
LAD14	AF22	I/O	BV_{DD}	23
LAD15	AD21	I/O	BV_{DD}	23
LALE	AH20	O	BV_{DD}	20
LBCTL	AE15	O	BV_{DD}	20
LCLK0	AF18	O	BV_{DD}	11
LCLK1	AF16	O	BV_{DD}	11
$\overline{\text{LCS0}}$	AC18	O	BV_{DD}	2
$\overline{\text{LCS1}}$	AC16	O	BV_{DD}	2
$\overline{\text{LCS2}}$	AB16	O	BV_{DD}	2
$\overline{\text{LCS3}}$	AC14	O	BV_{DD}	21
$\overline{\text{LCS4}}$/IRQ8	AD14	I/O	BV_{DD}	21
$\overline{\text{LCS5}}$/IRQ9	AE23	I/O	BV_{DD}	21
$\overline{\text{LCS6}}$/IRQ10	AD22	I/O	BV_{DD}	21
$\overline{\text{LCS7}}$/IRQ11	AC22	I/O	BV_{DD}	21
LDP0	AB14	I/O	BV_{DD}	—
LDP1	AA15	I/O	BV_{DD}	—
LGPL0/LFCLE	AA19	O	BV_{DD}	2
LGPL1/LFALE	AA17	O	BV_{DD}	2
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AD20	O	BV_{DD}	20
LGPL3/$\overline{\text{LFWP}}$	AA20	O	BV_{DD}	2
LGPL4/LUPWAIT/LBPBSE/$\overline{\text{LFRB}}$	AA18	I/O	BV_{DD}	29
LGPL5	AA16	O	BV_{DD}	2
LSYNC_IN	AH16	I	BV_{DD}	—
LSYNC_OUT	AH15	O	BV_{DD}	—
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$LFWE	AB20	O	BV_{DD}	11
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$	AB18	O	BV_{DD}	24
I^2C				
IIC1_SDA	AH26	I/O	OV_{DD}	5, 28
IIC1_SCL	AG26	I/O	OV_{DD}	5, 28
IIC2_SDA/SD_CLK	AG25	I/O	OV_{DD}	3
IIC2_SCL/$\overline{\text{SD\_CD}}$	AF26	I/O	OV_{DD}	3
JTAG				
TCK	N21	I	OV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
TDI	P21	I	OV_{DD}	26
TDO	P23	O	OV_{DD}	25
TMS	N22	I	OV_{DD}	26
$\overline{\text{TRST}}$	P22	I	OV_{DD}	26
Programmable Interrupt Controller				
IRQ0	R20	I	OV_{DD}	—
IRQ1	T21	I	OV_{DD}	—
IRQ2	R26	I	OV_{DD}	—
IRQ3	R25	I	OV_{DD}	—
IRQ4/MSRCID3	N20	I	OV_{DD}	—
IRQ5/MSRCID4	R21	I	OV_{DD}	—
IRQ6/MDVAL	R22	I	OV_{DD}	—
$\overline{\text{IRQ\_OUT}}$	M20	O	OV_{DD}	5, 6, 11
$\overline{\text{MCP}}$	M22	I	OV_{DD}	6
$\overline{\text{UDE}}$	M21	I	OV_{DD}	6
QUICC Engine Block				
QE_PA0	T11	I/O	$LV_{DD}1$	—
QE_PA1	U11	I/O	$LV_{DD}1$	—
QE_PA2	R11	I/O	$LV_{DD}1$	—
QE_PA3	U10	I/O	$LV_{DD}1$	—
QE_PA4	R10	I/O	$LV_{DD}1$	—
QE_PA5	V11	I/O	OV_{DD}	—
QE_PA6	R9	I/O	$LV_{DD}1$	—
QE_PA7	U9	I/O	$LV_{DD}1$	—
QE_PA8	T8	I/O	$LV_{DD}1$	—
QE_PA9	U8	I/O	$LV_{DD}1$	—
QE_PA10	V10	I/O	OV_{DD}	—
QE_PA11	V9	I/O	OV_{DD}	—
QE_PA12	R8	I/O	$LV_{DD}1$	—
QE_PA13	V8	I/O	OV_{DD}	—
QE_PA14	P7	I/O	$LV_{DD}2$	—
QE_PA15	L6	I/O	$LV_{DD}2$	—
QE_PA16	M6	I/O	$LV_{DD}2$	—
QE_PA17	N6	I/O	$LV_{DD}2$	—
QE_PA18	L5	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PA19	P1	I/O	OV_{DD}	—
QE_PA20	M5	I/O	$LV_{DD}2$	—
QE_PA21	N5	I/O	$LV_{DD}2$	—
QE_PA22	L4	I/O	$LV_{DD}2$	—
QE_PA23	M4	I/O	$LV_{DD}2$	—
QE_PA24	N1	I/O	OV_{DD}	—
QE_PA25	R1	I/O	OV_{DD}	—
QE_PA26	N4	I/O	$LV_{DD}2$	—
QE_PA27	T1	I/O	OV_{DD}	—
QE_PA28	N2	I/O	OV_{DD}	—
QE_PA29	P6	I/O	$LV_{DD}1$	—
QE_PA30	U6	I/O	$LV_{DD}1$	—
QE_PA31	T5	I/O	$LV_{DD}1$	—
QE_PB0	R5	I/O	$LV_{DD}1$	—
QE_PB1	P5	I/O	$LV_{DD}1$	—
QE_PB2	V6	I/O	OV_{DD}	—
QE_PB3	T3	I/O	$LV_{DD}1$	—
QE_PB4	U3	I/O	$LV_{DD}1$	—
QE_PB5	U4	I/O	$LV_{DD}1$	—
QE_PB6	U5	I/O	$LV_{DD}1$	—
QE_PB7	V3	I/O	OV_{DD}	11
QE_PB8	V4	I/O	OV_{DD}	—
QE_PB9	P4	I/O	$LV_{DD}1$	—
QE_PB10	V5	I/O	OV_{DD}	—
QE_PB11	W11	I/O	OV_{DD}	—
QE_PB12	L11	I/O	$LV_{DD}2$	—
QE_PB13	M11	I/O	$LV_{DD}2$	—
QE_PB14	N11	I/O	$LV_{DD}2$	—
QE_PB15	P11	I/O	$LV_{DD}2$	—
QE_PB16	P10	I/O	$LV_{DD}2$	—
QE_PB17	P2	I/O	OV_{DD}	—
QE_PB18	L10	I/O	$LV_{DD}2$	—
QE_PB19	M9	I/O	$LV_{DD}2$	—
QE_PB20	N9	I/O	$LV_{DD}2$	—
QE_PB21	P9	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PB22	T2	I/O	OV_{DD}	—
QE_PB23	R2	I/O	OV_{DD}	—
QE_PB24	P8	I/O	$LV_{DD}2$	—
QE_PB25	U2	I/O	OV_{DD}	—
QE_PB26	AG13	I/O	OV_{DD}	11
QE_PB27	AH14	I/O	OV_{DD}	22
QE_PB28	AC8	I/O	OV_{DD}	22
QE_PB29	AD8	I/O	OV_{DD}	—
QE_PB30	AD9	I/O	OV_{DD}	—
QE_PB31	AD10	I/O	OV_{DD}	11
QE_PC0	W3	I/O	OV_{DD}	—
QE_PC1	W4	I/O	OV_{DD}	—
QE_PC2	N3	I/O	$LV_{DD}2$	—
QE_PC3	L3	I/O	$LV_{DD}2$	—
QE_PC4	Y7	I/O	OV_{DD}	22
QE_PC5	W2	I/O	OV_{DD}	—
QE_PC6	W5	I/O	OV_{DD}	—
QE_PC7	W7	I/O	OV_{DD}	—
QE_PC8	T7	I/O	$LV_{DD}1$	—
QE_PC9	R3	I/O	$LV_{DD}1$	—
QE_PC10	AB2	I/O	OV_{DD}	—
QE_PC11	R7	I/O	$LV_{DD}1$	—
QE_PC12	AA6	I/O	OV_{DD}	—
QE_PC13	AA3	I/O	OV_{DD}	—
QE_PC14	AA5	I/O	OV_{DD}	—
QE_PC15	AA4	I/O	OV_{DD}	—
QE_PC16	L7	I/O	$LV_{DD}2$	—
QE_PC17	M8	I/O	$LV_{DD}2$	—
QE_PC18	AB3	I/O	OV_{DD}	—
QE_PC19	Y5	I/O	OV_{DD}	—
QE_PC20	U7	I/O	$LV_{DD}1$	—
QE_PC21	AB1	I/O	OV_{DD}	—
QE_PC22	Y3	I/O	OV_{DD}	—
QE_PC23	Y4	I/O	OV_{DD}	—
QE_PC24	N8	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PC25	P3	I/O	$LV_{DD}1$	—
QE_PC26	W8	I/O	OV_{DD}	—
QE_PC27	W9	I/O	OV_{DD}	—
QE_PC28	AF13	I/O	OV_{DD}	—
QE_PC29	V7	I/O	OV_{DD}	—
QE_PC30	AA14	I/O	OV_{DD}	—
QE_PC31	AA13	I/O	OV_{DD}	—
QE_PD0	AH6	I/O	OV_{DD}	11
QE_PD1	AF6	I/O	OV_{DD}	—
QE_PD2	AG6	I/O	OV_{DD}	—
QE_PD3	AF5	I/O	OV_{DD}	—
QE_PD4	AE4	I/O	OV_{DD}	22
QE_PD5	AD4	I/O	OV_{DD}	—
QE_PD6	AB6	I/O	OV_{DD}	—
QE_PD7	AD7	I/O	OV_{DD}	—
QE_PD8	AC6	I/O	OV_{DD}	—
QE_PD9	AD6	I/O	OV_{DD}	—
QE_PD10	AB5	I/O	OV_{DD}	—
QE_PD11	AC4	I/O	OV_{DD}	—
QE_PD12	AE5	I/O	OV_{DD}	—
QE_PD13	AE6	I/O	OV_{DD}	—
QE_PD14	AC7	I/O	OV_{DD}	—
QE_PD15	AB7	I/O	OV_{DD}	—
QE_PD16	AB8	I/O	OV_{DD}	—
QE_PD17	AA9	I/O	OV_{DD}	—
QE_PD18	Y8	I/O	OV_{DD}	—
QE_PD19	AA8	I/O	OV_{DD}	—
QE_PD20	AA12	I/O	OV_{DD}	—
QE_PD21	Y11	I/O	OV_{DD}	—
QE_PD22	AA11	I/O	OV_{DD}	—
QE_PD23	AB11	I/O	OV_{DD}	—
QE_PD24	AA7	I/O	OV_{DD}	—
QE_PD25	AB10	I/O	OV_{DD}	—
QE_PD26	Y9	I/O	OV_{DD}	—
QE_PD27	AA10	I/O	OV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PD28	AF1	I/O	OV_{DD}	—
QE_PD29	AG1	I/O	OV_{DD}	—
QE_PD30	AG2	I/O	OV_{DD}	—
QE_PD31	AH1	I/O	OV_{DD}	—
QE_PE0	AH2	I/O	OV_{DD}	—
QE_PE1	AH3	I/O	OV_{DD}	—
QE_PE2	AF4	I/O	OV_{DD}	—
QE_PE3	AG4	I/O	OV_{DD}	—
QE_PE4	AF3	I/O	OV_{DD}	—
QE_PE5	AE3	I/O	OV_{DD}	—
QE_PE6	AG3	I/O	OV_{DD}	—
QE_PE7	AH5	I/O	OV_{DD}	—
QE_PE8	AH4	I/O	OV_{DD}	—
QE_PE9	AG5	I/O	OV_{DD}	—
QE_PE10	AA1	I/O	OV_{DD}	—
QE_PE11	Y1	I/O	OV_{DD}	—
QE_PE12	AC1	I/O	OV_{DD}	—
QE_PE13	AC2	I/O	OV_{DD}	—
QE_PE14	V1	I/O	OV_{DD}	—
QE_PE15	AB4	I/O	OV_{DD}	—
QE_PE16	W1	I/O	OV_{DD}	—
QE_PE17	V2	I/O	OV_{DD}	—
QE_PE18	AC3	I/O	OV_{DD}	—
QE_PE19	AD2	I/O	OV_{DD}	—
QE_PE20	AD3	I/O	OV_{DD}	—
QE_PE21	AD1	I/O	OV_{DD}	—
QE_PE22	U1	I/O	OV_{DD}	—
QE_PE23	AE1	I/O	OV_{DD}	—
QE_PE24	AC12	I/O	OV_{DD}	11
QE_PE25	AB12	I/O	OV_{DD}	2
QE_PE26	AB13	I/O	OV_{DD}	11
QE_PE27	AH11	I/O	OV_{DD}	19
QE_PE28	AG10	I/O	OV_{DD}	19

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PE29	AH10	I/O	OV_{DD}	19
QE_PE30	AG11	I/O	OV_{DD}	—
QE_PE31	AE7	I/O	OV_{DD}	—
QE_PF0	AF8	I/O	OV_{DD}	—
QE_PF1	AG8	I/O	OV_{DD}	—
QE_PF2	AE8	I/O	OV_{DD}	—
QE_PF3	AE13	I/O	OV_{DD}	—
QE_PF4	AC13	I/O	OV_{DD}	—
QE_PF5	AD13	I/O	OV_{DD}	—
QE_PF6	AF12	I/O	OV_{DD}	—
QE_PF7	AE12	I/O	OV_{DD}	—
QE_PF8	AG12	I/O	OV_{DD}	—
QE_PF9	AD12	I/O	OV_{DD}	2
QE_PF10	AC10	I/O	OV_{DD}	2
QE_PF11	AC11	I/O	OV_{DD}	2
QE_PF12	AD11	I/O	OV_{DD}	—
QE_PF13	AH12	I/O	OV_{DD}	11
QE_PF14	AH13	I/O	OV_{DD}	2
QE_PF15	AE10	I/O	OV_{DD}	—
QE_PF16	AE9	I/O	OV_{DD}	—
QE_PF17	AF9	I/O	OV_{DD}	—
QE_PF18	AF10	I/O	OV_{DD}	—
QE_PF19	AH8	I/O	OV_{DD}	—
QE_PF20	AH7	I/O	OV_{DD}	—
QE_PF21	AG9	I/O	OV_{DD}	—
QE_PF22	AH9	I/O	OV_{DD}	—
SerDes				
SD_IMP_CAL_RX	W22	I	—	7
SD_IMP_CAL_TX	AA25	I	—	17
SD_PLL_TPA	AA26	O	AV_{DD}_SRDS	8
SD_PLL_TPD	W21	O	XV_{DD}	8
SD_REF_CLK	W26	I	ScoreVDD	—
$\overline{\text{SD\_REF\_CLK}}$	W25	I	ScoreVDD	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SD_RX0	T28	I	ScoreVDD	30
$\overline{\text{SD\_RX0}}$	T27	I	ScoreVDD	30
SD_RX1	V28	I	ScoreVDD	30
$\overline{\text{SD\_RX1}}$	V27	I	ScoreVDD	30
SD_RX2	Y28	I	ScoreVDD	30
$\overline{\text{SD\_RX2}}$	Y27	I	ScoreVDD	30
SD_RX3	AB28	I	ScoreVDD	30
$\overline{\text{SD\_RX3}}$	AB27	I	ScoreVDD	30
SD_TX0	T23	O	XV_{DD}	31
$\overline{\text{SD\_TX0}}$	T24	O	XV_{DD}	31
SD_TX1	V23	O	XV_{DD}	31
$\overline{\text{SD\_TX1}}$	V24	O	XV_{DD}	31
SD_TX2	Y23	O	XV_{DD}	31
$\overline{\text{SD\_TX2}}$	Y24	O	XV_{DD}	31
SD_TX3	AB23	O	XV_{DD}	31
$\overline{\text{SD\_TX3}}$	AB24	O	XV_{DD}	31
SD_TX_CLK	AA21	O	XV_{DD}	8
$\overline{\text{SD\_TX\_CLK}}$	AA22	O	XV_{DD}	8
System Control				
$\overline{\text{CKSTP\_IN}}$	AE28	I	OV_{DD}	4
$\overline{\text{CKSTP\_OUT}}$	AF28	O	OV_{DD}	5, 6, 11
$\overline{\text{HRESET}}$	AD23	I	OV_{DD}	4
$\overline{\text{HRESET\_REQ}}$	AC26	O	OV_{DD}	11
$\overline{\text{SRESET}}$	AC25	I	OV_{DD}	4
Debug				
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	P24	O	OV_{DD}	11
CLK_OUT	M24	O	OV_{DD}	—
TRIG_IN	N25	I	OV_{DD}	—
Voltage Control				
LVDD_VSEL0	AD28	I	OV_{DD}	15
LVDD_VSEL1	P26	I	OV_{DD}	16
BVDD_VSEL0	N26	I	OV_{DD}	14
BVDD_VSEL1	P20	I	OV_{DD}	14
Design for Test				
$\overline{\text{LSSD\_MODE}}$	AH27	I	OV_{DD}	10

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
Power Management				
ASLEEP	M23	O	OV_{DD}	11
Thermal Management				
THERM0	U21	—	Internal temperature diode cathode	32
THERM1	U20	—	Internal temperature diode anode	32
Reserved	T22	—	—	9
Analog				
D1_MVREF	N27	Reference voltage for DDR	MV_{REF}	—
D2_MVREF	J1			—
Power and Ground				
V_{DD}	L13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P16	1.0-V/1.1-V core power supply	V_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	P18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W19	1.0-V/1.1-V core power supply	V_{DD}	—