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MPC8572E PowerQUICC III Integrated Processor Hardware Specifications

1 Overview

This section provides a high-level overview of the features of the MPC8572E processor. [Figure 1](#) shows the major functional units within the MPC8572E.

1.1 Key Features

The following list provides an overview of the MPC8572E feature set:

- Two high-performance, 32-bit, Book E-enhanced cores that implement the Power Architecture® technology:
 - Each core is identical to the core within the MPC8572E processor.
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
 - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both

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the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the MPC8572E performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operation.

- 1 Mbyte L2 cache/SRAM
 - Shared by both cores.
 - Flexible configuration and individually configurable per core.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - Per-way allocation of cache region to a given processor.
 - SRAM features include the following:
 - 1, 2, 4, or 8 ways can be configured as SRAM.
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Address translation and mapping unit (ATMU)
 - Twelve local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.

- Three inbound windows plus a configuration window on PCI Express
- Four inbound windows plus a default window on Serial RapidIO®
- Four outbound windows plus default translation for PCI Express
- Eight outbound windows plus default translation for Serial RapidIO with segmentation and sub-segmentation support
- Two 64-bit DDR2/DDR3 memory controllers
 - Programmable timing supporting DDR2 and DDR3 SDRAM
 - 64-bit data interface per controller
 - Four banks of memory supported, each up to 4 Gbytes, for a maximum of 16 Gbytes per controller
 - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
 - Full ECC support
 - Page mode support
 - Up to 32 simultaneous open pages for DDR2 or DDR3
 - Contiguous or discontinuous memory mapping
 - Cache line, page, bank, and super-bank interleaving between memory controllers
 - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
 - Sleep mode support for self-refresh SDRAM
 - On-die termination support when using DDR2 or DDR3
 - Supports auto refreshing
 - On-the-fly power management using CKE signal
 - Registered DIMM support
 - Fast memory access through JTAG port
 - 1.8-V SSTL_1.8 compatible I/O
 - Support 1.5-V operation for DDR3. The detail is TBD pending on official release of appropriate industry specifications.
 - Support for battery-backed main memory
- Programmable interrupt controller (PIC)
 - Programming model is compliant with the OpenPIC architecture.
 - Supports 16 programmable interrupt and processor task priority levels
 - Supports 12 discrete external interrupts
 - Supports 4 message interrupts per processor with 32-bit messages
 - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
 - Four global high resolution timers/counters per processor that can generate interrupts
 - Supports a variety of other internal interrupt sources

- Supports fully nested interrupt delivery
- Interrupts can be routed to external pin for external processing.
- Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
- Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPsec, IKE, SSL/TLS, SRTP, 802.16e, and 3GPP
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
 - PKEU—public key execution unit
 - RSA and Diffie-Hellman; programmable field size up to 4096 bits
 - Elliptic curve cryptography with F_{2^m} and $F(p)$ modes and programmable field size up to 1023 bits
 - DEU—Data Encryption Standard execution unit
 - DES, 3DES
 - Two key (K1, K2, K1) or three key (K1, K2, K3)
 - ECB, CBC and OFB-64 modes for both DES and 3DES
 - AESU—Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, CCM, GCM, CMAC, OFB-128, CFB-128, and LRW modes
 - 128-, 192-, and 256-bit key lengths
 - AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - MDEU—message digest execution unit
 - SHA-1 with 160-bit message digest
 - SHA-2 (SHA-256, SHA-384, SHA-512)
 - MD5 with 128-bit message digest
 - HMAC with all algorithms
 - KEU—Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
 - RNG—random number generator
 - XOR engine for parity checking in RAID storage applications
 - CRC execution unit
 - CRC-32 and CRC-32C
- Pattern Matching Engine with DEFLATE decompression

- Regular expression (regex) pattern matching
 - Built-in case insensitivity, wildcard support, no pattern explosion
 - Cross-packet pattern detection
 - Fast pattern database compilation and fast incremental updates
 - 16000 patterns, each up to 128 bytes in length
 - Patterns can be split into 256 sets, each of which can contain 16 subsets
- Stateful rule engine enables hardware execution of state-aware logic when a pattern is found
 - Useful for contextual searches, multi-pattern signatures, or for performing additional checks after a pattern is found
 - Capable of capturing and utilizing data from the data stream (such as LENGTH field) and using that information in subsequent pattern searches (for example, positive match only if pattern is detected within the number of bytes specified in the LENGTH field)
 - 8192 stateful rules
- Deflate engine
 - Supports decompression of DEFLATE compression format including zlib and gzip
 - Can work independently or in conjunction with the Pattern Matching Engine (that is decompressed data can be passed directly to the Pattern Matching Engine without further software involvement or memory copying)
- Two Table Lookup Units (TLU)
 - Hardware-based lookup engine offloads table searches from e500 cores
 - Longest prefix match, exact match, chained hash, and flat data table formats
 - Up to 32 tables, with each table up to 16M entries
 - 32-, 64-, 96-, or 128-bit keys
- Two I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Enhanced local bus controller (eLBC)

- Multiplexed 32-bit address and data bus operating at up to 150 MHz
- Eight chip selects support eight external slaves
- Up to 8-beat burst transfers
- The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
- Three protocol engines available on a per-chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - NAND Flash control machine (FCM)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Four IEEE Std 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, RGMII, and SGMII
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
 - Flexible configuration for multiple PHY interface configurations
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (Q-in-Q) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision

- CRC generation and verification of inbound/outbound frames
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported
 - Broadcast address (accept/reject)
 - Hash table match on up to 512 multicast addresses
 - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- Two MII management interfaces for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- 10/100 Fast Ethernet controller (FEC) management interface
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII for system management
 - Note: When enabled, the FEC occupies eTSEC3 and eTSEC4 parallel interface signals. In such a mode, eTSEC3 and eTSEC4 are only available through SGMII interfaces.
- OCeaN switch fabric
 - Full crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Two integrated DMA controllers
 - Four DMA channels per controller
 - All channels accessible by the local masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no snoop)
 - Ability to start and flow control up to 4 (both Channel 0 and 1 for each DMA Controller) of the 8 total DMA channels from external 3-pin interface by the remote masters
 - The Channel 2 of DMA Controller 2 is only allowed to initiate and start a DMA transfer by the remote master, because only one of the 3-external pins (DMA2_DREQ[2]) is made available

- Ability to launch DMA from single write transaction
- Serial RapidIO interface unit
 - Supports *RapidIO Interconnect Specification, Revision 1.2*
 - Both 1x and 4x LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto-detection of 1x- and 4x-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compliant message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox
 - Single inbound doorbell message structure
 - Facility to accept port-write messages

- Three PCI Express controllers
 - PCI Express 1.0a compatible
 - Supports x8, x4, x2, and x1 link widths (see following bullet for specific width configuration options)
 - Auto-detection of number of connected lanes
 - Selectable operation as root complex or endpoint
 - Both 32- and 64-bit addressing
 - 256-byte maximum payload size
 - Virtual channel 0 only
 - Full 64-bit decode with 36-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
 - Single x8/x4/x2/x1 PCI Express
 - Dual x4/x2/x1 PCI Express
 - Single x4/x2/x1 PCI Express and dual x2/x1 PCI Express
 - Single 1x/4x Serial RapidIO and single x4/x2/x1 PCI Express
- Power management
 - Supports power saving modes: doze, nap, and sleep
 - Employs dynamic power management, that automatically minimizes power consumption of blocks when they are idle
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the eight counters
 - Supports duration and quantity threshold counting
 - Permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™ compatible, JTAG boundary scan
- 1023 FC-PBGA package

Figure 1 shows the MPC8572E block diagram.

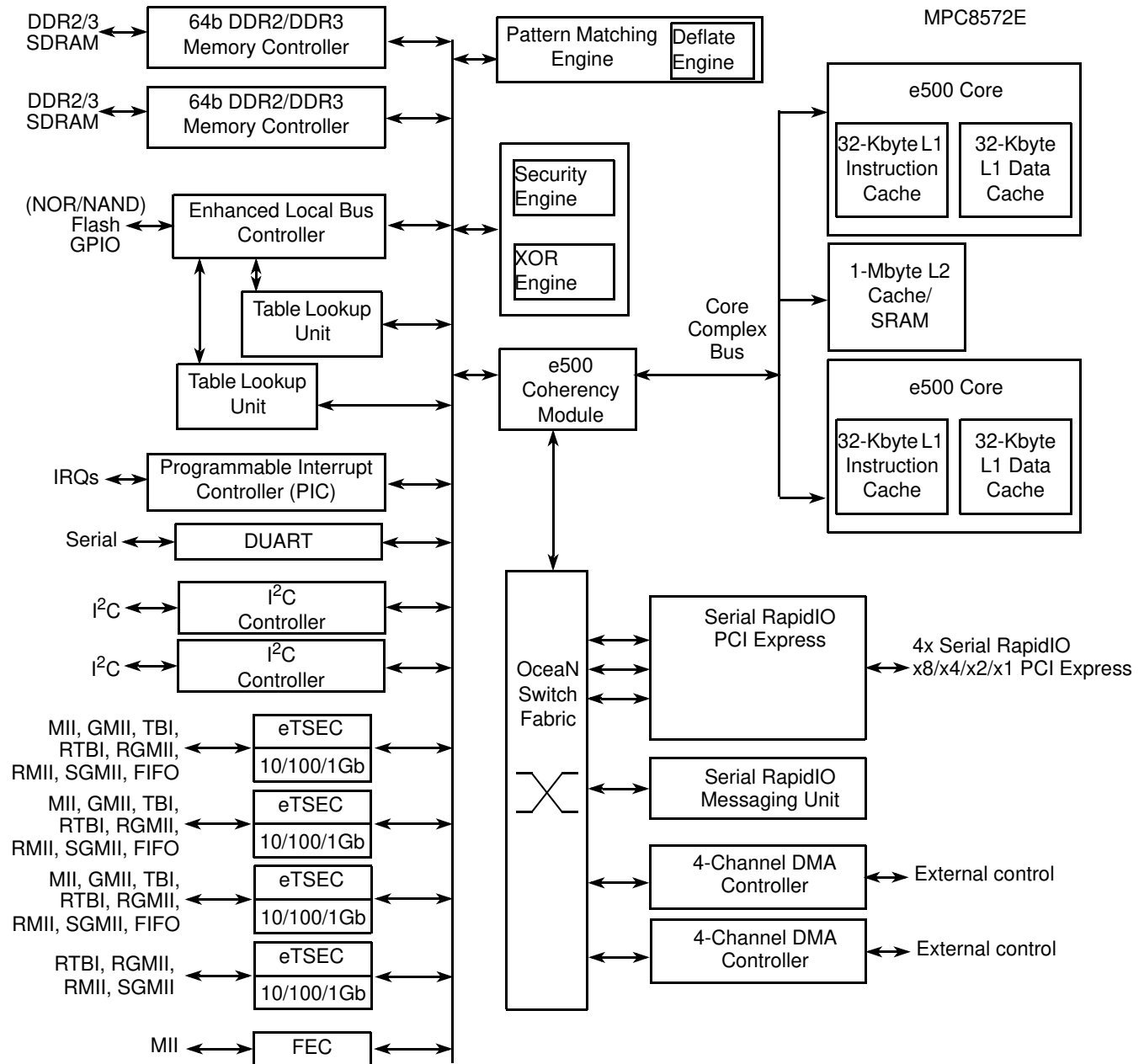


Figure 1. MPC8572E Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8572E. The MPC8572E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic		Symbol	Range	Unit	Notes
Core supply voltage		V_{DD}	-0.3 to 1.21	V	—
PLL supply voltage		AV_{DD}	-0.3 to 1.21	V	—
Core power supply for SerDes transceivers		SV_{DD}	-0.3 to 1.21	V	—
Pad power supply for SerDes transceivers		XV_{DD}	-0.3 to 1.21	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	-0.3 to 1.98	V	—
	DDR3 SDRAM Interface	—	-0.3 to 1.65		—
Three-speed Ethernet I/O, FEC management interface, MII management voltage		LV_{DD} (for eTSEC1 and eTSEC2)	-0.3 to 3.63 -0.3 to 2.75	V	2
		TV_{DD} (for eTSEC3 and eTSEC4, FEC)	-0.3 to 3.63 -0.3 to 2.75	—	2
DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	-0.3 to 3.63	V	—
Local bus and GPIO I/O voltage		BV_{DD}	-0.3 to 3.63 -0.3 to 2.75 -0.3 to 1.98	V	—
Input voltage	DDR2 and DDR3 SDRAM interface signals	MV_{IN}	-0.3 to ($GV_{DD} + 0.3$)	V	3
	DDR2 and DDR3 SDRAM interface reference	MV_{REF}^n	-0.3 to ($GV_{DD}/2 + 0.3$)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	-0.3 to ($LV_{DD} + 0.3$) -0.3 to ($TV_{DD} + 0.3$)	V	3
	Local bus and GPIO signals	BV_{IN}	-0.3 to ($BV_{DD} + 0.3$)	—	—
	DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	3
Storage temperature range		T_{STG}	-55 to 150	°C	—

Notes:

- Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,” for details on the recommended operating conditions per protocol.
- (M,L,O) V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values shown are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.1 V \pm 55 mV	V	—
PLL supply voltage		AV_{DD}	1.1 V \pm 55 mV	V	1
Core power supply for SerDes transceivers		SV_{DD}	1.1 V \pm 55 mV	V	—
Pad power supply for SerDes transceivers		XV_{DD}	1.1 V \pm 55 mV	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	1.8 V \pm 90 mV	V	—
	DDR3 SDRAM Interface		1.5 V \pm 75 mV		—
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V \pm 165 mV 2.5 V \pm 125 mV	V	4
		TV_{DD}	3.3 V \pm 165 mV 2.5 V \pm 125 mV		4
DUART, system control and power management, I ² C, and JTAG I/O voltage		OV_{DD}	3.3 V \pm 165 mV	V	3
Local bus and GPIO I/O voltage		BV_{DD}	3.3 V \pm 165 mV 2.5 V \pm 125 mV 1.8 V \pm 90 mV	V	—
Input voltage	DDR2 and DDR3 SDRAM Interface signals	MV_{IN}	GND to GV_{DD}	V	2
	DDR2 and DDR3 SDRAM Interface reference	MV_{REF}^n	$GV_{DD}/2 \pm 1\%$	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4
	Local bus and GPIO signals	BV_{IN}	GND to BV_{DD}	V	—
	Local bus, DUART, SYSCLK, Serial RapidIO, system control and power management, I ² C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3
Junction temperature range		T_J	0 to 105	°C	—

Notes:

1. This voltage is the input to the filter discussed in Section 21.2.1, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, that may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 2 shows the overshoot and undershoot voltages at the interfaces of the MPC8572E.

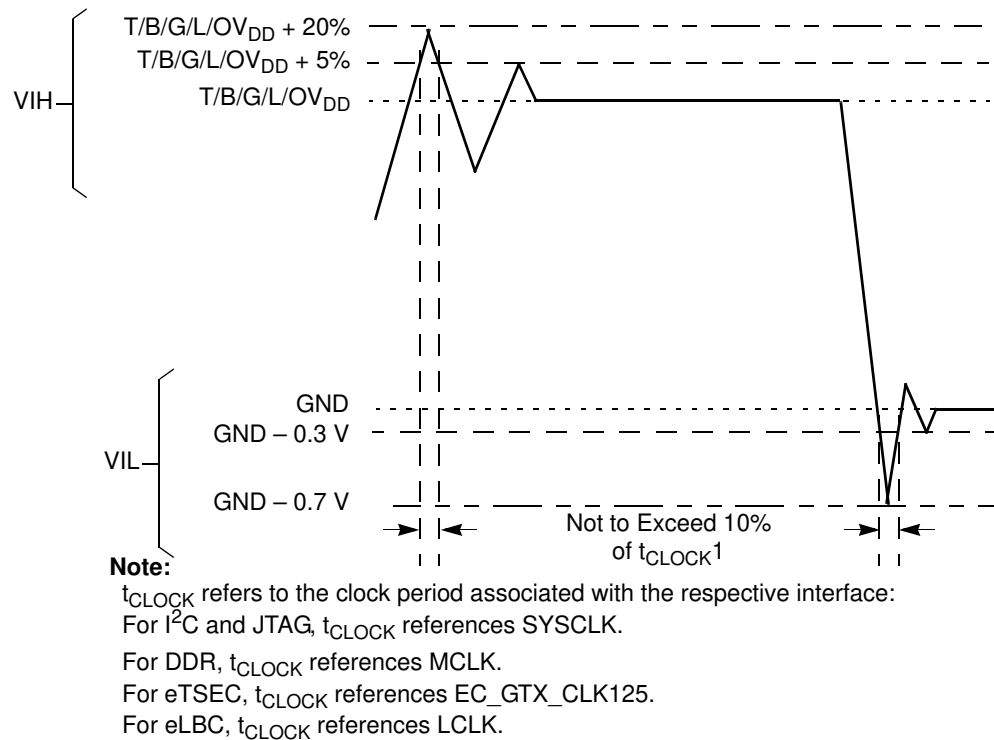


Figure 2. Overshoot/Undershoot Voltage for $T_{V_{DD}}/B_{V_{DD}}/G_{V_{DD}}/L_{V_{DD}}/O_{V_{DD}}$

The core voltage must always be provided at nominal 1.1 V. (See Table 2 for actual recommended core voltage.) Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. $T_{V_{DD}}$, $B_{V_{DD}}$, $O_{V_{DD}}$, and $L_{V_{DD}}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied MV_{REF^n} signal (nominally set to $G_{V_{DD}}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	$BV_{DD} = 3.3\text{ V}$ $BV_{DD} = 2.5\text{ V}$	1
	45(default) 45(default) 125	$BV_{DD} = 3.3\text{ V}$ $BV_{DD} = 2.5\text{ V}$ $BV_{DD} = 1.8\text{ V}$	
DDR2 signal	18 36 (half strength mode)	$GV_{DD} = 1.8\text{ V}$	2
DDR3 signal	20 40 (half strength mode)	$GV_{DD} = 1.5\text{ V}$	2
eTSEC/10/100 signals	45	$L/TV_{DD} = 2.5/3.3\text{ V}$	—
DUART, system control, JTAG	45	$OV_{DD} = 3.3\text{ V}$	—
I2C	150	$OV_{DD} = 3.3\text{ V}$	—

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at $T_j = 105^\circ\text{C}$ and at GV_{DD} (min).

2.2 Power Sequencing

The MPC8572E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD} , AV_{DD-n} , BV_{DD} , LV_{DD} , OV_{DD} , SV_{DD_SRDS1} and SV_{DD_SRDS2} , TV_{DD} , XV_{DD_SRDS1} and XV_{DD_SRDS2}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

To guarantee MCKE low during power-on reset, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-on reset, then the sequencing for GV_{DD} is not required.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-on reset, and extra current may be drawn by the device.

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with out the L in its part ordering is shown in [Table 4](#).

Table 4. MPC8572E Power Dissipation ¹

CCB Frequency	Core Frequency	Typical-65 ²	Typical-105 ³	Maximum ⁴	Unit
533	1067	12.3	17.8	18.5	W
533	1200	12.3	17.8	18.5	W
533	1333	16.3	22.8	24.5	W
600	1500	17.3	23.9	25.9	W

Notes:

- ¹ This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.
- ² Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.
- ³ Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.
- ⁴ Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices with the L in its port ordering is shown in [Table 5](#).

Table 5. MPC8572EL Power Dissipation ¹

CCB Frequency	Core Frequency	Typical-65 ²	Typical-105 ³	Maximum ⁴	Unit
533	1067	12	15	15.8	W
533	1200	12	15.5	16.3	W
533	1333	12	15.9	16.9	W
600	1500	13	18.7	20.0	W

Notes:

- ¹ This reflects the MPC8572E power dissipation excluding the power dissipation from B/G/L/O/T/XV_{DD} rails.
- ² Typical-65 is based on V_{DD} = 1.1 V, T_j = 65 °C, running Dhrystone.
- ³ Typical-105 is based on V_{DD} = 1.1 V, T_j = 105 °C, running Dhrystone.
- ⁴ Maximum is based on V_{DD} = 1.1 V, T_j = 105 °C, running a smoke test.

4 Input Clocks

4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) AC timing specifications for the MPC8572E.

Table 6. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” and Section 19.3, “e500 Core PLL Ratio,” for ratio settings.
- Rise and fall times for SYSCLK are measured at 0.6 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The SYSCLK driver’s closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on SYSCLK.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8572E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with $L_{V_{DD}}/TV_{DD}$ of $3.3V \pm 5\%$ or $2.5V \pm 5\%$

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time L/TV _{DD} =2.5V L/TV _{DD} =3.3V	t_{G125R} , t_{G125F}	—	—	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	45 47	—	55 53	%	2, 3

Notes:

- Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TV_{DD}=2.5V, and from 0.6V and 2.7V for L/TV_{DD}=3.3V.
- Timing is guaranteed by design and characterization.
- EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC_n_GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 DDR Clock Timing

Table 8 provides the DDR clock (DDRCLK) AC timing specifications for the MPC8572E.

Table 8. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66	—	100	MHz	1
DDRCLK cycle time	t_{DDRCLK}	10.0	—	15.15	ns	—
DDRCLK rise and fall time	t_{KH} , t_{KL}	0.6	1.0	1.2	ns	2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	3

Table 8. DDRCLK AC Timing Specifications (continued)

 At recommended operating conditions with OV_{DD} of $3.3V \pm 5\%$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK jitter	—	—	—	+/- 150	ps	4, 5, 6

Notes:

- Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to [Section 19.4, “DDR/DDRCLK PLL Ratio,”](#) for ratio settings.
- Rise and fall times for DDRCLK are measured at 0.6 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The DDRCLK driver’s closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track DDRCLK drivers with the specified jitter.
- For spread spectrum clocking, guidelines are +0% to -1% down spread at a modulation rate between 20 kHz and 60 kHz on DDRCLK.

4.5 Platform to eTSEC FIFO Restrictions

Note the following eTSEC FIFO mode maximum speed restrictions based on platform (CCB) frequency.

For FIFO GMII modes (both 8 and 16 bit) and 16-bit encoded FIFO mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock (CCB) frequency} / 4.2$$

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz.

For 8-bit encoded FIFO mode:

$$\text{FIFO TX/RX clock frequency} \leq \text{platform clock (CCB) frequency} / 3.2$$

For example, if the platform (CCB) frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the respective sections of this document.

5 RESET Initialization

[Table 9](#) describes the AC electrical specifications for the RESET initialization timing.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	2
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYCLKs	1

Table 9. RESET Initialization Timing Specifications (continued)

PLL config input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:

1. SYSCLK is the primary clock input for the MPC8572E.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Symbol	Min	Typical	Max
PLL lock times	—	100	μs	—
Local bus PLL	—	50	μs	—

6 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8572E. Note that the required $\text{GV}_{\text{DD}}(\text{typ})$ voltage is 1.8V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM, respectively.

6.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR2 SDRAM.

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for $\text{GV}_{\text{DD}}(\text{typ}) = 1.8 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	$\text{MV}_{\text{REF}n}$	$0.49 \times \text{GV}_{\text{DD}}$	$0.51 \times \text{GV}_{\text{DD}}$	V	2
I/O termination voltage	V_{TT}	$\text{MV}_{\text{REF}n} - 0.04$	$\text{MV}_{\text{REF}n} + 0.04$	V	3
Input high voltage	V_{IH}	$\text{MV}_{\text{REF}n} + 0.125$	$\text{GV}_{\text{DD}} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$\text{MV}_{\text{REF}n} - 0.125$	V	—
Output leakage current	I_{OZ}	-50	50	μA	4
Output high current ($\text{V}_{\text{OUT}} = 1.420 \text{ V}$)	I_{OH}	-13.4	—	mA	—

Table 11. DDR2 SDRAM Interface DC Electrical Characteristics for $GV_{DD}(typ) = 1.8\text{ V}$ (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current ($V_{OUT} = 0.280\text{ V}$)	I_{OL}	13.4	—	mA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REFn} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REFn} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to that far end signal termination is made and is expected to be equal to MV_{REFn} . This rail should track variations in the DC level of MV_{REFn} .
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 12 provides the recommended operating conditions for the DDR SDRAM controller of the MPC8572E when interfacing to DDR3 SDRAM.

Table 12. DDR3 SDRAM Interface DC Electrical Characteristics for $GV_{DD}(typ) = 1.5\text{ V}$

Parameter/Condition	Symbol	Min	Typical	Max	Unit
I/O supply voltage	GV_{DD}	1.425	1.575	V	1
I/O reference voltage	MV_{REFn}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
Input high voltage	V_{IH}	$MV_{REFn} + 0.100$	GV_{DD}	V	—
Input low voltage	V_{IL}	GND	$MV_{REFn} - 0.100$	V	—
Output leakage current	I_{OZ}	-50	50	μA	3

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REFn} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REFn} may not exceed $\pm 1\%$ of the DC value.
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 13 provides the DDR SDRAM controller interface capacitance for DDR2 and DDR3.

Table 13. DDR2 and DDR3 SDRAM Interface Capacitance for $GV_{DD}(typ)=1.8\text{ V}$ and 1.5 V

Parameter/Condition	Symbol	Min	Typical	Max	Unit
Input/output capacitance: DQ, DQS, \overline{DQS}	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, \overline{DQS}	C_{DIO}	—	0.5	pF	1, 2

Note:

- This parameter is sampled. $GV_{DD} = 1.8\text{ V} \pm 0.090\text{ V}$ (for DDR2), $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.
- This parameter is sampled. $GV_{DD} = 1.5\text{ V} \pm 0.075\text{ V}$ (for DDR3), $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.175 V.

Table 14 provides the current draw characteristics for MV_{REFn} .

Table 14. Current Draw Characteristics for MV_{REFn}

Parameter / Condition		Symbol	Min	Max	Unit	Note
Current draw for MV_{REFn}	DDR2 SDRAM	$I_{MV_{REFn}}$	—	1500	μA	1
	DDR3 SDRAM			1250		

1. The voltage regulator for MV_{REFn} must be able to supply up to 1500 μA or 1250 μA current for DDR2 or DDR3, respectively.

6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 800 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this MPC8572E hardware specifications document.

6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 15, Table 16, and Table 17 provide the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 15. DDR2 SDRAM Interface Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	≥ 667 MHz	V_{ILAC}	—	$MV_{REFn} - 0.20$	V	—
	≤ 533 MHz		—	$MV_{REFn} - 0.25$		
AC input high voltage	≥ 667 MHz	V_{IHAC}	$MV_{REFn} + 0.20$	—	V	—
	—		≤ 533 MHz	$MV_{REFn} + 0.25$		

Table 16. DDR3 SDRAM Interface Input AC Timing Specifications for 1.5-V Interface

At recommended operating conditions with GV_{DD} of 1.5 V \pm 5%. DDR3 data rate is between 606 MHz and 800 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	$MV_{REFn} - 0.175$	V	—
AC input high voltage	V_{IHAC}	$MV_{REFn} + 0.175$	—	V	—

Table 17. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 5\%$ for DDR2 or $1.5\text{ V} \pm 5\%$ for DDR3.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
800 MHz	—	-200	200	—	—
667 MHz	—	-240	240	—	—
533 MHz	—	-300	300	—	—
400 MHz	—	-365	365	—	—

Note:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

Figure 3 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

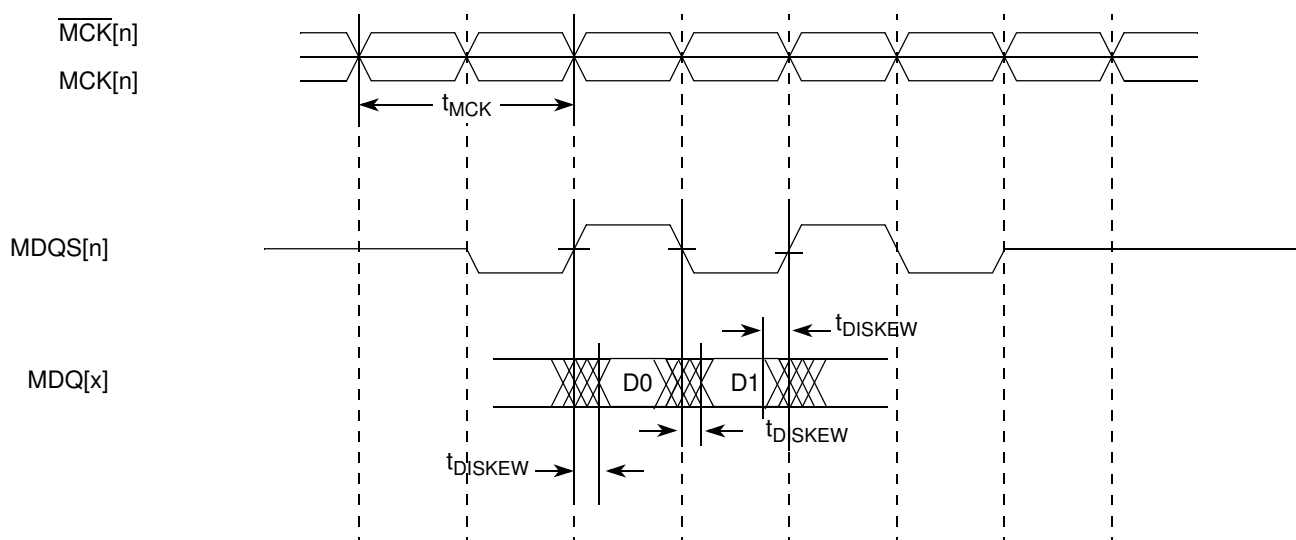


Figure 3. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

Table 18 contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 5\%$ for DDR2 or $1.5\text{ V} \pm 5\%$ for DDR3.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

 At recommended operating conditions with $G_{V_{DD}}$ of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

Parameter	Symbol ¹	Min	Max	Unit	Notes
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{MCS}[n]$ output setup with respect to MCK	t_{DDKHCS}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz	t_{DDKHCS}	1.95	—	ns	3
$\overline{MCS}[n]$ output hold with respect to MCK	t_{DDKHXC}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKMHM}			ns	4
800 MHz		-0.375	0.375		
\leq 667 MHz		-0.6	0.6		
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS} , t_{DDKLDS}			ps	5
800 MHz		375	—		
667 MHz		450	—		
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX} , t_{DDKLDX}			ps	5
800 MHz		375	—		
667 MHz		450	—		

Table 18. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

 At recommended operating conditions with $G_{V_{DD}}$ of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3.

Parameter	Symbol ¹	Min	Max	Unit	Notes
533 MHz		538	—		
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}			ns	6
800 MHz		$-0.5 \times t_{MCK} - 0.375$	$-0.5 \times t_{MCK} + 0.375$		
≤ 667 MHz		$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$		
MDQS epilogue end	t_{DDKHME}			ns	6
800 MHz		-0.375	0.375		
≤ 667 MHz	t_{DDKHME}	-0.6	0.6	ns	6

Note:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/\overline{MCK} referenced measurements are made from the crossing of the two signals ± 0.1 V.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/\overline{MCK} , \overline{MCS} , and MDQ/MECC/MDM/MDQS.
- Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the $MCK[n]$ clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the MDQS override bits (called `WR_DATA_DELAY`) in the `TIMING_CFG_2` register. This typically be set to the same delay as in `DDR_SDRAM_CLK_CNTL[CLK_ADJUST]`. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- All outputs are referenced to the rising edge of $MCK[n]$ at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 18](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 4 shows the DDR2 and DDR3 SDRAM Interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

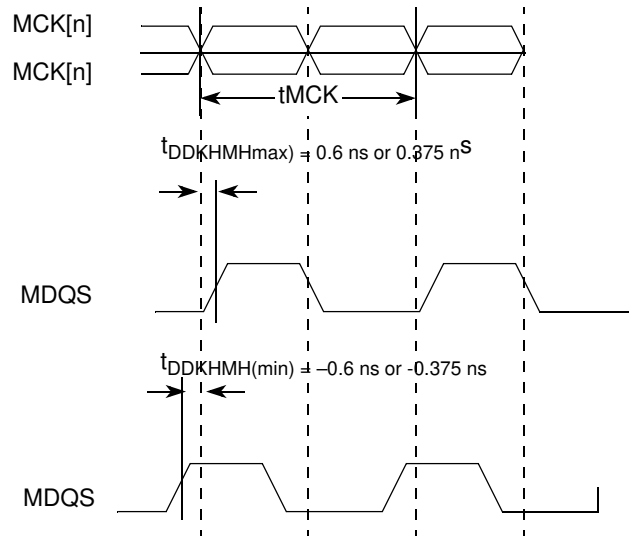


Figure 4. Timing Diagram for t_{DDKHMH}

Figure 5 shows the DDR2 and DDR3 SDRAM Interface output timing diagram.

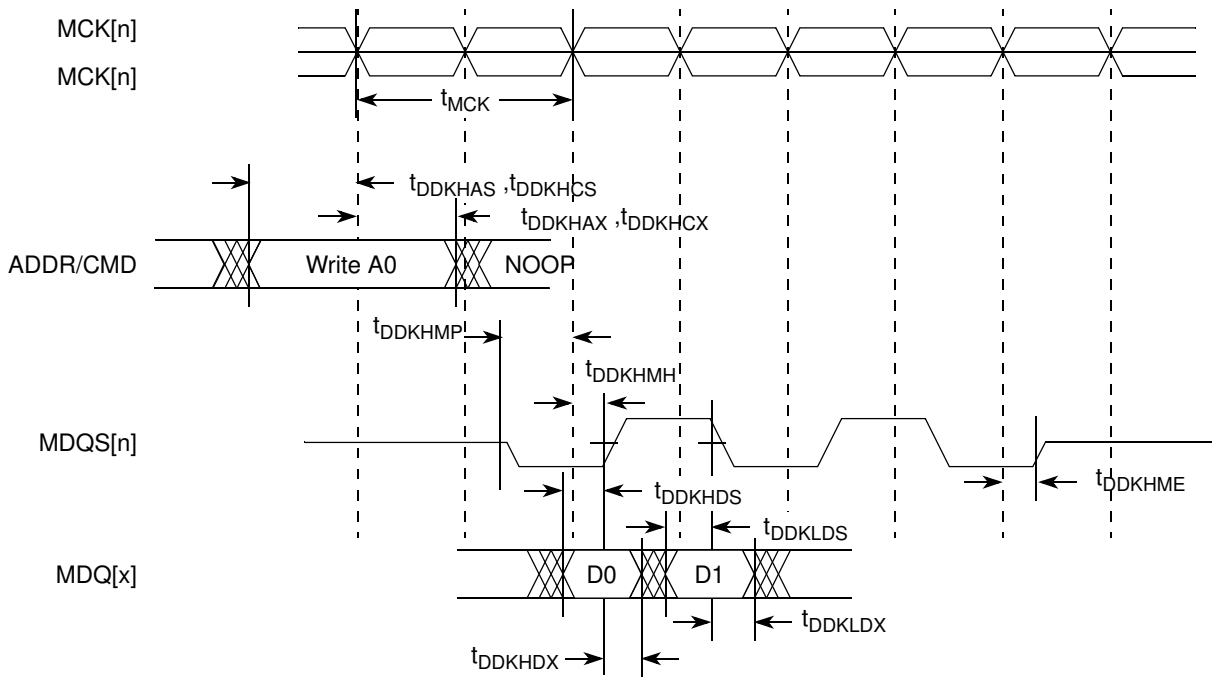


Figure 5. DDR2 and DDR3 SDRAM Interface Output Timing Diagram