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MPC866/MPC859 Hardware Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC866/859 family (refer to Table 1 for a list of devices). The MPC866P is the superset device of the MPC866/859 family.This document describes pertinent electrical and physical characteristics of the MPC8245. For functional characteristics of the processor, refer to the *MPC866 PowerQUICC Family Users Manual* (MPC866UM/D).

1 Overview

The MPC866/859 is a derivative of Freescale's MPC860 PowerQUICC™ family of devices. It is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC866/859/859DSL provides enhanced ATM functionality over that of other ATM-enabled members of the MPC860 family.

Contents

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Table 1 shows the functionality supported by the members of the MPC866/859 family.

2 Features

Table 1. MPC866 Family Functionality

Part	Cache		Ethernet		SCC	SMC
	Instruction	**Data**	**10T**	**10/100**		
MPC866P	16 Kbytes	8 Kbytes	Up to 4	1	4	2
MPC866T	4 Kbytes	4 Kbytes	Up to 4	1	4	2
MPC859P	16 Kbytes	8 Kbytes	1	1	1	2
MPC859T	4 Kbytes	4 Kbytes	1	1	1	2
MPC859DSL	4 Kbytes	4 Kbytes	1	1	1 [1]	1 [2]
MPC852T [3]	4 KBytes	4 Kbytes	2	1	2	1

[1] On the MPC859DSL, the SCC (SCC1) is for ethernet only. Also, the MPC859DSL does not support the Time Slot Assigner (TSA).

[2] On the MPC859DSL, the SMC (SMC1) is for UART only.

[3] For more details on the MPC852T, please refer to the *MPC852T Hardware Specifications.*

The following list summarizes the key MPC866/859 features:

- Embedded single-issue, 32-bit PowerPC™ core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  — The core performs branch prediction with conditional prefetch, without conditional execution
  — 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
    – 16-Kbyte instruction cache (MPC866P and MPC859P) is four-way, set-associative with 256 sets; 4-Kbyte instruction cache (MPC866T, MPC859T, and MPC859DSL) is two-way, set-associative with 128 sets.
    – 8-Kbyte data cache (MPC866P and MPC859P) is two-way, set-associative with 256 sets; 4-Kbyte data cache(MPC866T, MPC859T, and MPC859DSL) is two-way, set-associative with 128 sets.
    – Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
    – Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  — MMUs with 32-entry TLB, fully associative instruction and data TLBs
  — MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups.
  — Advanced on-chip-emulation debug mode
- The MPC866/859 provides enhanced ATM functionality over that of the MPC860SAR. The MPC866/859 adds major new features available in 'enhanced SAR' (ESAR) mode, including the following:
  — Improved operation, administration, and maintenance (OAM) support
  — OAM performance monitoring (PM) support
  — Multiple APC priority levels available to support a range of traffic pace requirements

- — ATM port-to-port switching capability without the need for RAM-based microcode
- — Simultaneous MII (10/100Base-T) and UTOPIA (half-duplex) capability
- — Optional statistical cell counters per PHY
- — UTOPIA level 2 compliant interface with added FIFO buffering to reduce the total cell transmission time. (The earlier UTOPIA level 1 specification is also supported.)
  - – Multi-PHY support on the MPC866, MPC859P, and MPC859T
  - – Four PHY support on the MPC866/859
- — Parameter RAM for both SPI and I^{2}C can be relocated without RAM-based microcode
- — Supports full-duplex UTOPIA both master (ATM side) and slave (PHY side) operation using a 'split' bus
- — AAL2/VBR functionality is ROM-resident.

- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- Thirty-two address lines
- Memory controller (eight banks)
  - — Contains complete dynamic RAM (DRAM) controller
  - — Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - — Up to 30 wait states programmable per memory bank
  - — Glueless interface to page mode/EDO/SDRAM, SRAM, EPROMs, flash EPROMs, and other memory devices.
  - — DRAM controller programmable to support most size and speed memory interfaces
  - — Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - — Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - — Variable block sizes (32 Kbytes–256 Mbytes)
  - — Selectable write protection
  - — On-chip bus arbitration logic
- General-purpose timers
  - — Four 16-bit timers cascadable to be two 32-bit timers
  - — Gate mode can enable/disable counting
  - — Interrupt can be masked on reference match and event capture
- Fast Ethernet controller (FEC)
  - — Simultaneous MII (10/100Base-T) and UTOPIA operation when using the UTOPIA multiplexed bus
- System integration unit (SIU)
  - — Bus monitor
  - — Software watchdog
  - — Periodic interrupt timer (PIT)
  - — Low-power stop mode
  - — Clock synthesizer
  - — Decrementer and time base from the PowerPC architecture
  - — Reset controller
  - — IEEE 1149.1 test access port (JTAG)

- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - The MPC866P and MPC866T have 23 internal interrupt sources; the MPC859P, MPC859T, and MPC859DSL have 20 internal interrupt sources.
  - Programmable priority between SCCs (MPC866P and MPC866T)
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8-Kbytes of dual-port RAM
  - MPC866P and MPC866T have 16 serial DMA (SDMA) channels; MPC859P, MPC859T, and MPC859DSL have 10 serial DMA (SDMA) channels.
  - Three parallel I/O registers with open-drain capability
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- MPC866P and MPC866T have four SCCs (serial communication controller); MPC859P, MPC859T, and MPC859DSL have one SCC; and SCC1 on MPC859DSL supports Ethernet only.
  - Serial ATM capability on all SCCs
  - Optional UTOPIA port on SCC4
  - Ethernet/IEEE 802.3 optional on SCC1–4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC)
- Two SMCs (serial management channels) (MPC859DSL has one SMC (SMC1) for UART.)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
 - Can be connected to the time-division multiplexed (TDM) channels

- One serial peripheral interface (SPI)
  — Supports master and slave modes
  — Supports multiple-master operation on the same bus
- One inter-integrated circuit (I^2C) port
  — Supports master and slave modes
  — Multiple-master environment support
- Time slot assigner (TSA) (MPC859DSL does not have TSA.)
  — Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  — Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  — 1- or 8-bit resolution
  — Allows independent transmit and receive routing, frame synchronization, and clocking
  — Allows dynamic changes
  — On MPC866P and MPC866T, can be internally connected to six serial channels (four SCCs and two SMCs); on MPC859P and MPC859T, can be connected to three serial channels (one SCC and two SMCs).
- Parallel interface port (PIP)
  — Centronics interface support
  — Supports fast connection between compatible ports on MPC866/859 or MC68360
- PCMCIA interface
  — Master (socket) interface, compliant with PCI Local Bus Specification (Rev 2.1)
  — Supports one or two PCMCIA sockets whether ESAR functionality is enabled
  — Eight memory or I/O windows supported
- Debug interface
  — Eight comparators: four operate on instruction address, two operate on data address, and two operate on data.
  — Supports conditions: = ≠ < >
  — Each watchpoint can generate a breakpoint internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3 V I/O operation with 5-V TTL compatibility; refer to Table 6 for a listing of the 5-V tolerant pins.
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 133 MHz

The MPC866/859 is comprised of three modules that each use a 32-bit internal bus: MPC8xx core, system integration unit (SIU), and communication processor module (CPM). The MPC866P block diagram is shown in Figure 1. The MPC859P/859T/859DSL block diagram is shown in Figure 2.
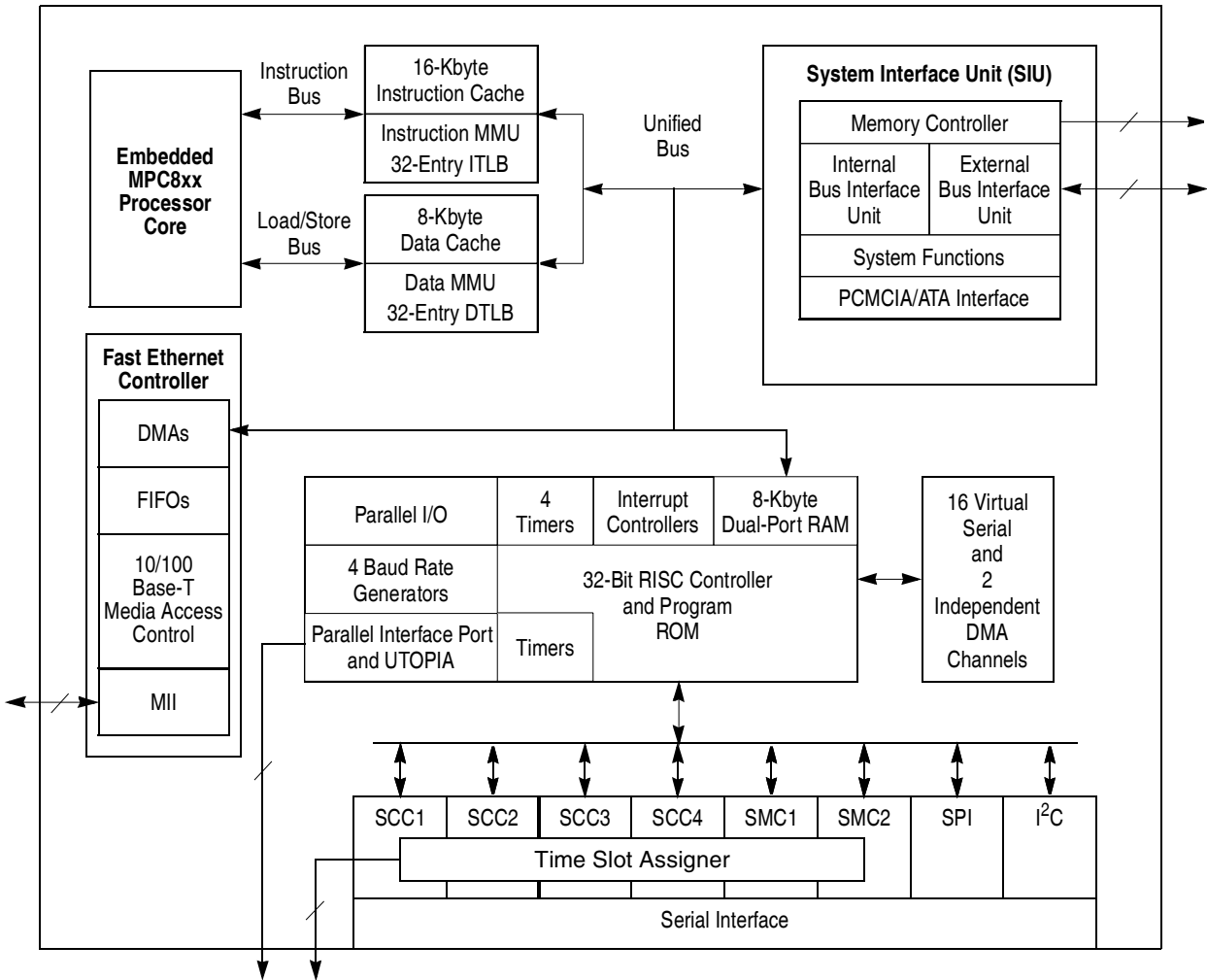
Figure 1. MPC866P Block Diagram
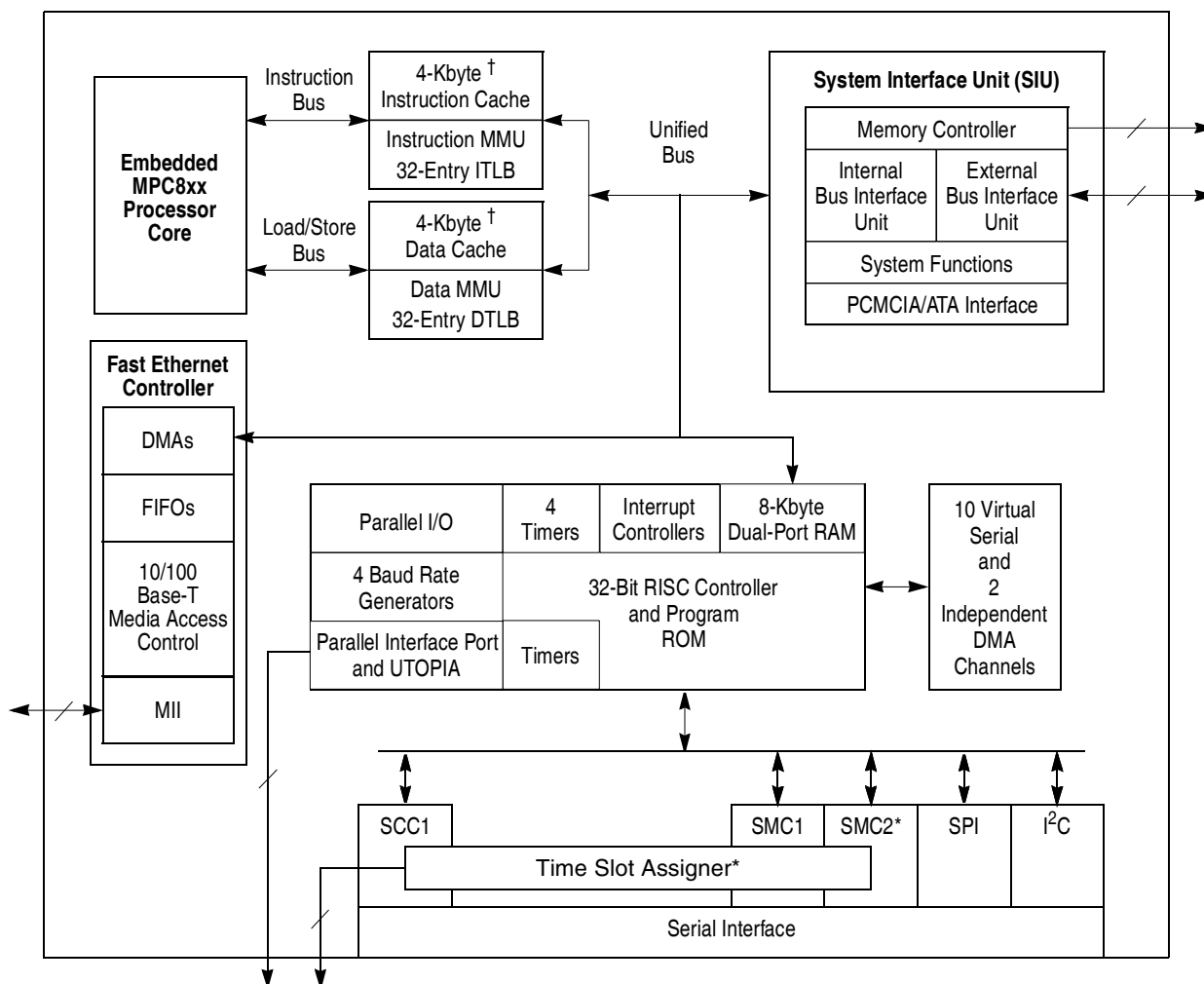
† The MPC859P has a 16-Kbyte instruction cache and a 8-Kbyte data cache.

* The MPC859DSL does not contain SMC2 nor the time slot assigner, and provides eight SDMA controllers.

Figure 2. MPC859P/859T/MPC859DSL Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC866/859. Table 2 shows the maximum tolerated ratings, and Table 3 shows the operating temperatures.

Table 2. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage [1]	VDDH	− 0.3 to 4.0	V
	VDDL	− 0.3 to 2.0	V
	VDDSYN	− 0.3 to 2.0	V
	Difference between VDDL to VDDSYN	100	mV
Input voltage [2]	V_{in}	GND − 0.3 to VDDH	V
Storage temperature range	T_{stg}	−55 to +150	°C

[1]   The power supply of the device must start its ramp from 0.0 V.

[2]   Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. See page 15.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than VDDH. This restriction applies to power-up and normal operation (that is, if the MPC866/859 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Table 3. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature [1] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	−40	°C
	$T_{j(max)}$	100	°C

[1]   Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC866/859.

Table 4. MPC866/859 Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient [1]	Natural Convection	Single-layer board (1s)	$R_{\theta JA}$ [2]	37	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	23	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$ [3]	30	
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	19	
Junction-to-board [4]			$R_{\theta JB}$	13	
Junction-to-case [5]			$R_{\theta JC}$	6	
Junction-to-package top [6]	Natural Convection		Ψ_{JT}	2	
	Airflow (200 ft/min)		Ψ_{JT}	2	

[1] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

[2] Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

[3] Per JEDEC JESD51-6 with the board horizontal.

[4] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

[6] Thermal characterization parameter indicating the temperature difference between package top and junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 5 shows power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice the bus speed.

Table 5. Power Dissipation (P$_D$)

Die Revision	Bus Mode	CPU Frequency	Typical [1]	Maximum [2]	Unit
0	1:1	50 MHz	110	140	mW
		66 MHz	150	180	mW
	2:1	66 MHz	140	160	mW
		80 MHz	170	200	mW
		100 MHz	210	250	mW
		133 MHz	260	320	mW

[1] Typical power dissipation at VDDL and VDDSYN is at 1.8 V. and VDDH is at 3.3 V.

[2] Maximum power dissipation at VDDL and VDDSYN is at 1.9 V, and VDDH is at 3.465 V.

NOTE

Values in Table 5 represent VDDL based power dissipation and do not include I/O power dissipation over VDDH. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry. The VDDSYN power dissipation is negligible.

6 DC Characteristics

Table 6 shows the DC electrical characteristics for the MPC866/859.

Table 6. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	VDDL (core)	1.7	1.9	V
	VDDH (I/O)	3.135	3.465	V
	VDDSYN [1]	1.7	1.9	V
	Difference between VDDL to VDDSYN	—	100	mV
Input high voltage (all inputs except EXTAL and EXTCLK) [2]	VIH	2.0	3.465	V

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Table 6. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input low voltage	VIL	GND	0.8	V
EXTAL, EXTCLK input high voltage	VIHC	0.7*(VDDH)	VDDH	V
Input leakage current, Vin = 5.5V (except TMS, $\overline{TRST}$, DSCK and DSDI pins) for 5 Volts Tolerant Pins [2]	I_{in}	—	100	µA
Input leakage current, Vin = VDDH (except TMS, $\overline{TRST}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input leakage current, Vin = 0 V (except TMS, $\overline{TRST}$, DSCK and DSDI pins)	I_{In}	—	10	µA
Input capacitance [3]	C_{in}	—	20	pF
Output high voltage, IOH = – 2.0 mA, except XTAL, and Open drain pins	VOH	2.4	—	V
Output low voltage • IOL = 2.0 mA (CLKOUT) • IOL = 3.2 mA [4] • IOL = 5.3 mA [5] • IOL = 7.0 mA (TXD1/PA14, TXD2/PA12) • IOL = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	VOL	—	0.5	V

[1] The difference between VDDL and VDDSYN can not be more than 100 m V.

[2] The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, $\overline{TRST}$_B, TMS, MII_TXEN, MII_MDIO are 5 V tolerant.

[3] Input capacitance is periodically sampled.

[4] A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), DP(0:3)/$\overline{IRQ}$(3:6), RD/$\overline{WR}$, $\overline{BURST}$, $\overline{RSV}$/$\overline{IRQ2}$, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1 /PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/$\overline{TOUT1}$/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, $\overline{TOUT2}$/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/$\overline{TOUT3}$/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/$\overline{TOUT4}$/CLK8/PA0, $\overline{REJCT1}$/$\overline{SPISEL}$/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, $\overline{SMSYN1}$/$\overline{SDACK1}$/PB23, $\overline{SMSYN2}$/$\overline{SDACK2}$/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/$\overline{RTS1}$/PB19, L1ST2/$\overline{RTS2}$/PB18, L1ST3/$\overline{L1RQB}$/PB17, L1ST4/$\overline{L1RQA}$/PB16, BRGO3/PB15, $\overline{RSTRT1}$/PB14, L1ST1/$\overline{RTS1}$/$\overline{DREQ0}$/PC15, L1ST2/$\overline{RTS2}$/$\overline{DREQ1}$/PC14, L1ST3/$\overline{L1RQB}$/PC13, L1ST4/$\overline{L1RQA}$/PC12, $\overline{CTS1}$/PC11, $\overline{TGATE1}$/$\overline{CD1}$/PC10, $\overline{CTS2}$/PC9, $\overline{TGATE2}$/$\overline{CD2}$/PC8, $\overline{CTS3}$/$\overline{SDACK2}$/L1TSYNCB/PC7, $\overline{CD3}$/L1RSYNCB/PC6, $\overline{CTS4}$/$\overline{SDACK1}$/L1TSYNCA/PC5, $\overline{CD4}$/L1RSYNCA/PC4, PD15/L1TSYNCA, PD14/L1RSYNCA, PD13/L1TSYNCB, PD12/L1RSYNCB, PD11/RXD3, PD10/TXD3, PD9/RXD4, PD8/TXD4, PD5/REJECT2, PD6/$\overline{RTS4}$, PD7/$\overline{RTS3}$, PD4/REJECT3, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, MII_TXD[0:3].

[5] $\overline{BDIP}$/$\overline{GPL\_B}$(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:5), $\overline{CS}$(6)/$\overline{CE}$(1)_B, $\overline{CS}$(7)/$\overline{CE}$(2)_B, $\overline{WE0}$/$\overline{BS\_B0}$/$\overline{IORD}$, $\overline{WE1}$/$\overline{BS\_B1}$/$\overline{IOWR}$, $\overline{WE2}$/$\overline{BS\_B2}$/$\overline{PCOE}$, $\overline{WE3}$/$\overline{BS\_B3}$/$\overline{PCWE}$, BS_A(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/$\overline{GPL\_A1}$/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, UPWAITB/$\overline{GPL\_B4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE1\_A}$, $\overline{CE2\_A}$, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/$\overline{STS}$, OP3/MODCK2/DSDO, BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, P_D = (VDDL x IDDL) + PI/O, where PI/O is the power dissipation of the I/O drivers. The VDDSYN power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity T_J-T_A) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 3.
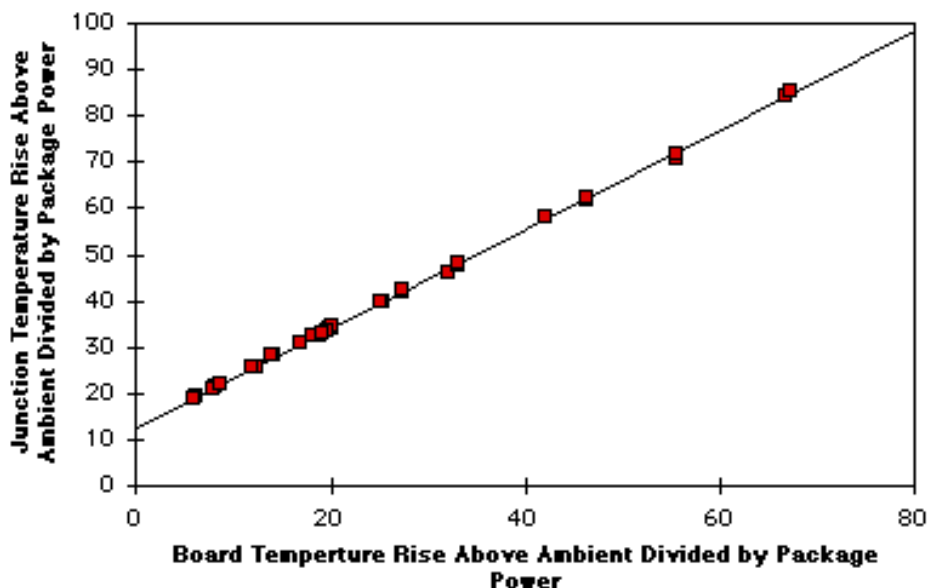
Figure 3. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$T_J = T_B + (R_{\theta JB} \times P_D)$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

T_B = board temperature °C

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC866/859 power supply. The MPC866/859 has a core voltage (VDDL) and PLL voltage (VDDSYN) that operates at a lower voltage than the I/O voltage VDDH. The I/O section of the MPC866/859 is supplied with 3.3 V across VDDH and V_{SS} (GND).

Signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and MII_MDIO are 5-V tolerant. All inputs cannot be more than 2.5 V greater than VDDH. In addition, 5-V tolerant pins cannot exceed 5.5 V and the remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- VDDL must not exceed VDDH during power up and power down.
- VDDL must not exceed 1.9 V and VDDH must not exceed 3.465 V.

These cautions are necessary for the long term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 4 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on powerup and the 1N5820 diodes regulate the maximum potential difference on powerdown.
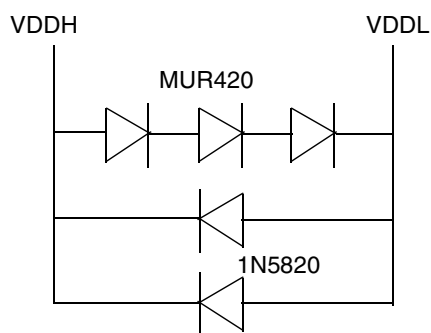
Figure 4. Example Voltage Sequencing Circuit

9 Layout Practices

Each V_{DD} pin on the MPC866/859 should be provided with a low-impedance path to the board's supply. Furthermore, each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 μF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than 1/2" per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC866/859 have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times.

This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6" are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to Section 14.4.3, Clock Synthesizer Power (VDDSYN, VSSSYN, VSSSYN1), in the *MPC866 User's Manual*.

10 Bus Signal Timing

The maximum bus speed supported by the MPC866/859 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC866/859 used at 100 MHz must be configured for a 50-MHz bus). Table 7 and Table 8 show the frequency ranges for standard part frequencies.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Freq	50 MHz		66 MHz	
	Min	Max	Min	Max
Core	40	50	40	66.67
Bus	40	50	40	66.67

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Freq	50 MHz		66 MHz		100 MHz		133 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core	40	50	40	66.67	40	100	40	133.34
Bus	20	25	20	33.33	20	50	20	66.67

Table 9 shows the timings for the MPC866/859 at 33, 40, 50, and 66 MHz bus operation. The timing for the MPC866/859 bus shown in this table assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay.

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus Period (CLKOUT) See Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew	− 2	+2	− 2	+2	− 2	+2	− 2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK	—	0.50	—	0.50	—	0.50	—	0.50	%

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 x B1, MAX = 0.6 x B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B3	CLKOUT pulse width high (MIN = 0.4 x B1, MAX = 0.6 x B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 x B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR output hold (MIN = 0.25 x B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2), IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 x B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), valid (MAX = 0.25 x B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR valid (MAX = 0.25 x B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [4] (MAX = 0.25 x B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), PTR High-Z (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 x B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	9.80	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 [1])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 x B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns

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Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 x B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{TEA}$ High-Z (MIN = 0.00 x B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time) [2] (4 MIN = 0.00 x B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time) (MIN = 0.00 x B1 + 1.00 [3])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [4] (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [4] (MIN = 0.00 x B1 + 1.00 [5])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [6] (MIN = 0.00 x B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [6] (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 x B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns

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Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 x B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 x B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0,1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns

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Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1– 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 (MIN = 0.50 x B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29d	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 (MIN = 1.50 x B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29f	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 – 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 – 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29h	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access [7] (MIN = 0.25 x B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 x B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B30b	$\overline{WE}$(0:3) negated to A(0:31) invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 x B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 x B1 – 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 X B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns

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Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 x B1 + 6.6)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 x B1 + 6.60)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 x B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 x B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns

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Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 − 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 − 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 x B1 − 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 x B1 − 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B37	UPWAIT valid to CLKOUT falling edge [8] (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[8] (MIN = 0.00 x B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [9] (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

[1] For part speeds above 50 MHz, use 9.80 ns for B11a.

[2] The timing required for $\overline{BR}$ input is relevant when the MPC866/859 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC866/859 is selected to work with the external bus arbiter.

[3] For part speeds above 50 MHz, use 2 ns for B17.

[4] The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of CLKOUT, in which the $\overline{TA}$ input signal is asserted.

[5] For part speeds above 50 MHz, use 2 ns for B19.

[6] The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats, where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)
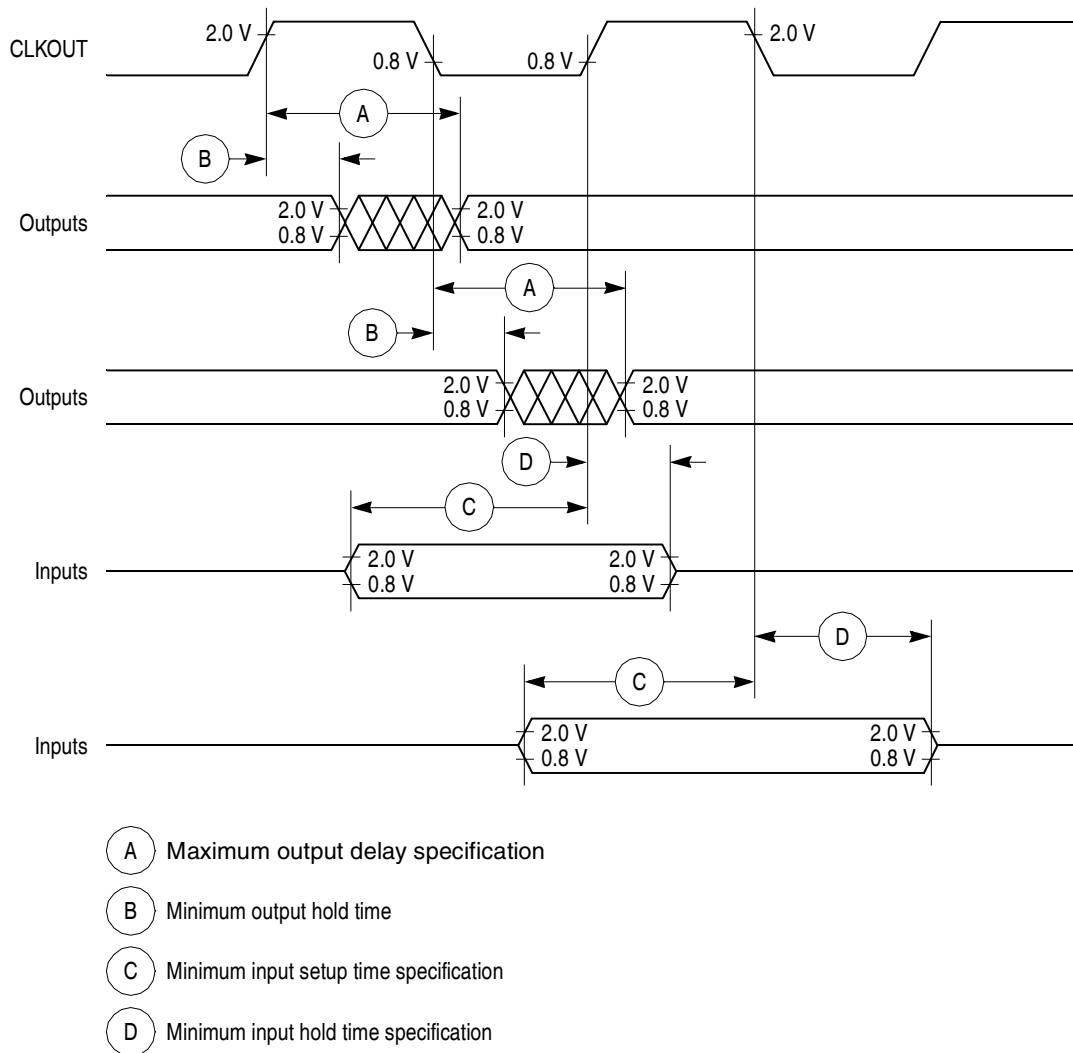
[7] The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

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8 The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 20.

9 The $\overline{AS}$ signal is considered asynchronous to CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 23.

Figure 5 shows the control timing diagram.

A	Maximum output delay specification
B	Minimum output hold time
C	Minimum input setup time specification
D	Minimum input hold time specification

Figure 5. Control Timing

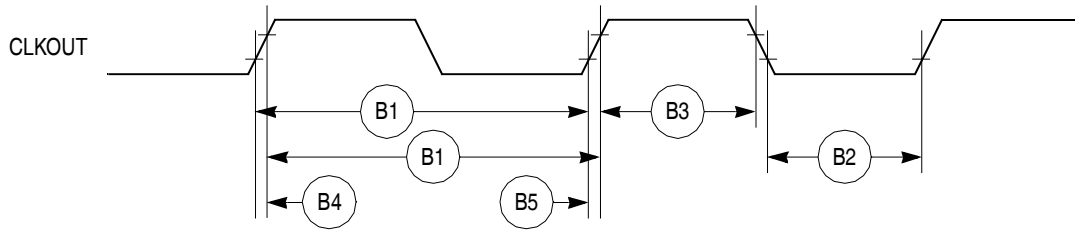Figure 6 shows the timing for the external clock.

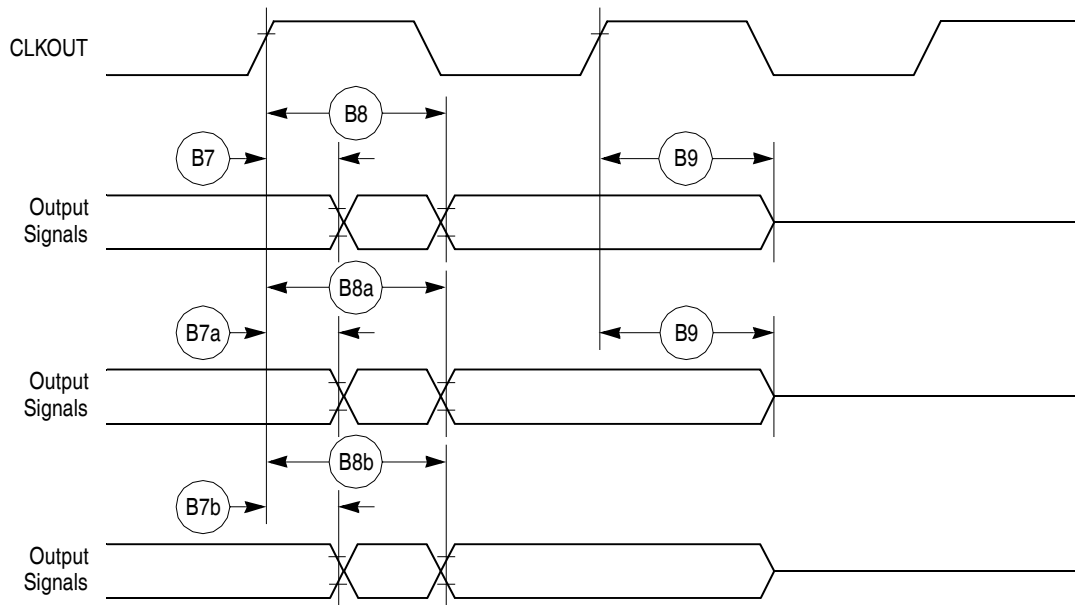**Figure 6. External Clock Timing**

Figure 7 shows the timing for the synchronous output signals.

Figure 7. Synchronous Output Signals Timing