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**Freescale Semiconductor**
**Technical Data**

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# MPC862/857T/857DSL PowerQUICC™ Family Hardware Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC862/857T/857DSL family (refer to Table 1 for a list of devices). The MPC862P, which contains a PowerPC™ core processor, is the superset device of the MPC862/857T/857DSL family. For functional characteristics of the processor, refer to the *MPC862 PowerQUICC™ Family Users Manual* (MPC862UM/D).

**Contents**





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# 1 Overview

The MPC862/857T/857DSL is a derivative of Freescale's MPC860 PowerQUICC™ family of devices. It is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC862/857T/857DSL provides enhanced ATM functionality over that of other ATM-enabled members of the MPC860 family.

Table 1 shows the functionality supported by the members of the MPC862/857T/857DSL family.

**Table 1. MPC862 Family Functionality**

| Part | Cache | | Ethernet | | SCC | SMC |
|---|---|---|---|---|---|---|
| | Instruction Cache | Data Cache | 10T | 10/100 | | |
| MPC862P | 16 Kbyte | 8 Kbyte | Up to 4 | 1 | 4 | 2 |
| MPC862T | 4 Kbyte | 4 Kbyte | Up to 4 | 1 | 4 | 2 |
| MPC857T | 4 Kbyte | 4 Kbyte | 1 | 1 | 1 | 2 |
| MPC857DSL | 4 Kbyte | 4 Kbyte | 1 | 1 | 1 [1] | 1 [2] |

[1] On the MPC857DSL, the SCC (SCC1) is for ethernet only. Also, the MPC857DSL does not support the Time Slot Assigner (TSA).

[2] On the MPC857DSL, the SMC (SMC1) is for UART only.

# 2 Features

The following list summarizes the key MPC862/857T/857DSL features:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1).
    - 16-Kbyte instruction cache (MPC862P) is four-way, set-associative with 256 sets; 4-Kbyte instruction cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
    - 8-Kbyte data cache (MPC862P) is two-way, set-associative with 256 sets; 4-Kbyte data cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode

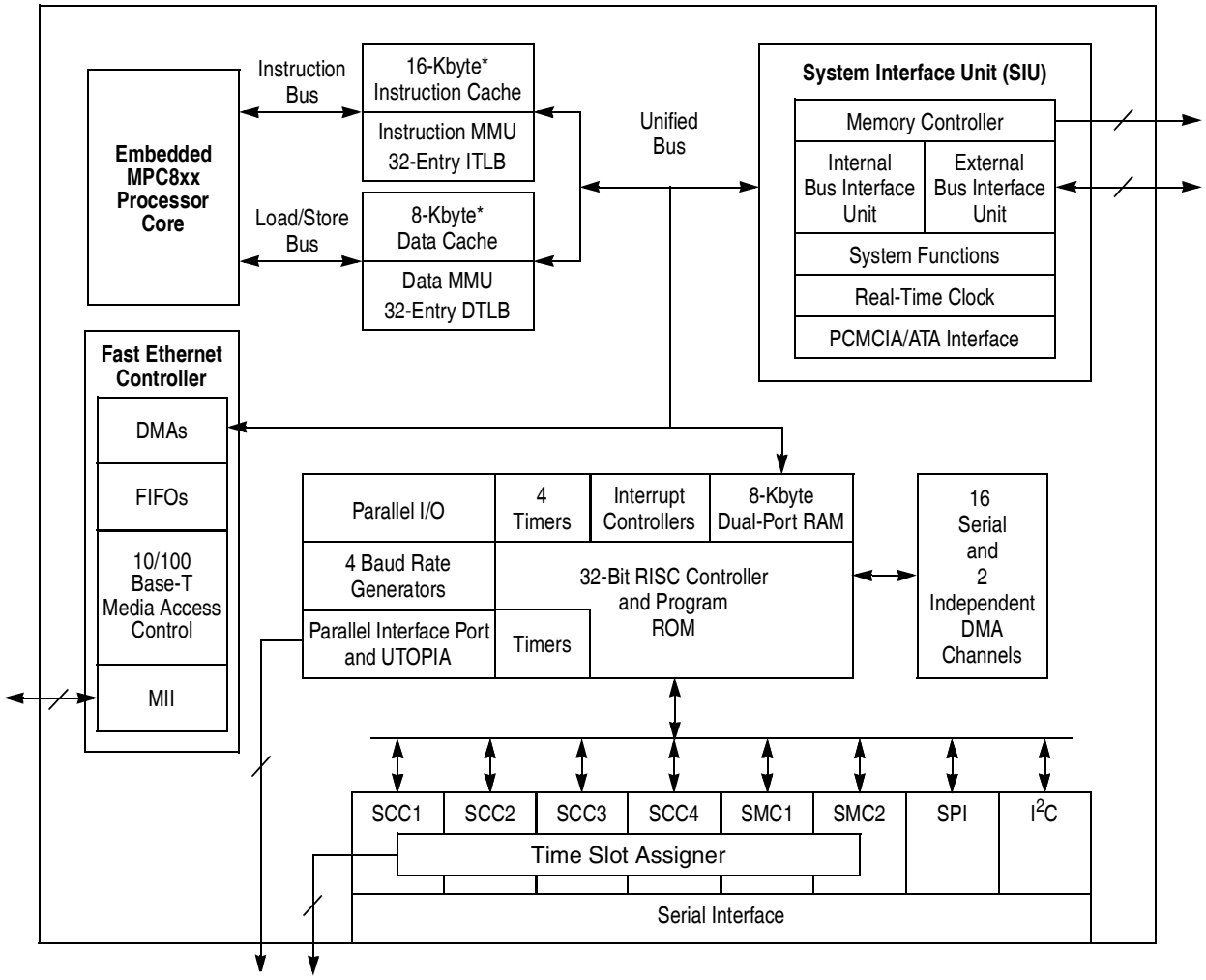
- The MPC862/857T/857DSL provides enhanced ATM functionality over that of the MPC860SAR. The MPC862/857T/857DSL adds major new features available in “enhanced SAR” (ESAR) mode, including the following:
  - Improved operation, administration and maintenance (OAM) support
  - OAM performance monitoring (PM) support
  - Multiple APC priority levels available to support a range of traffic pace requirements
  - ATM port-to-port switching capability without the need for RAM-based microcode
  - Simultaneous MII (10/100Base-T) and UTOPIA (half-duplex) capability
  - Optional statistical cell counters per PHY
  - UTOPIA level 2 compliant interface with added FIFO buffering to reduce the total cell transmission time. (The earlier UTOPIA level 1 specification is also supported.)
  - Multi-PHY support on the MPC857T
  - Four PHY support on the MPC857DSL
  - Parameter RAM for both SPI and $I^2C$ can be relocated without RAM-based microcode
  - Supports full-duplex UTOPIA both master (ATM side) and slave (PHY side) operation using a “split” bus
  - AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to Page mode/EDO/SDRAM, SRAM, EPROMs, flash EPROMs, and other memory devices.
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbyte–256 Mbyte)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers cascadable to be two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Fast Ethernet controller (FEC)
  - Simultaneous MII (10/100Base-T) and UTOPIA operation when using the UTOPIA multiplexed bus.

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - The MPC862P and MPC862T have 23 internal interrupt sources; the MPC857T and MPC857DSL have 20 internal interrupt sources
  - Programmable priority between SCCs (MPC862P and MPC862T)
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8-Kbytes of dual-port RAM
  - The MPC862P and MPC862T have 16 serial DMA (SDMA) channels; the MPC857T and MPC857DSL have 10 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- The MPC862P and MPC862T have four SCCs (serial communication controller) The MPC857T and MPC857DSL have one SCC, SCC1; the MPC857DSL supports ethernet only
  - Serial ATM capability on all SCCs
  - Optional UTOPIA port on SCC4
  - Ethernet/IEEE 802.3 optional on SCC1–4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk

  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels) (The MPC857DSL has one SMC, SMC1 for UART)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- One inter-integrated circuit ($I^2C$) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time-slot assigner (TSA) (The MPC857DSL does not have the TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, clocking
  - Allows dynamic changes
  - On the MPC862P and MPC862T, can be internally connected to six serial channels (four SCCs and two SMCs); on the MPC857T, can be connected to three serial channels (one SCC and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC862/857T/857DSL or MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one or two PCMCIA sockets dependent upon whether ESAR functionality is enabled
  - 8 memory or I/O windows supported
- Low power support
  - Full on—All units fully powered
  - Doze—Core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby

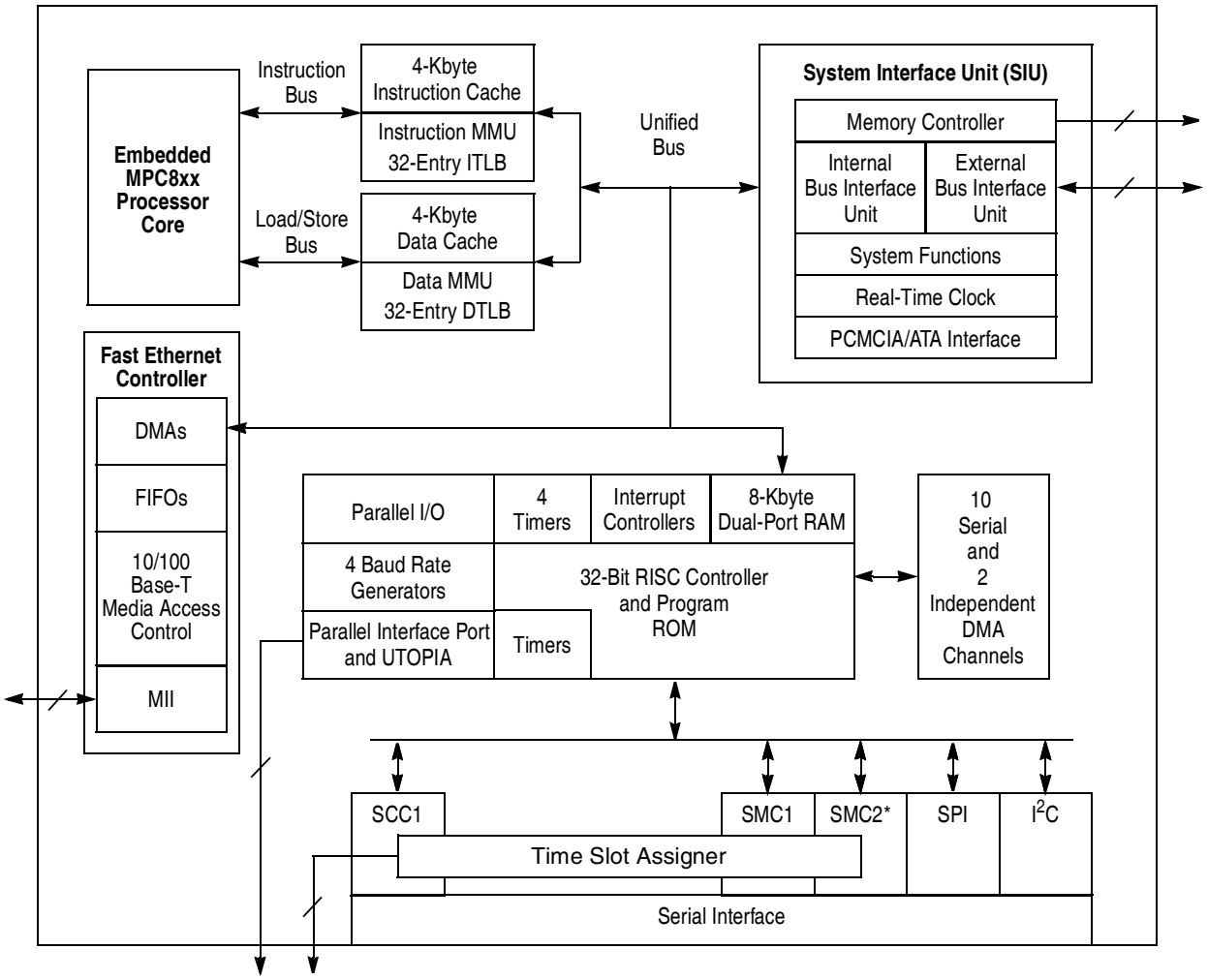
  - Sleep—All units disabled except RTC, PIT, time base, and decrementer with PLL active for fast wake up
  - Deep sleep—All units disabled including PLL except RTC, PIT, time base, and decrementer.
  - Power down mode— All units powered down except PLL, RTC, PIT, time base and decrementer
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- 3.3 V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 100MHz

The MPC862/857T/857DSL is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). The MPC862P/862T block diagram is shown in Figure 1. The MPC857T/857DSL block diagram is shown in Figure 2.




*The MPC862T contains 4-Kbyte instruction cache and 4-Kbyte data cache.

**Figure 1. MPC862P/862T Block Diagram**




*The MPC857DSL does not contain SMC2 nor the Time Slot Assigner, and provides eight SDMA controllers.

**Figure 2. MPC857T/MPC857DSL Block Diagram**

# 3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC862/857T/857DSL. Table 2 provides the maximum ratings.

**Table 2. Maximum Tolerated Ratings**

(GND = 0 V)

| Rating | Symbol | Value | Unit | Max Freq (MHz) |
|---|---|---|---|---|
| Supply voltage [1] | VDDH | -0.3 to 4.0 | V | - |
| | VDDL | -0.3 to 4.0 | V | - |
| | KAPWR | -0.3 to 4.0 | V | - |
| | VDDSYN | -0.3 to 4.0 | V | - |

**Table 2. Maximum Tolerated Ratings (continued)**

(GND = 0 V)

| Rating | Symbol | Value | Unit | Max Freq (MHz) |
|---|---|---|---|---|
| Input voltage [2] | $V_{in}$ | GND-0.3 to VDDH | V | - |
| Temperature [3] (standard) [4] | $T_{A(min)}$ | 0 | °C | 100 |
| | $T_{j(max)}$ | 105 | °C | 100 |
| Temperature [3] (extended) | $T_{A(min)}$ | -40 | °C | 80 |
| | $T_{j(max)}$ | 115 | °C | 80 |
| Storage temperature range | $T_{stg}$ | -55 to +150 | °C | - |

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
**Caution**: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC862/857T/857DSL is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

3 Minimum temperatures are guaranteed as ambient temperature, $T_A$. Maximum temperatures are guaranteed as junction temperature, $T_j$.

4 JTAG is tested only at ambient, not at standard maximum or extended maximum.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{CC}$).

# 4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC862/857T/857DSL.

**Table 3. MPC862/857T/857DSL Thermal Resistance Data**

| Rating | Environment | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Junction to ambient [1] | Natural Convection | Single layer board (1s) | $R_{\theta JA}$ [2] | 37 | °C/W |
| | | Four layer board (2s2p) | $R_{\theta JMA}$ [3] | 23 | |
| | Air flow (200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ [3] | 30 | |
| | | Four layer board (2s2p) | $R_{\theta JMA}$ [3] | 19 | |
| Junction to board [4] | | | $R_{\theta JB}$ | 13 | |
| Junction to case [5] | | | $R_{\theta JC}$ | 6 | |
| Junction to package top [6] | Natural Convection | | $\Psi_{JT}$ | 2 | |
| | Air flow (200 ft/min) | | $\Psi_{JT}$ | 2 | |

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

# 5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

**Table 4. Power Dissipation ($P_D$)**

| Die Revision | Frequency | Typical [1] | Maximum [2] | Unit |
|---|---|---|---|---|
| 0<br>(1:1 Mode) | 50 MHz | 656 | 735 | mW |
| | 66 MHz | TBD | TBD | mW |
| A.1, B.0<br>(1:1 Mode) | 50 MHz | 630 | 760 | mW |
| | 66 MHz | 890 | 1000 | mW |

**Table 4. Power Dissipation ($P_D$) (continued)**

| Die Revision | Frequency | Typical [1] | Maximum [2] | Unit |
|---|---|---|---|---|
| A.1, B.0 (2:1 Mode) | 66 MHz | 910 | 1060 | mW |
| | 80 MHz | 1.06 | 1.20 | W |
| B.0 (2:1 Mode) | 100 MHz | 1.35 | 1.54 | W |

1 Typical power dissipation is measured at 3.3 V.

2 Maximum power dissipation is measured at 3.5 V.

**NOTE**

Values in Table 4 represent VDDL based power dissipation and do not include I/O power dissipation over VDDH. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

# 6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC862/857T/857DSL.

**Table 5. DC Electrical Specifications**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating voltage | VDDH, VDDL, KAPWR, VDDSYN | 3.135 | 3.465 | V |
| | KAPWR (power-down mode) | 2.0 | 3.6 | V |
| | KAPWR (all other operating modes) | VDDH – 0.4 | VDDH | V |
| Input High Voltage (all inputs except EXTAL and EXTCLK) | VIH | 2.0 | 5.5 | V |
| Input Low Voltage [1] | VIL | GND | 0.8 | V |
| EXTAL, EXTCLK Input High Voltage | VIHC | 0.7*(VCC) | VCC+0.3 | V |
| Input Leakage Current, Vin = 5.5 V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins) | $I_{in}$ | — | 100 | µA |
| Input Leakage Current, Vin = 3.6 V (Except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI) | $I_{In}$ | — | 10 | µA |
| Input Leakage Current, Vin = 0 V (Except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input Capacitance [2] | $C_{in}$ | — | 20 | pF |
| Output High Voltage, IOH = -2.0 mA, VDDH = 3.0 V (Except XTAL, XFC, and Open drain pins) | VOH | 2.4 | — | V |

**Table 5. DC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Output Low Voltage<br>IOL = 2.0 mA (CLKOUT)<br>IOL = 3.2 mA [3]<br>IOL = 5.3 mA [4]<br>IOL = 7.0 mA (TXD1/PA14, TXD2/PA12)<br>IOL = 8.9 mA (TS, TA, TEA, BI, BB, HRESET, SRESET) | VOL | — | 0.5 | V |

1 $V_{IL}$(max) for the $I^2C$ interface is 0.8 V rather than the 1.5 V as specified in the $I^2C$ standard.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1 /PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, REJCT1/SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, CTS3/SDACK2/L1TSYNCB/PC7, CD3/L1RSYNCB/PC6, CTS4/SDACK1/L1TSYNCA/PC5, CD4/L1RSYNCA/PC4, PD15/L1TSYNCA, PD14/L1RSYNCA, PD13/L1TSYNCB, PD12/L1RSYNCB, PD11/RXD3, PD10/TXD3, PD9/RXD4, PD8/TXD4, PD5/REJECT2, PD6/RTS4, PD7/RTS3, PD4/REJECT3, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, MII_TXD[0:3].

4 BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, BADDR(28:30).

# 7 Thermal Calculation and Measurement

For the following discussions, $P_D$= (VDD x IDD) + PI/O, where PI/O is the power dissipation of the I/O drivers.

## 7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$ = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

$P_D$ = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J$-$T_A$) are possible.

## 7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 3.

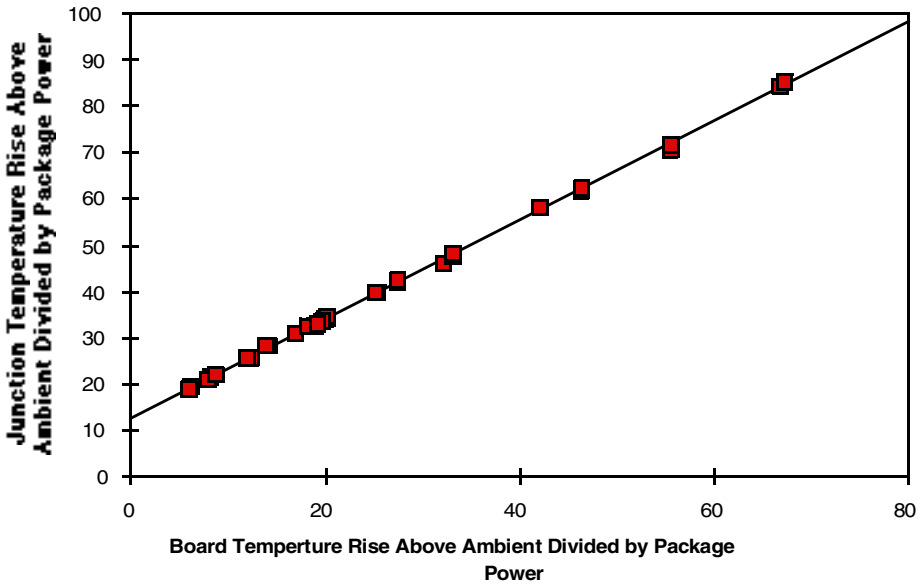



**Figure 3. Effect of Board Temperature Rise on Thermal Behavior**

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

$T_B$ = board temperature (ºC)

$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

## 7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

## 7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$ = thermal characterization parameter

$T_T$ = thermocouple temperature on top of package

$P_D$ = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 7.6 References

| | |
|---|---|
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| MIL-SPEC and EIA/JESD (JEDEC) Specifications<br>(Available from Global Engineering Documents) | 800-854-7179 or<br>303-397-7956 |
| JEDEC Specifications | http://www.jedec.org |

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

# 8 Layout Practices

Each $V_{CC}$ pin on the MPC862/857T/857DSL should be provided with a low-impedance path to the board’s supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{CC}$ power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip $V_{CC}$ and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as $V_{CC}$ and GND planes.

All output pins on the MPC862/857T/857DSL have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{CC}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

# 9 Bus Signal Timing

The maximum bus speed supported by the MPC862/857T/857DSL is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC862/857T/857DSL used at 80MHz must be configured for a 40 MHz bus). Table 6 shows the period ranges for standard part frequencies.

**Table 6. Period Range for Standard Part Frequencies**

| Freq | 50 MHz | | 66 MHz | | 80 MHz | | 100 MHz | |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max |
| Period | 20.00 | 30.30 | 15.15 | 30.30 | 25.00 | 30.30 | 20.00 | 30.30 |

Table 7 provides the bus operation timing for the MPC862/857T/857DSL at 33 MHz, 40 Mhz, 50 MHz and 66 Mhz.

The timing for the MPC862/857T/857DSL bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

**Table 7. Bus Operation Timings**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B1 | CLKOUT period | 30.30 | 30.30 | 25.00 | 30.30 | 20.00 | 30.30 | 15.15 | 30.30 | ns |
| B1a | EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2) | -0.90 | 0.90 | -0.90 | 0.90 | -0.90 | 0.90 | -0.90 | 0.90 | ns |
| B1b | EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10) | -2.30 | 2.30 | -2.30 | 2.30 | -2.30 | 2.30 | -2.30 | 2.30 | ns |
| B1c | CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) [1] | -0.60 | 0.60 | -0.60 | 0.60 | -0.60 | 0.60 | -0.60 | 0.60 | ns |
| B1d | CLKOUT phase jitter[1] | -2.00 | 2.00 | -2.00 | 2.00 | -2.00 | 2.00 | -2.00 | 2.00 | ns |
| B1e | CLKOUT frequency jitter (MF < 10) [1] | — | 0.50 | — | 0.50 | — | 0.50 | — | 0.50 | % |
| B1f | CLKOUT frequency jitter (10 < MF < 500) [1] | — | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | % |
| B1g | CLKOUT frequency jitter (MF > 500) [1] | — | 3.00 | — | 3.00 | — | 3.00 | — | 3.00 | % |
| B1h | Frequency jitter on EXTCLK [2] | — | 0.50 | — | 0.50 | — | 0.50 | — | 0.50 | % |
| B2 | CLKOUT pulse width low (MIN = 0.040 x B1) | 12.10 | — | 10.00 | — | 8.00 | — | 6.10 | — | ns |
| B3 | CLKOUT width high (MIN = 0.040 x B1) | 12.10 | — | 10.00 | — | 8.00 | — | 6.10 | — | ns |
| B4 | CLKOUT rise time [3] (MAX = 0.00 x B1 + 4.00) | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B5[33] | CLKOUT fall time[3] (MAX = 0.00 x B1 + 4.00) | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B7 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) invalid (MIN = 0.25 x B1) | 7.60 | — | 6.30 | — | 5.00 | — | 3.80 | — | ns |
| B7a | CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR invalid (MIN = 0.25 x B1) | 7.60 | — | 6.30 | — | 5.00 | — | 3.80 | — | ns |
| B7b | CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ invalid [4] (MIN = 0.25 x B1) | 7.60 | — | 6.30 | — | 5.00 | — | 3.80 | — | ns |
| B8 | CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B8a | CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B8b | CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS Valid [4] (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B9 | CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B11 | CLKOUT to TS, BB assertion (MAX = 0.25 x B1 + 6.0) | 7.60 | 13.60 | 6.30 | 12.30 | 5.00 | 11.00 | 3.80 | 11.30 | ns |
| B11a | CLKOUT to TA, BI assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 [5]) | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.80 | ns |
| B12 | CLKOUT to TS, BB negation (MAX = 0.25 x B1 + 4.8) | 7.60 | 12.30 | 6.30 | 11.00 | 5.00 | 9.80 | 3.80 | 8.50 | ns |
| B12a | CLKOUT to TA, BI negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | ns |
| B13 | CLKOUT to TS, BB High-Z (MIN = 0.25 x B1) | 7.60 | 21.60 | 6.30 | 20.30 | 5.00 | 19.00 | 3.80 | 14.00 | ns |
| B13a | CLKOUT to TA, BI High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | ns |
| B14 | CLKOUT to TEA assertion (MAX = 0.00 x B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | ns |
| B15 | CLKOUT to TEA High-Z (MIN = 0.00 x B1 + 2.50) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | ns |
| B16 | TA, BI valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B16a | TEA, KR, RETRY, CR valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5) | 4.50 | — | 4.50 | — | 4.50 | — | 4.50 | — | ns |
| B16b | BB, BG, BR, valid to CLKOUT (setup time) [6] (4MIN = 0.00 x B1 + 0.00) | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | — | ns |
| B17 | CLKOUT to TA, TEA, BI, BB, BG, BR valid (hold time) (MIN = 0.00 x B1 + 1.00 [7]) | 1.00 | — | 1.00 | — | 1.00 | — | 2.00 | — | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B17a | CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 x B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B18 | D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [8] (MIN = 0.00 x B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B19 | CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [8] (MIN = 0.00 x B1 + 1.00 [9]) | 1.00 | — | 1.00 | — | 1.00 | — | 2.00 | — | ns |
| B20 | D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [10](MIN = 0.00 x B1 + 4.00) | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | — | ns |
| B21 | CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [10] (MIN = 0.00 x B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B22 | CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B22a | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 x B1 + 8.00) | — | 8.00 | — | 8.00 | — | 8.00 | — | 8.00 | ns |
| B22b | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B22c | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 x B1 + 6.6) | 10.90 | 18.00 | 10.90 | 18.00 | 7.00 | 14.30 | 5.20 | 12.30 | ns |
| B23 | CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 x B1 + 8.00) | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | ns |
| B24 | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B24a | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 x B1 - 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B25 | CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted (MAX = 0.00 x B1 + 9.00) | — | 9.00 | | 9.00 | | 9.00 | | 9.00 | ns |
| B26 | CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 x B1 + 9.00) | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B27 | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00) | 35.90 | — | 29.30 | — | 23.00 | — | 16.90 | — | ns |
| B27a | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00) | 43.50 | — | 35.50 | — | 28.00 | — | 20.70 | — | ns |
| B28 | CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00) | — | 9.00 | — | 9.00 | — | 9.00 | — | 9.00 | ns |
| B28a | CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B28b | CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80) | — | 14.30 | — | 13.00 | — | 11.80 | — | 10.50 | ns |
| B28c | CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6) | 10.90 | 18.00 | 10.90 | 18.00 | 7.00 | 14.30 | 5.20 | 12.30 | ns |
| B28d | CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6) | — | 18.00 | — | 18.00 | — | 14.30 | — | 12.30 | ns |
| B29 | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B29a | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 - 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B29b | $\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B29c | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 x B1 - 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B29d | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 - 2.00) | 43.50 | — | 35.50 | — | 28.00 | — | 20.70 | — | ns |
| B29e | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00) | 43.50 | — | 35.50 | — | 28.00 | — | 20.70 | — | ns |
| B29f | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 6.30) | 5.00 | — | 3.00 | — | 1.10 | — | 0.00 | — | ns |
| B29g | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 6.30) | 5.00 | — | 3.00 | — | 1.10 | — | 0.00 | — | ns |
| B29h | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 3.30) | 38.40 | — | 31.10 | — | 24.20 | — | 17.50 | — | ns |
| B29i | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 3.30) | 38.40 | — | 31.10 | — | 24.20 | — | 17.50 | — | ns |
| B30 | $\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM write access [11] (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B30a | $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 x B1 - 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B30b | $\overline{WE}$(0:3) negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00) | 43.50 | — | 35.50 | — | 28.00 | — | 20.70 | — | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B30c | $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 x B1 - 3.00) | 8.40 | — | 6.40 | — | 4.50 | — | 2.70 | — | ns |
| B30d | $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1 | 38.67 | — | 31.38 | — | 24.50 | — | 17.83 | — | ns |
| B31 | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 X B1 + 6.00) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B31a | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B31b | CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00) | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B31c | CLKOUT rising edge to $\overline{CS}$ valid- as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.30) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B31d | CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 x B1 + 6.6) | 9.40 | 18.00 | 7.60 | 16.00 | 13.30 | 14.10 | 11.30 | 12.30 | ns |
| B32 | CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B32a | CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B32b | CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00) | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B32c | CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B32d | CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 x B1 + 6.60) | 9.40 | 18.00 | 7.60 | 16.00 | 13.30 | 14.10 | 11.30 | 12.30 | ns |
| B33 | CLKOUT falling edge to $\overline{GPL}$ valid - as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B33a | CLKOUT rising edge to $\overline{GPL}$ Valid - as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B34 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B34a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B34b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM (MIN = 0.75 x B1 - 2.00) | 20.70 | — | 16.70 | — | 13.00 | — | 9.40 | — | ns |
| B35 | A(0:31), BADDR(28:30) to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B35a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - As Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B35b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 x B1 - 2.00) | 20.70 | — | 16.70 | — | 13.00 | — | 9.40 | — | ns |
| B36 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B37 | UPWAIT valid to CLKOUT falling edge [12] (MIN = 0.00 x B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B38 | CLKOUT falling edge to UPWAIT valid [12] (MIN = 0.00 x B1 + 1.00) | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| B39 | $\overline{AS}$ valid to CLKOUT rising edge [13] (MIN = 0.00 x B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B40 | A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 x B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B41 | $\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 x B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B42 | CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 x B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B43 | $\overline{AS}$ negation to memory controller signals negation (MAX = TBD) | — | TBD | — | TBD | — | TBD | — | TBD | ns |

1 Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

2 If the rate of change of the frequency of EXTAL is slow (I.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (I.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

3 The timings specified in B4 and B5 are based on full strength clock.

4 The timing for $\overline{BR}$ output is relevant when the MPC862/857T/857DSL is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC862/857T/857DSL is selected to work with internal bus arbiter.

5 For part speeds above 50MHz, use 9.80ns for B11a.

6 The timing required for $\overline{BR}$ input is relevant when the MPC862/857T/857DSL is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC862/857T/857DSL is selected to work with external bus arbiter.

7 For part speeds above 50MHz, use 2ns for B17.

8 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

9 For part speeds above 50MHz, use 2ns for B19.

10 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

11 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

12 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 19.

13 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 22.

Figure 4 is the control timing diagram.

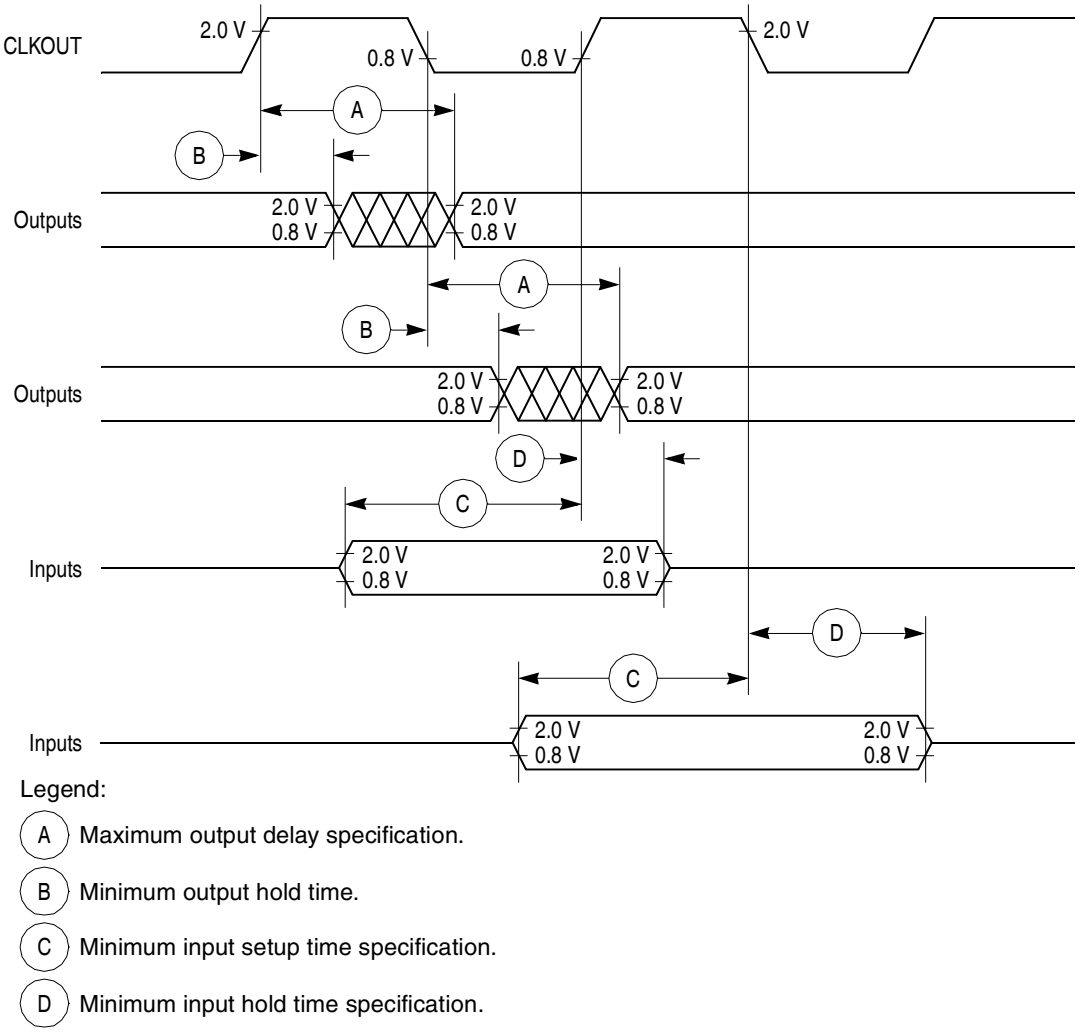


**Figure 4. Control Timing**

Figure 5 provides the timing for the external clock.

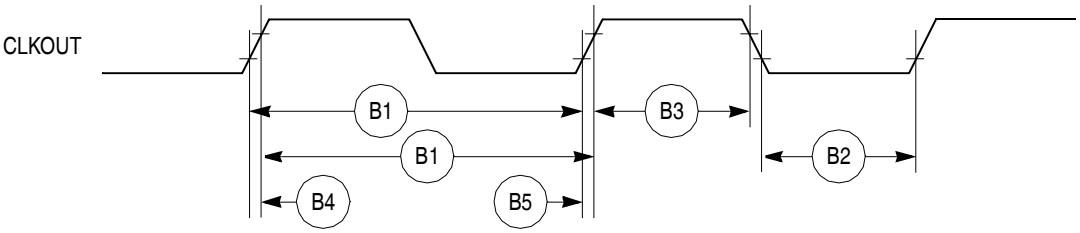


**Figure 5. External Clock Timing**

Figure 6 provides the timing for the synchronous output signals.

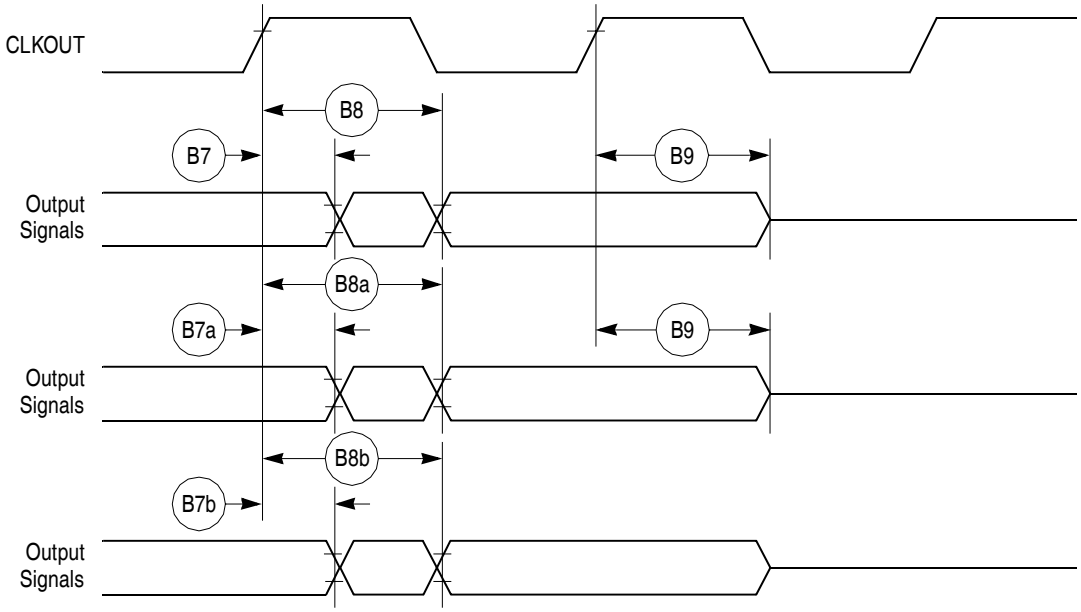


**Figure 6. Synchronous Output Signals Timing**

Figure 7 provides the timing for the synchronous active pull-up and open-drain output signals.

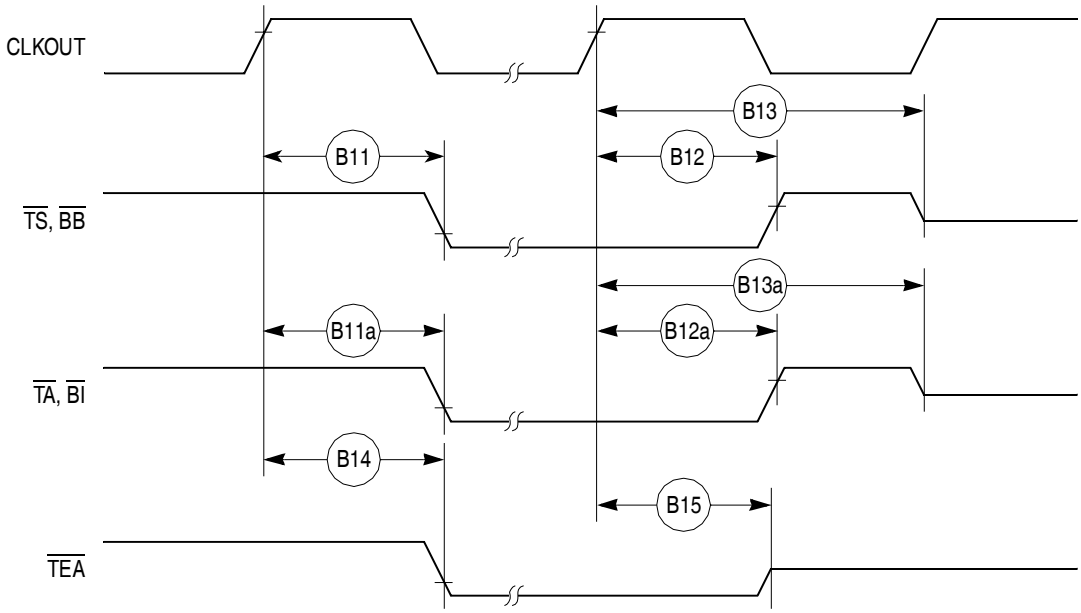


**Figure 7. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing**