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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



3.3 V 1:60 LVCMOS PLL Clock Generator

The MPC9330 is a 3.3 V compatible, 1:6 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance telecomm, networking and computing applications. With output frequencies up to 120 MHz and output skews less than 150 ps, the device meets the needs of the most demanding clock applications. The MPC9330 is specified for the temperature range of 0°C to +70°C.

Features

- 1:6 PLL based low-voltage clock generator
- 3.3 V power supply
- Generates clock signals up to 120 MHz
- Maximum output skew of 150 ps
- On-chip crystal oscillator clock reference
- Alternative LVCMOS PLL reference clock input
- Internal and external PLL feedback
- PLL multiplies the reference clock by 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3, or x/4
- Supports zero-delay operation in external feedback mode
- Synchronous output clock stop in logic low eliminates output runt pulses
- Power_down feature reduces output clock frequency
- Drives up to 12 clock lines
- 32-lead LQFP packaging
- 32-lead Pb-free package available
- Ambient temperature range 0°C to +70°C
- Internal power-up reset
- Pin and function compatible to the MPC930

Functional Description

The MPC9330 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9330 requires either the selection of internal PLL feedback or the connection of one of the device outputs to the feedback input to close the PLL feedback path in external feedback mode. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. In external PLL feedback configuration and with the available post-PLL dividers (divide-by-2, divide-by-4 and divide-by-6), the internal VCO of the MPC9330 is running at either 4x, 8x, 12x, 16x, or 24x of the reference clock frequency. In internal feedback configuration (divide-by-16) the internal VCO is running 16x of the reference frequency. The frequency of the QA, QB, QC output banks is a division of the VCO frequency and can be configured independently for each output bank using the FSELA, FSELB and FSELC pins, respectively. The available output to input frequency ratios are 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3, or x/4.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible input as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be disabled (high-impedance) by deasserting the OE/MR pin. In the PLL configuration with external feedback selected, deasserting OE/MR causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Asserting OE/MR will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The MPC9330 output clock stop control allows the outputs to start and stop synchronously in the logic low state, without the potential generation of runt pulses.

The MPC9330 is fully 3.3 V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9330 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MPC9330

**3.3 V 1:6 LVCMOS
PLL CLOCK GENERATOR**



**FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03**



**AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03**

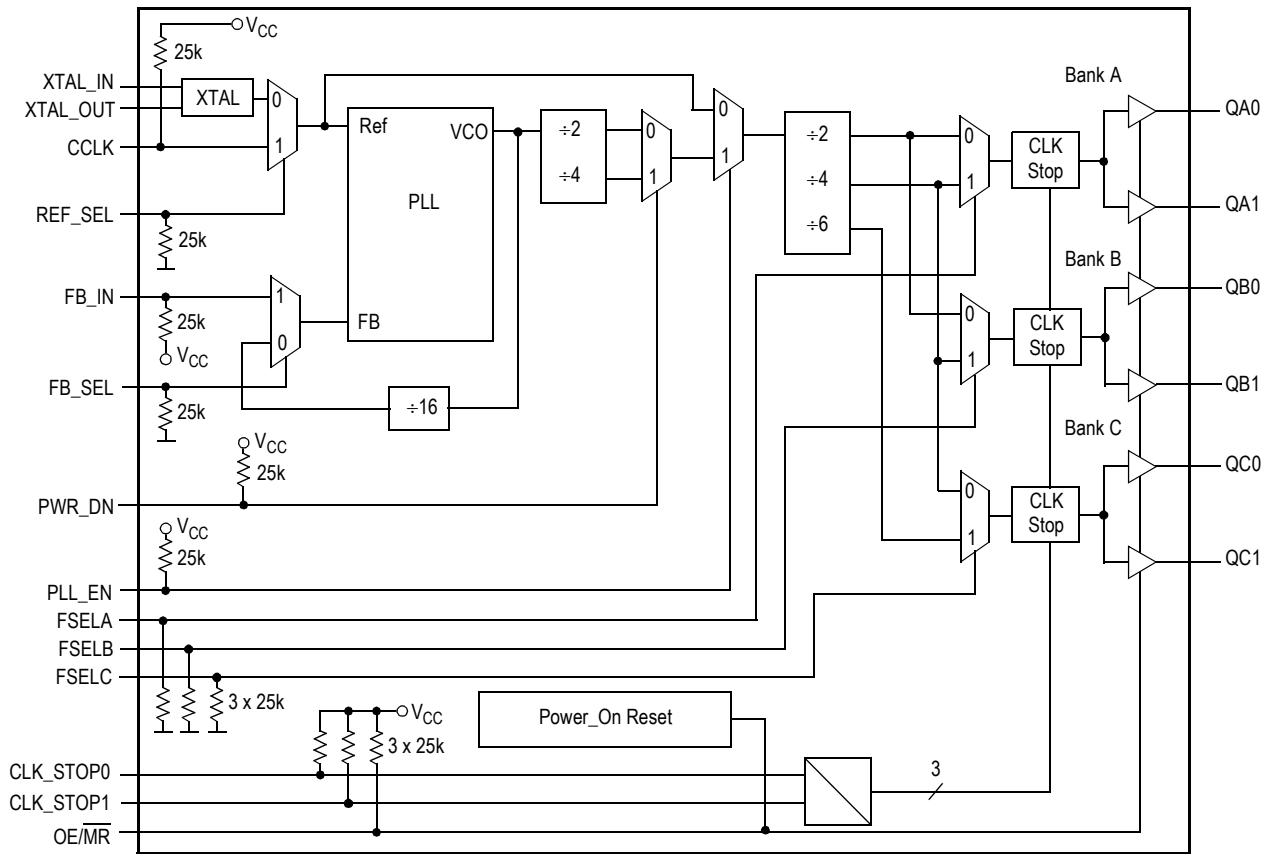
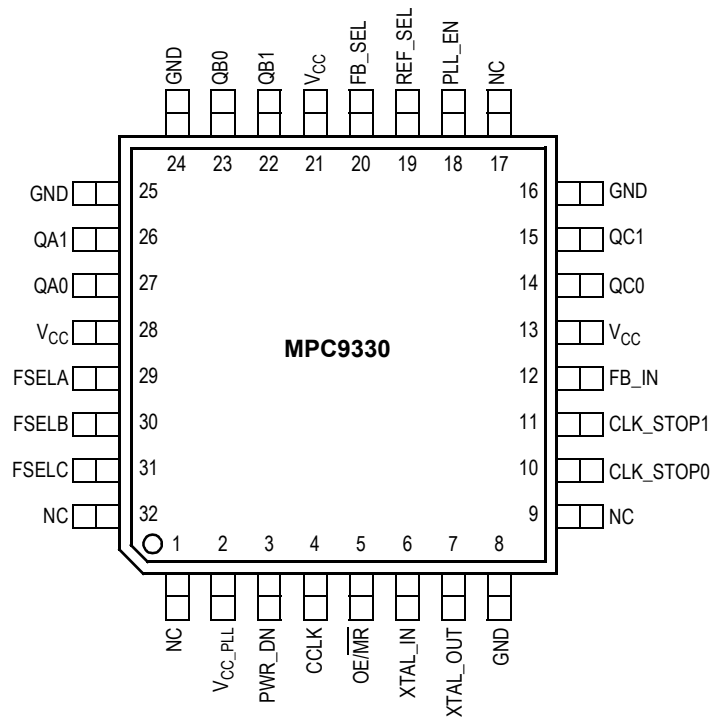


Figure 1. MPC9330 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see application section for details.

Figure 2. MPC9330 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

| Pin | I/O | Type | Function |
|---------------------|--------|-----------------|--|
| CCLK | Input | LVC MOS | PLL reference clock signal |
| XTAL_IN, XTAL_OUT | Input | Analog | Crystal oscillator interface |
| FB_IN | Input | LVC MOS | PLL feedback signal input, connect to an output |
| FB_SEL | Input | LVC MOS | Feedback select |
| REF_SEL | Input | LVC MOS | Reference clock select |
| PWR_DN | Input | LVC MOS | Output frequency and power down select |
| FSELA | Input | LVC MOS | Frequency divider select for bank A outputs |
| FSELB | Input | LVC MOS | Frequency divider select for bank B outputs |
| FSELC | Input | LVC MOS | Frequency divider select for bank C outputs |
| PLL_EN | Input | LVC MOS | PLL enable/disable |
| CLK_STOP0-1 | Input | LVC MOS | Clock output enable/disable |
| OE/MR | Input | LVC MOS | Output enable/disable (high-impedance tristate) and device reset |
| QA0-1, QB0-1, QC0-1 | Output | LVC MOS | Clock outputs |
| GND | Supply | Ground | Negative power supply |
| V _{CC_PLL} | Supply | V _{CC} | PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V _{CC_PLL} . Please see applications section for details. |
| V _{CC} | Supply | V _{CC} | Positive power supply for I/O and core. All V _{CC} pins must be connected to the positive power supply for correct operation. |

Table 2. Function Table

| Control | Default | 0 | 1 |
|---|---------|---|---|
| REF_SEL | 0 | The crystal oscillator output is the PLL reference clock | CCLK is the PLL reference clock |
| FB_SEL | 0 | Internal PLL feedback of 16. $f_{VCO} = 16 * f_{ref}$ | External feedback. Zero-delay operation enabled for CCLK as reference clock |
| PLL_EN | 1 | Test mode with PLL disabled. The reference clock is substituted for the internal VCO output. MPC9330 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Normal operation mode with PLL enabled. |
| PWR_DN | 1 | VCO ÷ 2 (High output frequency range) | VCO ÷ 4 (Low output frequency range) |
| FSELA | 0 | Output divider ÷ 2 | Output divider ÷ 4 |
| FSELB | 0 | Output divider ÷ 2 | Output divider ÷ 4 |
| FSELC | 0 | Output divider ÷ 4 | Output divider ÷ 6 |
| CLK_STOP[0:1] | 11 | See Table 3 | |
| OE/MR | 1 | Outputs disabled (high-impedance state) and reset of the device. During reset in external feedback configuration, the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9330 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLK). Reset does not affect PLL lock in internal feedback configuration. | Outputs enabled (active) |
| PWR_DN, FSELA, FSELB and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 8 through Table 10 for supported frequency ranges and output to input frequency ratios. | | | |

Table 3. Clock Output Synchronous Disable (CLK_STOP) Function Table⁽¹⁾

| CLK_STOP0 | CLK_STOP1 | QA[0:1] | QB[0:1] | QC[0:1] |
|-----------|-----------|--------------------------|--------------------------|--------------------------|
| 0 | 0 | Active | Stopped in logic L state | Stopped in logic L state |
| 0 | 1 | Active | Stopped in logic L state | Active |
| 1 | 0 | Stopped in logic L state | Stopped in logic L state | Active |
| 1 | 1 | Active | Active | Active |

1. Output operation for OE/MR=1 (outputs enabled). OE/MR=0 will disable (high-impedance state) all outputs independent on CLK_STOP[0:1].

Table 4. General Specifications

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|-----------------|-----------------------------------|------|---------------------|-----|------|------------|
| V _{TT} | Output Termination Voltage | | V _{CC} ÷ 2 | | V | |
| MM | ESD Protection (Machine Model) | 200 | | | V | |
| HBM | ESD Protection (Human Body Model) | 2000 | | | V | |
| LU | Latch-Up Immunity | 200 | | | mA | |
| C _{PD} | Power Dissipation Capacitance | | 10 | | pF | Per output |
| C _{IN} | Input Capacitance | | 4.0 | | pF | Inputs |

Table 5. Absolute Maximum Ratings⁽¹⁾

| Symbol | Characteristics | Min | Max | Unit | Condition |
|------------------|---------------------|------|----------------------|------|-----------|
| V _{CC} | Supply Voltage | -0.3 | 3.9 | V | |
| V _{IN} | DC Input Voltage | -0.3 | V _{CC} +0.3 | V | |
| V _{OUT} | DC Output Voltage | -0.3 | V _{CC} +0.3 | V | |
| I _{IN} | DC Input Current | | ±20 | mA | |
| I _{OUT} | DC Output Current | | ±50 | mA | |
| T _S | Storage Temperature | -65 | 125 | °C | |

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---------------------|----------------------------------|-----|---------|-----------------------|--------|--|
| V _{IH} | Input High Voltage | 2.0 | | V _{CC} + 0.3 | V | LVC MOS |
| V _{IL} | Input Low Voltage | | | 0.8 | V | LVC MOS |
| V _{OH} | Output High Voltage | 2.4 | | | V | I _{OH} = -24 mA ⁽¹⁾ |
| V _{OL} | Output Low Voltage | | | 0.55 0.30 | V V | I _{OL} = 24 mA I _{OL} = 12 mA |
| Z _{OUT} | Output Impedance | | 14 – 17 | | Ω | |
| I _{IN} | Input Current ⁽²⁾ | | | ±100 | μA | V _{IN} = V _{CC} or GND |
| I _{CC_PLL} | Maximum PLL Supply Current | | 5.0 | 10 | mA | V _{CC_PLL} Pin |
| I _{CCQ} | Maximum Quiescent Supply Current | | 5.0 | 10 | mA | All V _{CC} Pins |

1. The MPC9330 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. Inputs have pull-down or pull-up resistors affecting the input current.

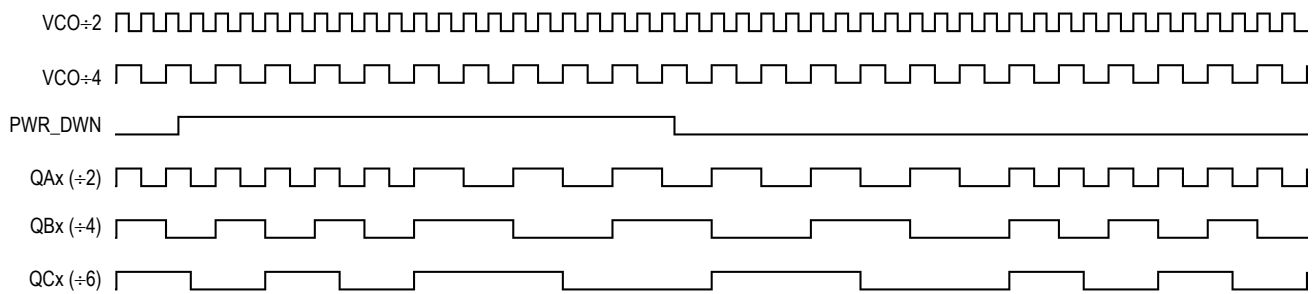
Table 7. AC Characteristics ($V_{CC} = 3.3\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C)⁽¹⁾

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition | |
|------------------------|--|----------------------------------|-------|----------|------|---------------|------------|
| f_{ref} | Input Reference Frequency ⁽²⁾ PLL mode, external feedback | $\div 4$ feedback ⁽³⁾ | 50 | | 120 | MHz | PLL locked |
| | | $\div 8$ feedback | 25 | | 60 | MHz | |
| | PLL mode, internal feedback Input Reference Frequency in PLL bypass mode ⁽⁴⁾ | $\div 12$ feedback | 16.67 | | 40 | MHz | |
| | | $\div 16$ feedback | 12.5 | | 30 | MHz | |
| | | $\div 24$ feedback | 8.33 | | 20 | MHz | |
| | | $(\div 16$ feedback) | 12.5 | | 30 | MHz | |
| | | | | TBD | MHz | | |
| f_{VCO} | VCO Lock Frequency Range ⁽⁵⁾ | 200 | | 480 | MHz | | |
| f_{XTAL} | Crystal Interface Frequency Range ⁽⁶⁾ | 10 | | 25 | MHz | | |
| f_{MAX} | Output Frequency | $\div 4$ output | 50 | | 120 | MHz | PLL locked |
| | | $\div 8$ output | 25 | | 60 | MHz | |
| | | $\div 12$ output | 16.67 | | 40 | MHz | |
| | | $\div 16$ output | 12.5 | | 30 | MHz | |
| | | $\div 24$ output | 8.33 | | 20 | MHz | |
| f_{refDC} | Reference Input Duty Cycle | 25 | | 75 | % | | |
| $t_{PW, MIN}$ | Minimum Input Reference Pulse Width | 2 | | | ns | | |
| t_r, t_f | CCLK Input Rise/Fall Time | | | 1.0 | ns | 0.8 to 2.0 V | |
| $t_{(\varnothing)}$ | Propagation Delay (SPO) ⁽⁷⁾ for the | - entire f_{ref} range | -1.2 | | +1.2 | ° | |
| | | - $f_{ref} = 8.33\text{ MHz}$ | -400 | | +400 | ps | |
| | | - $f_{ref} = 50.0\text{ MHz}$ | -70 | | +70 | ps | |
| $t_{sk(o)}$ | Output-to-Output Skew ⁽⁸⁾ (within output bank) (any output) | | | 50 | ps | | |
| | | | | 150 | ps | | |
| DC | Output Duty Cycle | 45 | 50 | 55 | % | | |
| t_r, t_f | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.55 to 2.4 V | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | 10 | ns | | |
| $t_{PZL, LZ}$ | Output Enable Time | | | 10 | ns | | |
| $t_{JIT(CC)}$ | Cycle-to-cycle jitter | | 50 | 300 | ps | | |
| $t_{JIT(PER)}$ | Period Jitter | | 35 | 250 | ps | | |
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter RMS (1σ) | | 10 | 70 | ps | | |
| BW | PLL closed loop bandwidth ⁽⁹⁾ PLL mode, external feedback | $\div 4$ feedback | | 0.8-5.0 | | MHz | |
| | | $\div 8$ feedback | | 0.5-2.0 | | MHz | |
| | | $\div 12$ feedback | | 0.3-1.0 | | MHz | |
| | | $\div 16$ feedback | | 0.25-0.6 | | MHz | |
| | | $\div 24$ feedback | | 0.2-0.5 | | MHz | |
| t_{LOCK} | Maximum PLL Lock Time | | | 10 | ms | | |

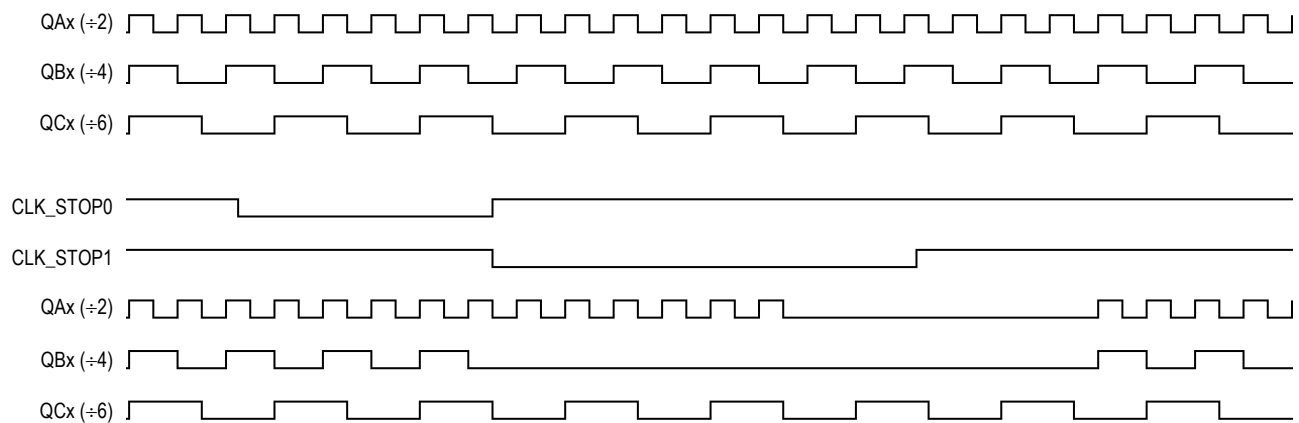
- AC characteristics apply for parallel output termination of $50\ \Omega$ to V_{TT} .
- PLL mode requires $PLL_EN = 0$ to enable the PLL.
- $\div 4$ feedback (FB) can be accomplished by setting $PWR_DN = 0$ and the connection of one $\div 2$ output to FB_IN . See [Table 3](#) to [Table 5](#) for other feedback configurations.
- In bypass mode, the MPC9330 divides the input reference clock.
- The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
- The usable crystal frequency range depends on the VCO lock frequency and the PLL feedback ratio.
- SPO is the static phase offset between CCLK and FB_IN ($FB_SEL=1$ and PLL locked). $t_{sk(o)} [ps] = t_{sk(o)} [^\circ] B(fref \div 360^\circ)$
- Skew data applicable for equally loaded outputs only.
- -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Output Power Down (PWR_DN) Timing Diagram



Output Clock Stop (CLK_STOP) Timing Diagram



Programming the MPC9330

The MPC9330 supports output clock frequencies from 8.33 to 120 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 480 MHz for stable and optimal

operation. The FSELA, FSELB, FSELC and PWR_DN pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:4, 1:3, 1:2, 1:1, 2:3, 4:3 and 3:2. [Table 8](#) through [Table 10](#) illustrate the various output configurations and frequency ratios supported by the MPC9330.

Table 8. MPC9330 Example Configurations (Internal Feedback: FB_SEL = 0)

| fref ⁽¹⁾ [MHz] | PWR_DN | FSELA | FSELB | FSELC | QA[0:1]:fref ratio | QB[0:1]:fref ratio | QC[0:1]:fref ratio |
|---------------------------|--------|-------|-------|--------------------|-----------------------|----------------------------|----------------------------|
| 12.5–30.0 | 0 | 0 | 0 | 0 | fref · 4 (50-120 MHz) | fref · 4 (50-120 MHz) | fref · 2 (25-60 MHz) |
| | 0 | 0 | 0 | 1 | fref · 4 (50-120 MHz) | fref · 4 (50-120 MHz) | fref · 4 ÷ 3 (16.6-40 MHz) |
| | 0 | 0 | 1 | 0 | fref · 4 (50-120 MHz) | fref · 2 (25-60 MHz) | fref · 2 (25-60 MHz) |
| | 0 | 0 | 1 | 1 | fref · 4 (50-120 MHz) | fref · 2 (25-60 MHz) | fref · 4 ÷ 3 (16.6-40 MHz) |
| | 0 | 1 | 0 | 0 | fref · 2 (25-60 MHz) | fref · 4 (50-120 MHz) | fref · 2 (25-60 MHz) |
| | 0 | 1 | 0 | 1 | fref · 2 (25-60 MHz) | fref · 4 (50-120 MHz) | fref · 4 ÷ 3 (16.6-40 MHz) |
| | 0 | 1 | 1 | 0 | fref · 2 (25-60 MHz) | fref · 2 (25-60 MHz) | fref · 2 (25-60 MHz) |
| | 0 | 1 | 1 | 1 | fref · 2 (25-60 MHz) | fref · 2 (25-60 MHz) | fref · 4 ÷ 3 (16.6-40 MHz) |
| | 1 | 0 | 0 | 0 | fref · 2 (25-60 MHz) | fref · 2 (25-60 MHz) | fref (12.5-30 MHz) |
| | 1 | 0 | 0 | 1 | fref · 2 (25-60 MHz) | fref · 2 (25-60 MHz) | fref · 2 ÷ 3 (8.33-20 MHz) |
| | 1 | 0 | 1 | 0 | fref · 2 (25-60 MHz) | fref (12.5-30 MHz) | fref (12.5-30 MHz) |
| | 1 | 0 | 1 | 1 | fref · 2 (25-60 MHz) | fref (12.5-30 MHz) | fref · 2 ÷ 3 (8.33-20 MHz) |
| | 1 | 1 | 0 | 0 | fref (12.5-30 MHz) | fref · 2 (25-60 MHz) | fref (12.5-30 MHz) |
| | 1 | 1 | 0 | 1 | fref (12.5-30 MHz) | fref · 2 (25-60 MHz) | fref · 2 ÷ 3 (8.33-20 MHz) |
| 1 | 1 | 1 | 0 | fref (12.5-30 MHz) | fref (12.5-30 MHz) | fref (12.5-30 MHz) | |
| 1 | 1 | 1 | 1 | fref (12.5-30 MHz) | fref (12.5-30 MHz) | fref · 2 ÷ 3 (8.33-20 MHz) | |

1. fref is the input clock reference frequency (CCLK or XTAL).

Table 9. MPC9330 Example Configurations (External Feedback and PWR_DN = 0)

| PLL Feedback | fref ⁽¹⁾ [MHz] | FSELA | FSELB | FSELC | QA[0:1]:fref ratio | QB[0:1]:fref ratio | QC[0:1]:fref ratio |
|-------------------------|---------------------------|-------|-------|-------|--------------------------|--------------------------|--------------------------|
| VCO ÷ 4 ⁽²⁾ | 50–120 | 0 | 0 | 0 | fref (50-120 MHz) | fref (50-120 MHz) | fref ÷ 2 (25-60 MHz) |
| | | 0 | 0 | 1 | fref (50-120 MHz) | fref (50-120 MHz) | fref ÷ 3 (16.6-40 MHz) |
| | | 0 | 1 | 0 | fref (50-120 MHz) | fref ÷ 2 (25-60 MHz) | fref ÷ 2 (25-60 MHz) |
| | | 0 | 1 | 1 | fref (50-120 MHz) | fref ÷ 2 (25-60 MHz) | fref ÷ 3 (16.6-40 MHz) |
| VCO ÷ 8 ⁽³⁾ | 25–60 | 1 | 0 | 0 | fref (25-60 MHz) | fref · 2 (50-120 MHz) | fref (25-60 MHz) |
| | | 1 | 0 | 1 | fref (25-60 MHz) | fref · 2 (50-120 MHz) | fref 2 ÷ 3 (16.6-40 MHz) |
| | | 1 | 1 | 0 | fref (25-60 MHz) | fref (25-60 MHz) | fref (25-60 MHz) |
| | | 1 | 1 | 1 | fref (25-60 MHz) | fref (25-60 MHz) | fref 2 ÷ 3 (16.6-40 MHz) |
| VCO ÷ 12 ⁽⁴⁾ | 16.67–40 | 0 | 0 | 1 | fref · 3 (50-120 MHz) | fref · 3 (50-120 MHz) | fref (16.6-40 MHz) |
| | | 0 | 1 | 1 | fref · 3 (50-120 MHz) | fref · 3 ÷ 2 (25-60 MHz) | fref (16.6-40 MHz) |
| | | 1 | 0 | 1 | fref · 3 ÷ 2 (25-60 MHz) | fref · 3 (50-120 MHz) | fref (16.6-40 MHz) |
| | | 1 | 1 | 1 | fref · 3 ÷ 2 (25-60 MHz) | fref · 3 ÷ 2 (25-60 MHz) | fref (16.6-40 MHz) |

1. fref is the input clock reference frequency (CCLK or XTAL).

2. QAx connected to FB_IN and FSELA=0, PWR_DN=0.

3. QAx connected to FB_IN and FSELA=1, PWR_DN=0.

4. QCx connected to FB_IN and FSELC=1, PWR_DN=0.

Table 10. MPC9330 Example Configurations (External Feedback and PWR_DN = 1)

| PLL Feedback | fref ⁽¹⁾ [MHz] | FSELA | FSELB | FSELC | QA[0:1]:fref ratio | QB[0:1]:fref ratio | QC[0:1]:fref ratio |
|-------------------------|---------------------------|-------|-------|-------|--------------------------|--------------------------|--------------------------|
| VCO ÷ 16 ⁽²⁾ | 12.5–30 | 1 | 0 | 0 | fref (12.5-30 MHz) | fref 2 (25-60 MHz) | fref (12.5-30 MHz) |
| | | 1 | 0 | 1 | fref (12.5-30 MHz) | fref 2 (25-60 MHz) | fref 2 ÷ 3 (8.33-20 MHz) |
| | | 1 | 1 | 0 | fref (12.5-30 MHz) | fref (12.5-30 MHz) | fref (12.5-30 MHz) |
| | | 1 | 1 | 1 | fref (12.5-30 MHz) | fref (12.5-30 MHz) | fref 2 ÷ 3 (8.33-20 MHz) |
| VCO ÷ 24 ⁽³⁾ | 8.33–20 | 0 | 0 | 1 | fref 3 (25-60 MHz) | fref 3 (25-60 MHz) | fref (8.33-20 MHz) |
| | | 0 | 1 | 1 | fref 3 (25-60 MHz) | fref 3 ÷ 2 (12.5-30 MHz) | fref (8.33-20 MHz) |
| | | 1 | 0 | 1 | fref 3 ÷ 2 (12.5-30 MHz) | fref 3 (25-60 MHz) | fref (8.33-20 MHz) |
| | | 1 | 1 | 1 | fref 3 ÷ 2 (12.5-30 MHz) | fref 3 ÷ 2 (12.5-30 MHz) | fref (8.33-20 MHz) |

1. fref is the input clock reference frequency (CCLK or XTAL).

2. QAx connected to FB_IN and FSELA=1, PWR_DN=1.

3. QCx connected to FB_IN and FSELC=1, PWR_DN=1.

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9330 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance, I/O jitter. The MPC9330 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9330. Figure 3 illustrates a typical power supply filter scheme. The MPC9330 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet, the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 5 mA (10 mA maximum), assuming that a minimum of 2.985 V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 3 should have a resistance of 10–15 Ω to meet the voltage drop criteria.

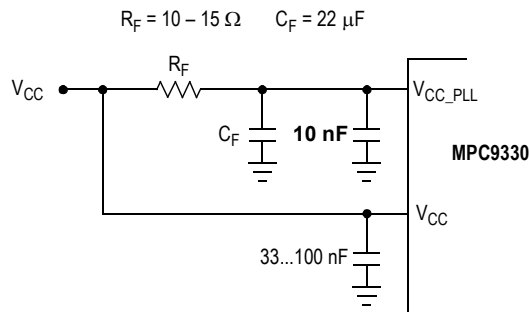


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz, and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and, thus, increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9330 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in

this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9330 clock driver was designed to drive high-speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω , the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Freescale application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9330 clock driver. For the series terminated case, however, there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9330 clock driver is effectively doubled due to its capability to drive multiple lines.

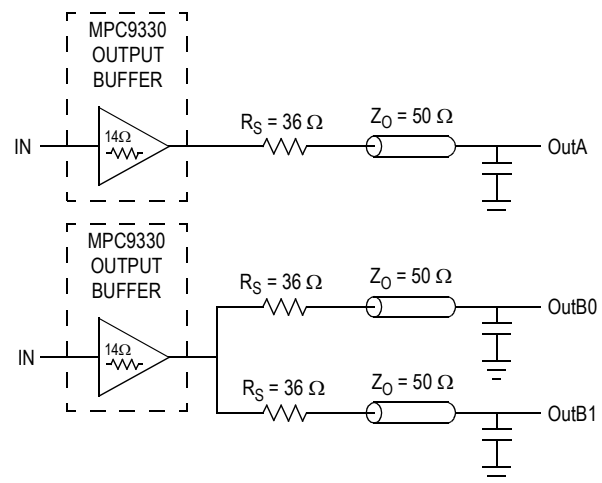


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 4 show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9330 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9330. The output waveform in Figure 5 shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of

the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$

$$Z_0 = 50 \Omega \parallel 50 \Omega$$

$$R_S = 36 \Omega \parallel 36 \Omega$$

$$R_0 = 14 \Omega$$

$$V_L = 3.0 (25 \div (18 + 14 + 25))$$

$$= 1.31 \text{ V}$$

At the load end, the voltage will double due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

1. Final skew data pending specification.

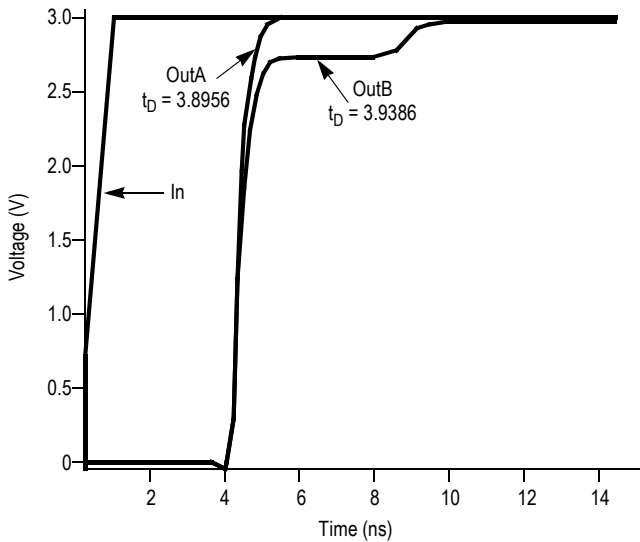


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region, it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.

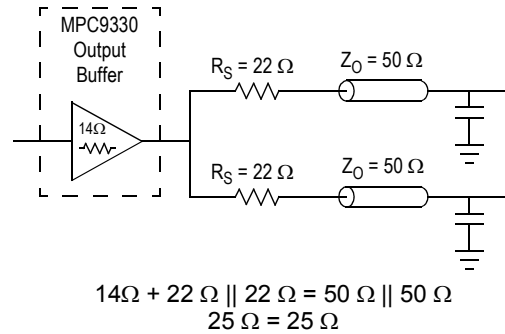


Figure 6. Optimized Dual Line Termination

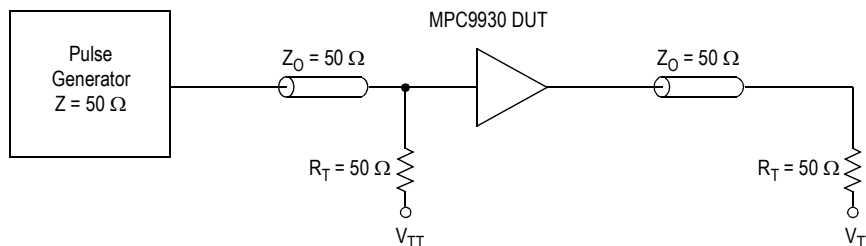
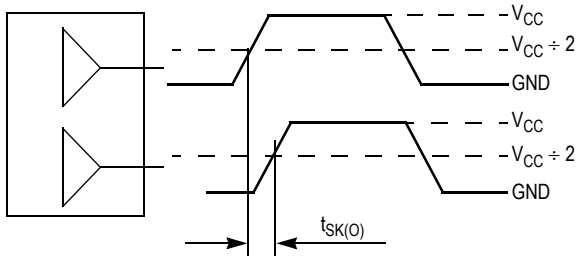


Figure 7. CCLK MPC9330 AC Test Reference for $V_{CC} = 3.3 \text{ V}$



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-Output Skew $t_{sk(O)}$

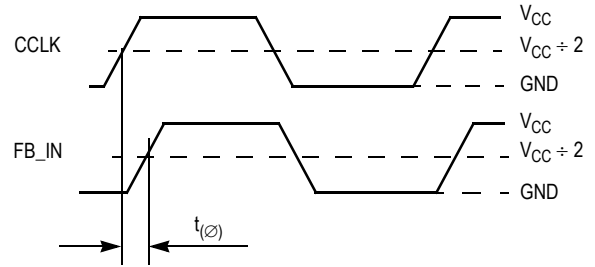
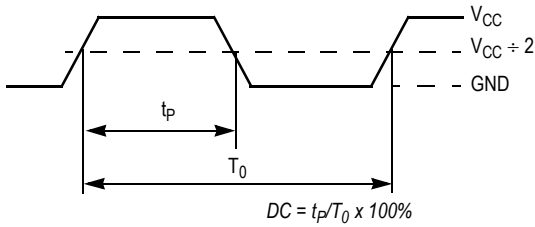
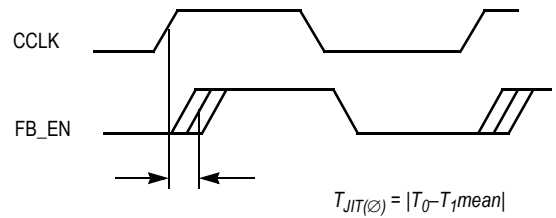


Figure 9. Propagation Delay ($t_{(0)}$, static phase offset) Test Reference



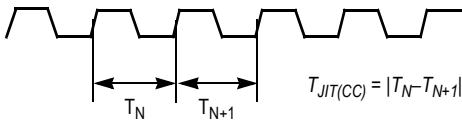
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 10. Output Duty Cycle (DC)



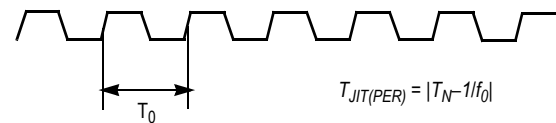
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 11. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 12. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 13. Period Jitter

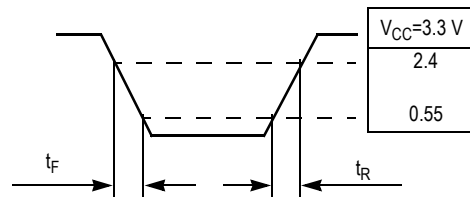
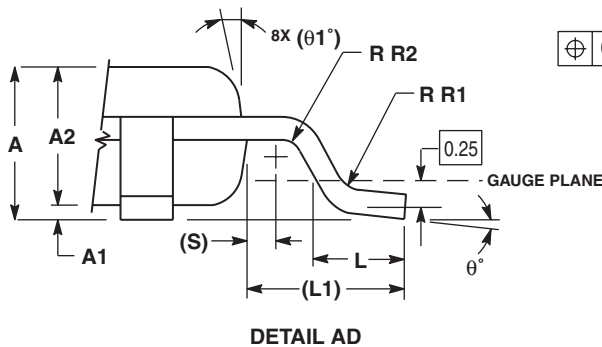
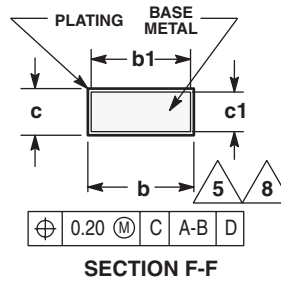
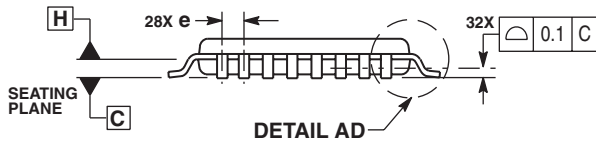
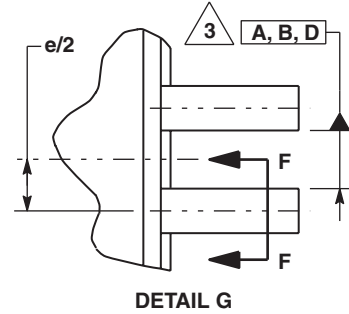
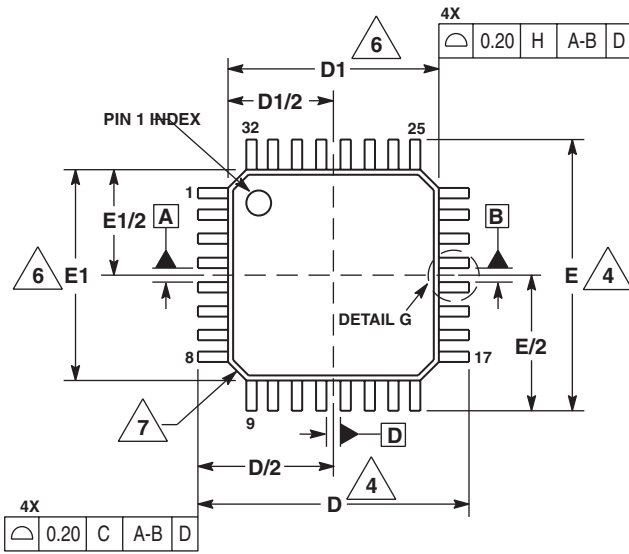


Figure 14. Output Transition Time Test Reference

PACKAGE DIMENSIONS



- NOTES:
- DIMENSIONS ARE IN MILLIMETERS.
 - INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 - DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
 - DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
 - DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
 - DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
 - EXACT SHAPE OF EACH CORNER IS OPTIONAL.
 - THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 1.40 | 1.60 |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| b | 0.30 | 0.45 |
| b1 | 0.30 | 0.40 |
| c | 0.09 | 0.20 |
| c1 | 0.09 | 0.16 |
| D | 9.00 | BSC |
| D1 | 7.00 | BSC |
| e | 0.80 | BSC |
| E | 9.00 | BSC |
| E1 | 7.00 | BSC |
| L | 0.50 | 0.70 |
| L1 | 1.00 | REF |
| q | 0° | 7° |
| q1 | 12 | REF |
| R1 | 0.08 | 0.20 |
| R2 | 0.08 | --- |
| S | 0.20 | REF |

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How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
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For Literature Requests Only:

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