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## 3.3V/2.5V LVCMOS 1:12 Clock Fanout Buffer

The MPC9448 is a 3.3V or 2.5V compatible, 1:12 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 350 MHz and output skews less than 150 ps, the device meets the needs of most demanding clock applications.

- 12 LVCMOS compatible clock outputs
- Selectable LVCMOS and differential LVPECL compatible clock inputs
- Maximum clock frequency of 350 MHz
- Maximum clock skew of 150 ps
- Synchronous output stop in logic low state eliminates output runt pulses
- High-impedance output control
- 3.3V or 2.5V power supply
- Drives up to 24 series terminated clock lines
- Ambient temperature range -40°C to +85°C
- 32-Lead LQFP packaging
- Supports clock distribution in networking, telecommunication and computing applications
- Pin and function compatible to MPC948

### Functional Description

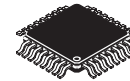
The MPC9448 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 350 MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each output is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable, independent clock inputs are available, providing support of LVCMOS and differential LVPECL clock distribution systems. The MPC9448 CLK\_STOP control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of -40°C to +85°C. The MPC9448 is pin and function compatible but performance-enhanced to the MPC948.

**MPC9448**

**LOW VOLTAGE  
3.3V/2.5V LVCMOS 1:12  
CLOCK FANOUT BUFFER**



**FA SUFFIX**  
32-LEAD LQFP PACKAGE  
CASE 873A

# MPC9448

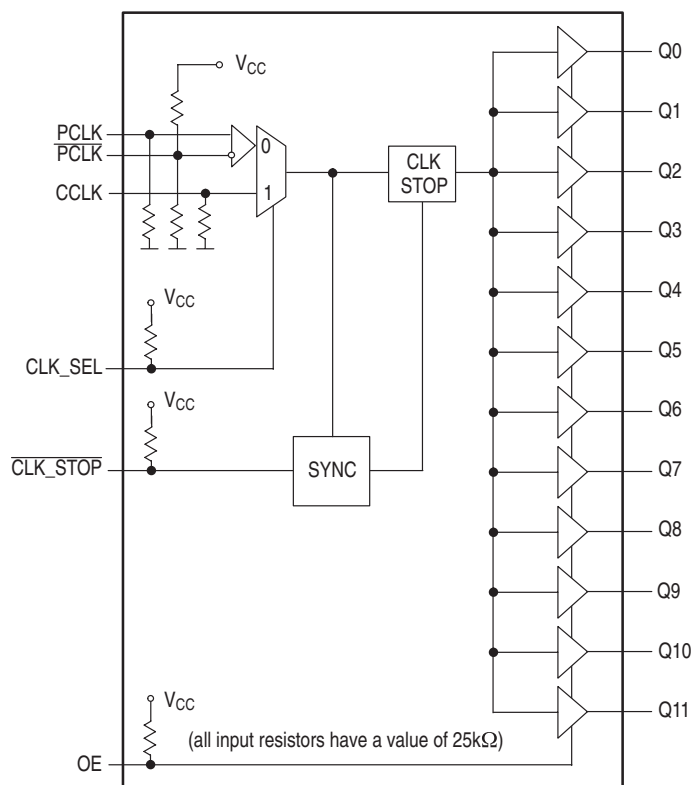


Figure 1. Logic Diagram

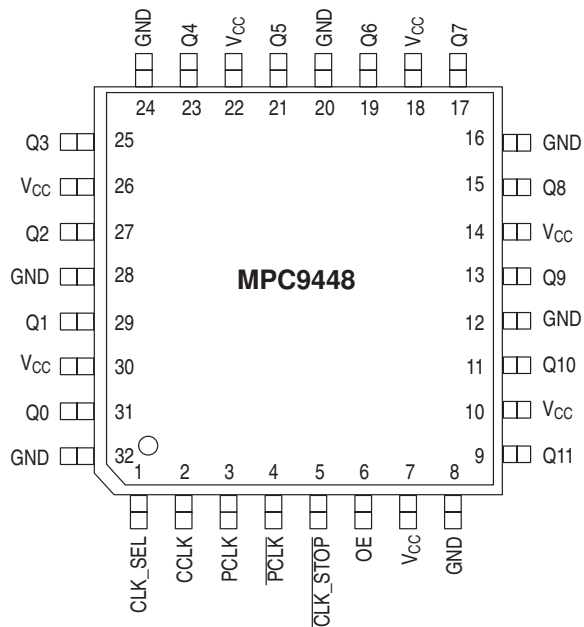


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. FUNCTION TABLE

Control	Default	0	1
CLK_SEL	1	PECL differential input selected	CCLK input selected
OE	1	Outputs disabled (high-impedance state) <sup>1</sup>	Outputs enabled
CLK_STOP	1	Outputs synchronously stopped in logic low state	Outputs active

1. OE=0 will high-impedance tristate all outputs independent on CLK\_STOP.

Table 2. PIN CONFIGURATION

Pin	I/O	Type	Function
PCLK, PCLK	Input	LVPECL	Clock signal input
CCLK	Input	LVC MOS	Alternative clock signal input
CLK_SEL	Input	LVC MOS	Clock input select
CLK_STOP	Input	LVC MOS	Clock output enable/disable
OE	Input	LVC MOS	Output enable/disable (high-impedance tristate)
Q0–11	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

**Table 3. ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	-0.3	3.9	V
V <sub>IN</sub>	DC Input Voltage	-0.3	V <sub>CC</sub> + 0.3	V
V <sub>OUT</sub>	DC Output Voltage	-0.3	V <sub>CC</sub> + 0.3	V
I <sub>IN</sub>	DC Input Current		±20	mA
I <sub>OUT</sub>	DC Output Current		±50	mA
T <sub>Stor</sub>	Storage Temperature Range	-65	125	°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**Table 4. GENERAL SPECIFICATIONS**

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V <sub>TT</sub>	Output Termination Voltage		V <sub>CC</sub> ÷ 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-up Immunity	200			mA	
C <sub>PD</sub>	Power Dissipation Capacitance		10		pF	Per Output
C <sub>IN</sub>	Input Capacitance		4.0		pF	Inputs

**Table 5. DC CHARACTERISTICS** (V<sub>CC</sub> = 3.3V ±5%, T<sub>A</sub> = -40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V <sub>IH</sub>	Input HIGH Voltage	2.0		V <sub>CC</sub> + 0.3	V	LVCMOS
V <sub>IL</sub>	Input LOW Voltage	-0.3		0.8	V	LVCMOS
V <sub>PP</sub>	Peak-to-Peak Input Voltage	PCLK 250			mV	LVPECL
V <sub>CMR</sub> <sup>a</sup>	Common Mode Range	PCLK 1.1		V <sub>CC</sub> - 0.6	V	LVPECL
I <sub>IN</sub>	Input Current <sup>b</sup>			300	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
V <sub>OH</sub>	Output HIGH Voltage	2.4			V	I <sub>OH</sub> = -24mA <sup>c</sup>
V <sub>OL</sub>	Output LOW Voltage			0.55 0.30	V V	I <sub>OL</sub> = 24mA <sup>c</sup> I <sub>OL</sub> = 12mA
Z <sub>OUT</sub>	Output Impedance		17		Ω	
I <sub>CCQ</sub> <sup>d</sup>	Maximum Quiescent Supply Current			2.0	mA	All V <sub>CC</sub> Pins

- V<sub>CMR</sub> (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V<sub>CMR</sub> range and the input swing lies within the V<sub>PP</sub> (DC) specification.
- Input pull-up / pull-down resistors influence input current.
- The MPC9448 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V<sub>TT</sub>. Alternatively, the device drives up to two 50Ω series terminated transmission lines (for V<sub>CC</sub>=3.3V) or one 50Ω series terminated transmission line (for V<sub>CC</sub>=2.5V).
- I<sub>CCQ</sub> is the DC current consumption of the device with all outputs open and the input in its default state or open.

**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )<sup>a</sup>

Symbol	Characteristics	Min	Typ	Max	Unit	Condition	
$f_{ref}$	Input Frequency	0		350	MHz		
$f_{MAX}$	Maximum Output Frequency	0		350	MHz		
$V_{PP}$	Peak-to-peak input voltage	PCLK 400		1000	mV	LVPECL	
$V_{CMR}^b$	Common Mode Range	PCLK 1.3		$V_{CC}-0.8$	V	LVPECL	
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns		
$t_r, t_f$	CCLK Input Rise/Fall Time			1.0 <sup>c</sup>	ns	0.8 to 2.0V	
$t_{PLH/HL}$ $t_{PLH/HL}$	Propagation delay	PCLK to any Q 1.6 CCLK to any Q 1.3		3.6 3.3	ns		
$t_{PLZ, HZ}$	Output Disable Time			11	ns		
$t_{PZL, LZ}$	Output Enable Time			11	ns		
$t_S$	Setup time	CCLK to $\overline{CLK\_STOP}$ 0.0 PCLK to $\overline{CLK\_STOP}$ 0.0			ns		
$t_H$	Hold time	CCLK to $\overline{CLK\_STOP}$ 1.0 PCLK to $\overline{CLK\_STOP}$ 1.5			ns		
$t_{sk(O)}$	Output-to-output Skew			150	ps		
$t_{sk(PP)}$	Device-to-device Skew	PCLK or CCLK to any Q		2.0	ns		
$t_{SK(P)}$	Output pulse skew <sup>d</sup>	Using CCLK Using PCLK		300 400	ps		
DCQ	Output Duty Cycle	$f_Q < 170$ MHz	45	50	55	%	$DC_{REF} = 50\%$
$t_r, t_f$	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V

- a. AC characteristics apply for parallel output termination of  $50\Omega$  to  $V_{TT}$ .
- b.  $V_{CMR}$  (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the  $V_{CMR}$  range and the input swing lies within the  $V_{PP}$  (AC) specification. Violation of  $V_{CMR}$  or  $V_{PP}$  impacts  $t_{PLH/HL}$  and  $t_{SK(PP)}$ .
- c. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- d. Output pulse skew is the absolute difference of the propagation delay times:  $|t_{PLH} - t_{PHL}|$ .

**Table 7. DC CHARACTERISTICS** ( $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$V_{IH}$	Input high voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
$V_{IL}$	Input low voltage	-0.3		0.7	V	LVC MOS
$V_{PP}$	Peak-to-peak input voltage	PCLK 250			mV	LVPECL
$V_{CMR}^a$	Common Mode Range	PCLK 1.0		$V_{CC}-0.7$	V	LVPECL
$I_{IN}$	Input current <sup>b</sup>			300	$\mu A$	$V_{IN}=GND$ or $V_{IN}=V_{CC}$
$V_{OH}$	Output High Voltage	1.8			V	$I_{OH} = -15$ mA <sup>c</sup>
$V_{OL}$	Output Low Voltage			0.6	V	$I_{OL} = 15$ mA <sup>c</sup>
$Z_{OUT}$	Output impedance		19		$\Omega$	
$I_{CCQ}^d$	Maximum Quiescent Supply Current			2.0	mA	All $V_{CC}$ Pins

- a.  $V_{CMR}$  (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the  $V_{CMR}$  range and the input swing lies within the  $V_{PP}$  (DC) specification.
- b. Input pull-up / pull-down resistors influence input current.
- c. The MPC9448 is capable of driving  $50\Omega$  transmission lines on the incident edge. Each output drives one  $50\Omega$  parallel terminated transmission line to a termination voltage of  $V_{TT}$ . Alternatively, the device drives one  $50\Omega$  series terminated transmission lines at  $V_{CC}=2.5V$ .
- d.  $I_{CCQ}$  is the DC current consumption of the device with all outputs open and the input in its default state or open.

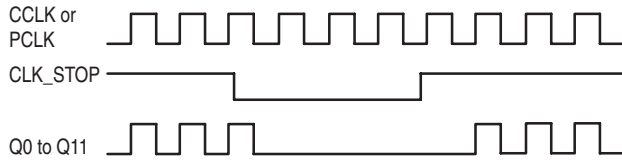
**Table 8. AC CHARACTERISTICS** ( $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )<sup>a</sup>

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$f_{ref}$	Input Frequency	0		350	MHz	
$f_{MAX}$	Maximum Output Frequency	0		350	MHz	
$V_{PP}$	Peak-to-peak input voltage	PCLK	400	1000	mV	LVPECL
$V_{CMR}^b$	Common Mode Range	PCLK	1.2	$V_{CC}-0.8$	V	LVPECL
$t_{p, REF}$	Reference Input Pulse Width	1.4			ns	
$t_r, t_f$	CCLK Input Rise/Fall Time			1.0 <sup>c</sup>	ns	0.8 to 2.0V
$t_{PLH/HL}$	Propagation delay	PCLK to any Q	1.5	4.2	ns	
$t_{PLH/HL}$		CCLK to any Q	1.7	4.4	ns	
$t_{PLZ, HZ}$	Output Disable Time			11	ns	
$t_{PZL, LZ}$	Output Enable Time			11	ns	
$t_S$	Setup time	CCLK to CLK_STOP	0.0		ns	
		PCLK to CLK_STOP	0.0		ns	
$t_H$	Hold time	CCLK to CLK_STOP	1.0		ns	
		PCLK to CLK_STOP	1.5		ns	
$t_{sk(O)}$	Output-to-output Skew			150	ps	
$t_{sk(PP)}$	Device-to-device Skew	PCLK or CCLK to any Q		2.7	ns	
$t_{SK(p)}$	Output pulse skew <sup>d</sup>	Using CCLK		200	ps	
		Using PCLK		300	ps	
$DC_Q$	Output Duty Cycle	$f_Q < 350$ MHz and using CCLK	45	50	%	$DC_{REF} = 50\%$
		$f_Q < 200$ MHz and using PCLK	45	50	%	
$t_r, t_f$	Output Rise/Fall Time		0.1	1.0	ns	0.6 to 1.8V

- a. AC characteristics apply for parallel output termination of  $50\Omega$  to  $V_{TT}$ .
- b.  $V_{CMR}$  (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the  $V_{CMR}$  range and the input swing lies within the  $V_{PP}$  (AC) specification. Violation of  $V_{CMR}$  or  $V_{PP}$  impacts  $t_{PLH/HL}$  and  $t_{SK(PP)}$ .
- c. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- d. Output pulse skew is the absolute difference of the propagation delay times:  $|t_{pLH} - t_{pHL}|$ .

APPLICATIONS INFORMATION

Figure 3. Output Clock Stop (CLK\_STOP) Timing Diagram



Driving Transmission Lines

The MPC9448 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 17Ω (V<sub>CC</sub>=3.3V), the outputs can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Motorola application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V<sub>CC</sub>+2.

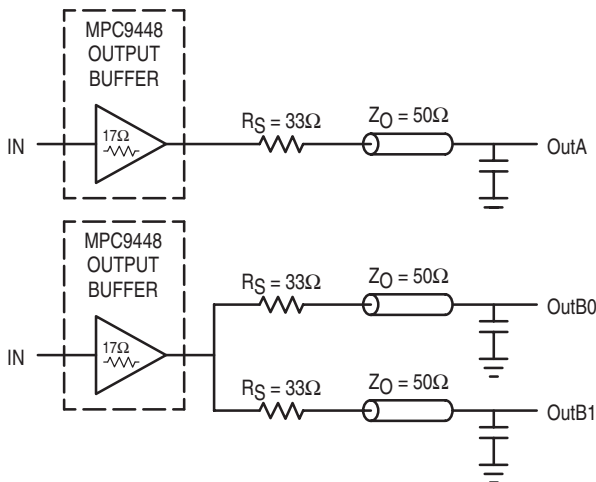


Figure 4. Single versus Dual Transmission Lines

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9448 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 4 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9448 clock driver is effectively doubled due to its capability to drive multiple lines at V<sub>CC</sub>=3.3V.

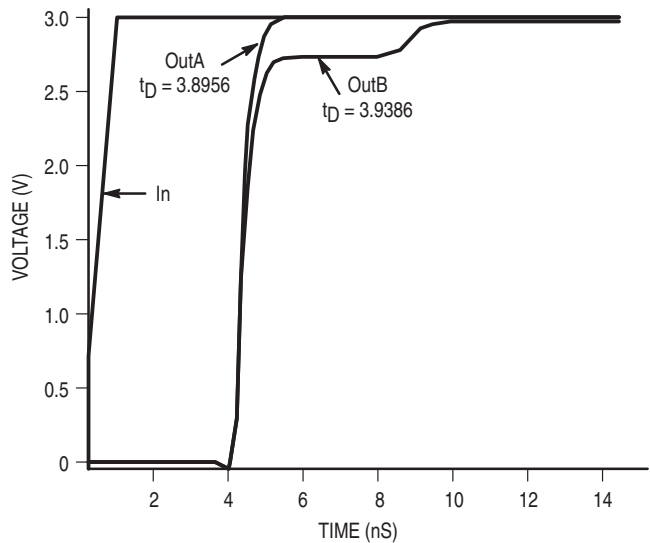


Figure 5. Single versus Dual Line Termination Waveforms

The waveform plots in Figure 5 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9448 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9448. The output waveform in Figure 5 “Single versus Dual Line Termination Waveforms” shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 33Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0) )$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_S = 33\Omega \parallel 33\Omega$$

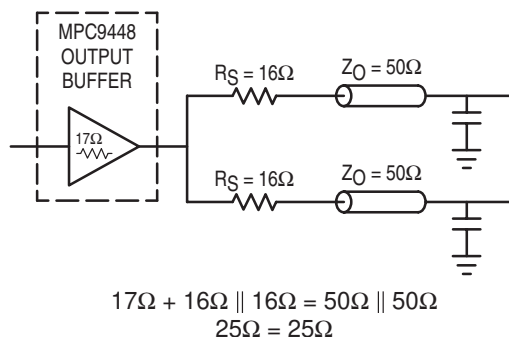
$$R_0 = 17\Omega$$

$$V_L = 3.0 ( 25 \div (16.5 + 17 + 25) )$$

$$= 1.28V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



**Figure 6. Optimized Dual Line Termination**

### Power Consumption of the MPC9448 and Thermal Management

The MPC9448 AC specification is guaranteed for the entire operating frequency range up to 350 MHz. The MPC9448 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC9448 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

$$P_{TOT} = \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_M C_L \right) \right] \cdot V_{CC} \quad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_M C_L \right) \right] + \sum_P \left[ DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \quad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \quad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[ \frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \quad \text{Equation 4}$$

**Table 9. Die junction temperature and MTBF**

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC9448 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC9448 is represented in equation 1.

Where  $I_{CCQ}$  is the static current consumption of the MPC9448,  $C_{PD}$  is the power dissipation capacitance per output,  $(M)\Sigma C_L$  represents the external capacitive output load,  $N$  is the number of active outputs ( $N$  is always 12 in case of the MPC9448). The MPC9448 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore,  $\Sigma C_L$  is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2,  $P$  stands for the number of outputs with a parallel or thevenin termination,  $V_{OL}$ ,  $I_{OL}$ ,  $V_{OH}$  and  $I_{OH}$  are a function of the output termination technique and  $DC_Q$  is the clock signal duty cycle. If transmission lines are used  $\Sigma C_L$  is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature  $T_J$  as a function of the power consumption.

Where  $R_{thja}$  is the thermal impedance of the package (junction to ambient) and  $T_A$  is the ambient temperature. According to Table 9, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC9448 in a series terminated transmission line system, equation 4.

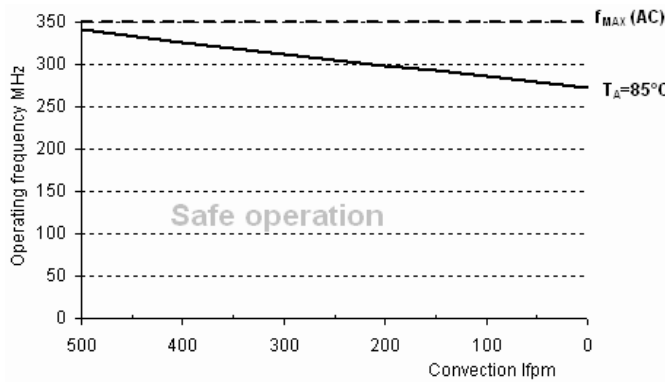


$T_{J,MAX}$  should be selected according to the MTBF system requirements and Table 9.  $R_{thja}$  can be derived from Table 10. The  $R_{thja}$  represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

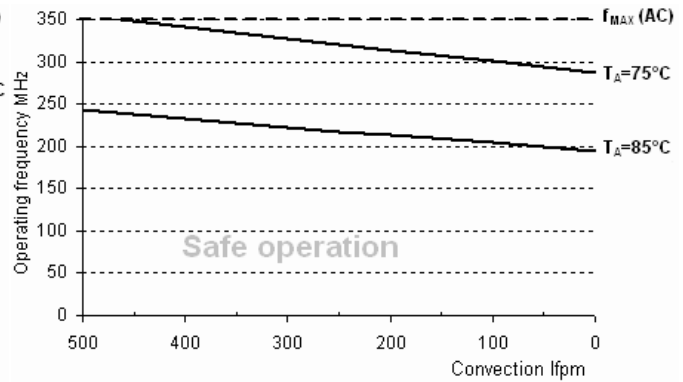
**Table 10. Thermal package impedance of the 32LQFP**

Convection, LFPM	$R_{thja}$ (1P2S board), °C/W	$R_{thja}$ (2P2S board), °C/W
Still air	86	61
100 lfpm	76	56
200 lfpm	71	54
300 lfpm	68	53
400 lfpm	66	52
500 lfpm	60	49

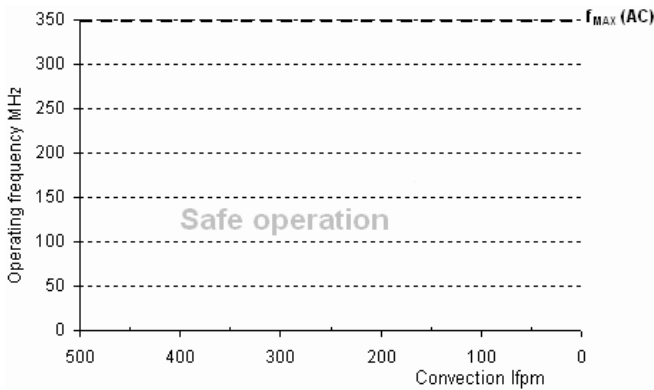
If the calculated maximum frequency is below 350 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC9448. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.



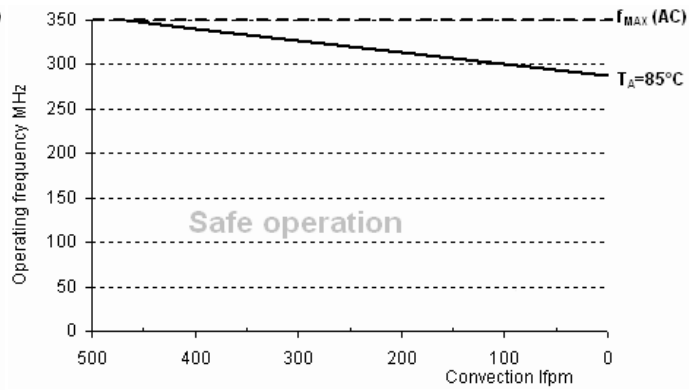
**Figure 7. Maximum MPC9448 frequency,  $V_{CC} = 3.3V$ , MTBF 9.1 years, driving series terminated transmission lines, 2s2p board**



**Figure 8. Maximum MPC9448 frequency,  $V_{CC} = 3.3V$ , MTBF 9.1 years, 4 pF load per line, 2s2p board**



**Figure 9. No maximum frequency limitation for  $V_{CC} = 3.3V$ , MTBF 4 years, driving series terminated transmission lines, 2s2p board**



**Figure 10. Maximum MPC9448 frequency,  $V_{CC} = 3.3V$ , MTBF 4 years, 4 pF load per line, 2s2p board**

The Following Figures Illustrate the Measurement Reference for the MPC9448 Clock Driver Circuit

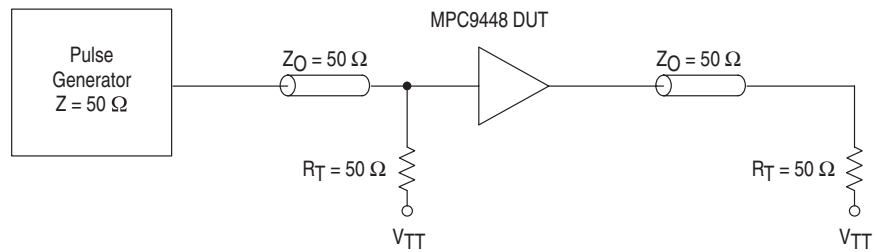


Figure 11. CCLK MPC9448 AC Test Reference for  $V_{CC} = 3.3V$  and  $V_{CC} = 2.5V$

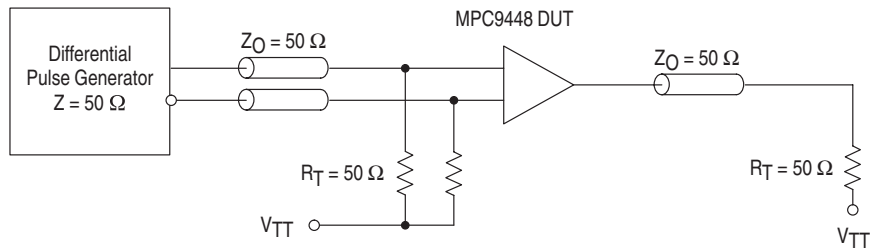


Figure 12. PCLK MPC9448 AC Test Reference

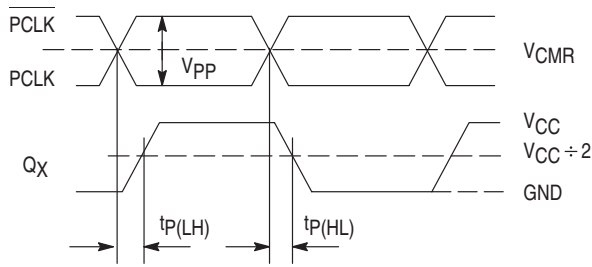


Figure 13. Propagation Delay (tpD) Test Reference

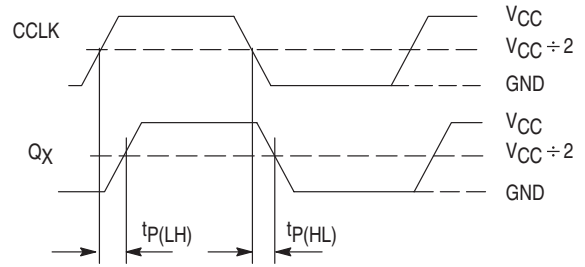
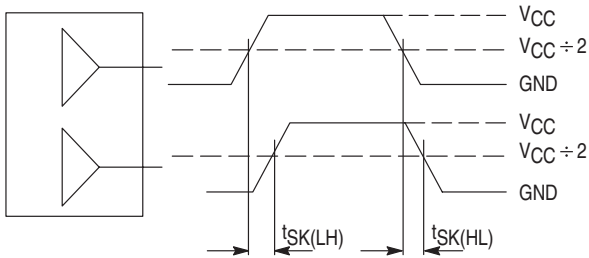
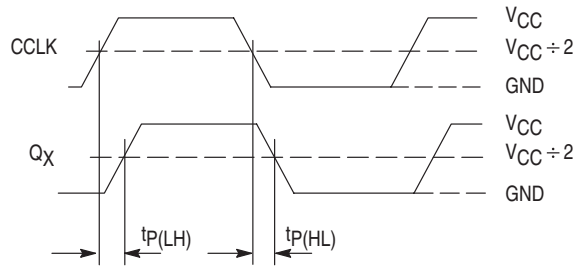


Figure 14. Propagation Delay (tpD) Test Reference



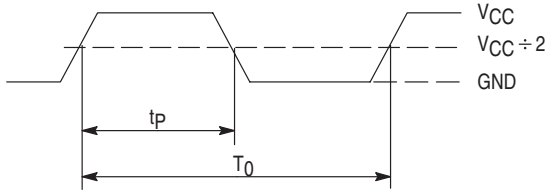
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-Output Skew tSK(LH, HL)



$$t_{SK}(P) = |t_{PLH} - t_{PHL}|$$

Figure 16. Output Pulse Skew (tSK(P)) Test Reference



$$DC = (tp \div T_0 \times 100\%)$$

The time from the output controlled edge to the non-controlled edge, divided by the time between output controlled edges, expressed as a percentage

Figure 17. Output Duty Cycle (DC)

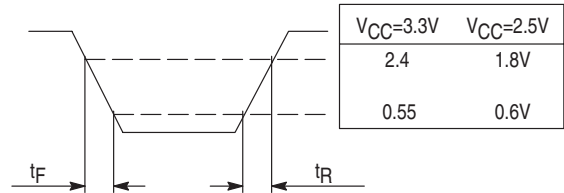
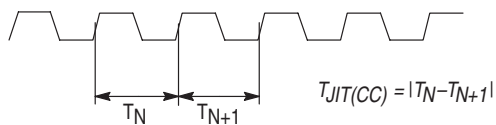


Figure 18. Output Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 19. Cycle-to-Cycle Jitter

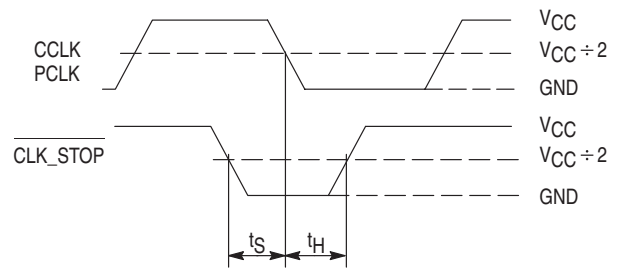
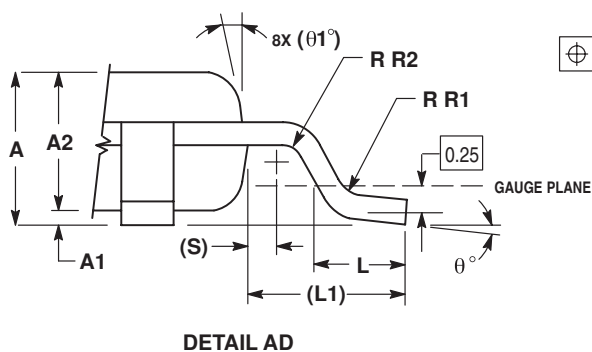
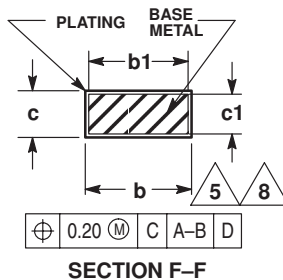
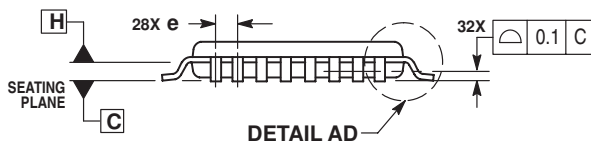
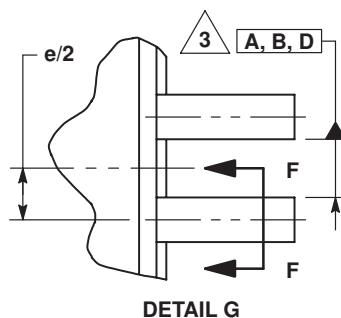
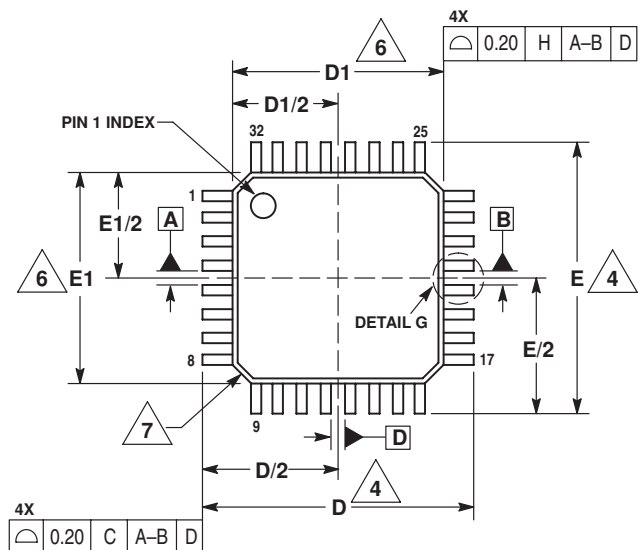


Figure 20. Setup and Hold Time (tS, tH) Test Reference

OUTLINE DIMENSIONS

FA SUFFIX  
LQFP PACKAGE  
CASE 873A-03  
ISSUE B



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.

MILLIMETERS		
DIM	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
θ	0°	7°
θ1	12° REF	
R1	0.08	0.20
R2	0.08	—
S	0.20 REF	

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