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Datasheet
PolarFire
Preliminary



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see [System Services \(see page 59\)](#).
- The Non-Volatile Characteristics section was updated. For more information, see [Non-Volatile Characteristics \(see page 51\)](#).
- The Fabric Macros section was updated. For more information, see [Fabric Macros \(see page 60\)](#).
- The Transceiver Switching Characteristics section was updated. For more information, see [Transceiver Switching Characteristics \(see page 42\)](#).

1.2 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

1.3 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see [HSIO Maximum Input Buffer Speed](#) and [HSIO Maximum Output Buffer Speed](#).
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see [I/O Standards Specifications](#).
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see [Non-Volatile Characteristics](#).
- A note was added defining power down conditions for programming recovery conditions. For more information, see [Power-Supply Ramp Times](#).

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Overview

This datasheet describes PolarFire® FPGA device characteristics with industrial temperature range (–40 °C to 100 °C T_J) and extended commercial temperature range (0 °C to 100 °C T_J). The devices are provided with a standard speed grade (STD) and a –1 speed grade with higher performance. The FPGA core supply V_{DD} can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply V_{DDA} can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the Libero project.

3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the [PolarFire Power Estimator Spreadsheet](#).

- [PO0137](#): PolarFire FPGA Product Overview
- [ER0217](#): PolarFire FPGA Pre-Production Device Errata
- [UG0722](#): PolarFire FPGA Packaging and Pin Descriptions Users Guide
- [UG0726](#): PolarFire FPGA Board Design User Guide
- [UG0686](#): PolarFire FPGA User I/O User Guide
- [UG0680](#): PolarFire FPGA Fabric User Guide
- [UG0714](#): PolarFire FPGA Programming User Guide
- [UG0684](#): PolarFire FPGA Clocking Resources User Guide
- [UG0687](#): PolarFire FPGA 1G Ethernet Solutions User Guide
- [UG0727](#): PolarFire FPGA 10G Ethernet Solutions User Guide
- [UG0748](#): PolarFire FPGA Low Power User Guide
- [UG0676](#): PolarFire FPGA DDR Memory Controller User Guide
- [UG0743](#): PolarFire FPGA Debugging User Guide
- [UG0725](#): PolarFire FPGA Device Power-Up and Resets User Guide
- [UG0677](#): PolarFire FPGA Transceiver User Guide
- [UG0685](#): PolarFire FPGA PCI Express User Guide
- [UG0753](#): PolarFire FPGA Security User Guide
- [UG0752](#): PolarFire FPGA Power Estimator User Guide

4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

5 Silicon Status

There are three silicon status levels:

- **Advanced**—initial estimated information based on simulations
- **Preliminary**—information based on simulation and/or initial characterization
- **Production**—final production silicon data

The following table shows the status of the PolarFire FPGA device.

Table 2 • PolarFire FPGA Silicon Status

Device	Silicon Status
MPF100T, TL, TS, TLS	Preliminary
MPF200T, TL, TS, TLS	Preliminary
MPF300T, TL, TS, TLS	Preliminary
MPF500T, TL, TS, TLS	Preliminary

6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	V _{DD}	-0.5	1.13	V
Transceiver Tx and Rx lanes supply	V _{DDA}	-0.5	1.13	V
Programming and HSIO receiver supply	V _{DD18}	-0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	V _{DD25}	-0.5	2.7	V
Transceiver PLL high-voltage supply	V _{DDA25}	-0.5	2.7	V
Transceiver reference clock supply	V _{DD_XCVR_CLK}	-0.5	3.6	V
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	-0.5	3.6	V
HSIO DC I/O supply ²	V _{DDIx}	-0.5	2.0	V
GPIO DC I/O supply ²	V _{DDIx}	-0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	V _{DDI3}	-0.5	3.6	V
GPIO auxiliary power supply for I/O bank x ²	V _{DDAUXx}	-0.5	3.6	V
Maximum DC input voltage on GPIO	V _{IN}	-0.5	3.8	V
Maximum DC input voltage on HSIO	V _{IN}	-0.5	2.2	V
Transceiver Receiver absolute input voltage	Transceiver V _{IN}	-0.5	1.26	V
Transceiver Reference clock absolute input voltage	Transceiver REFCLK V _{IN}	-0.5	3.6	V
Storage temperature (ambient) ¹	T _{STG}	-65	150	°C
Junction temperature ¹	T _J	-55	135	°C
Maximum soldering temperature RoHS	T _{SOLROHS}		260	°C
Maximum soldering temperature leaded	T _{SOLPB}		220	°C

1. See [FPGA Programming Cycles vs Retention Characteristics](#) for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
2. The power supplies for a given I/O bank x are shown as V_{DDIx} and V_{DDAUXx}.

6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core supply at 1.0 V mode ¹	V _{DD}	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode ¹	V _{DD}	1.02	1.05	1.08	V
Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less) ¹	V _{DDA}	0.97	1.00	1.03	V

Parameter	Symbol	Min	Typ	Max	Unit
Transceiver TX and RX lanes supply at 1.05 V mode (when any lane rate is greater than 10.3125 Gbps) ¹	V _{DDA}	1.02	1.05	1.08	V
Programming and HSIO receiver supply	V _{DD18}	1.71	1.80	1.89	V
FPGA core and FPGA PLL high-voltage supply	V _{DD25}	2.425	2.50	2.575	V
Transceiver PLL high-voltage supply	V _{DDA25}	2.425	2.50	2.575	V
Transceiver reference clock supply –3.3 V nominal	V _{DD_XCVR_CLK}	3.135	3.3	3.465	V
Transceiver reference clock supply –2.5 V nominal	V _{DD_XCVR_CLK}	2.375	2.5	2.625	V
Global V _{REF} for transceiver reference clocks ³	XCVR _{VREF}	Ground		V _{DD_XCVR_CLK}	V
HSIO DC I/O supply. Allowed nominal options: 1.2 V, 1.35 V, 1.5 V, and 1.8 V ⁴	V _{DDix}	1.14	Various	1.89	V
GPIO DC I/O supply. Allowed nominal options: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V ^{2,4}	V _{DDix}	1.14	Various	3.465	V
Dedicated I/O DC supply for JTAG and SPI (GPIO Bank 3). Allowed nominal options: 1.8 V, 2.5 V, and 3.3 V	V _{DDI3}	1.71	Various	3.465	V
GPIO auxiliary supply for I/O bank x with V _{DDix} = 3.3 V nominal ^{2,4}	V _{DDAUXx}	3.135	3.3	3.465	V
GPIO auxiliary supply for I/O bank x with V _{DDix} = 2.5 V nominal or lower ^{2,4}	V _{DDAUXx}	2.375	2.5	2.625	V
Extended commercial temperature range	T _J	0		100	°C
Industrial temperature range	T _J	–40		100	°C
Extended commercial programming temperature range	T _{PRG}	0		100	°C
Industrial programming temperature range	T _{PRG}	–40		100	°C

1. V_{DD} and V_{DDA} can independently operate at 1.0 V or 1.05 V nominal. These supplies are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank number, if V_{DDix} is 2.5 V nominal or 3.3 V nominal, V_{DDAUXx} must be connected to the V_{DDix} supply for that bank. If V_{DDix} for a given GPIO bank is <2.5 V nominal, V_{DDAUXx} per I/O bank must be powered at 2.5 V nominal.
3. XCVR_{VREF} globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near V_{DD_XCVR_CLK}/2 V but is allowed in the specified range.
4. The power supplies for a given I/O bank x are shown as VDDix and VDDAUXx.

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance ¹	C _{IN} (dedicated GPIO)		5.6	pf	
	C _{IN} (GPIO)		5.6	pf	
	C _{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I _L (GPIO)		10	μA	I/O disabled, high – Z
	I _L (HSIO)		10	μA	I/O disabled, high – Z
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}	T _{RISE}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}	T _{FALL}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Pad pull-up when V _{IN} = 0 ⁵	I _{PU}	137	220	μA	V _{DDIX} = 3.3 V
Pad pull-up when V _{IN} = 0 ⁵		102	166	μA	V _{DDIX} = 2.5 V
Pad pull-up when V _{IN} = 0		68	115	μA	V _{DDIX} = 1.8 V
Pad pull-up when V _{IN} = 0		51	88	μA	V _{DDIX} = 1.5 V
Pad pull-up when V _{IN} = 0 ⁶		29	73	μA	V _{DDIX} = 1.35 V
Pad pull-up when V _{IN} = 0		16	46	μA	V _{DDIX} = 1.2 V
Pad pull-down when V _{IN} = 3.3 V ⁵	I _{PD}	65	187	μA	V _{DDIX} = 3.3 V
Pad pull-down when V _{IN} = 2.5 V ⁵		63	160	μA	V _{DDIX} = 2.5 V
Pad pull-down when V _{IN} = 1.8 V		60	117	μA	V _{DDIX} = 1.8 V
Pad pull-down when V _{IN} = 1.5 V		57	95	μA	V _{DDIX} = 1.5 V
Pad pull-down when V _{IN} = 1.35 V		52	86	μA	V _{DDIX} = 1.35 V
Pad pull-down when V _{IN} = 1.2 V		47	79	μA	V _{DDIX} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty-cycle.

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for HSIO.

Table 6 • Maximum Overshoot During Transitions for HSIO

AC (V_{IN}) Overshoot Duration as % at $T_J = 100\text{ }^\circ\text{C}$	Condition (V)
100	1.8
100	1.85
100	1.9
100	1.95
100	2
100	2.05
100	2.1
100	2.15
100	2.2
90	2.25
30	2.3
7.5	2.35
1.9	2.4

Note: Overshoot level is for VDDI at 1.8 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for HSIO.

Table 7 • Maximum Undershoot During Transitions for HSIO

AC (V_{IN}) Undershoot Duration as % at $T_J = 100\text{ }^\circ\text{C}$	Condition (V)
100	-0.05
100	-0.1
100	-0.15
100	-0.2
100	-0.25
100	-0.3
100	-0.35
100	-0.4
44	-0.45
14	-0.5
4.8	-0.55
1.6	-0.6

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for GPIO.

Table 8 • Maximum Overshoot During Transitions for GPIO

AC (V _{IN}) Overshoot Duration as % at T _J = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

Note: Overshoot level is for V_{DDI} at 3.3 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for GPIO.

Table 9 • Maximum Undershoot During Transitions for GPIO

AC (V _{IN}) Undershoot Duration as % at T _J = 100 °C	Condition (V)
100	-0.5
100	-0.55
100	-0.6
100	-0.65
100	-0.7
100	-0.75
100	-0.8
100	-0.85
100	-0.9
100	-0.95
100	-1
100	-1.05
100	-1.1
100	-1.15
100	-1.2
69	-1.25
45	-1.3

6.2.2.1 Power-Supply Ramp Times

The following table shows the allowable power-up ramp times. Times shown correspond to the ramp of the supply from 0 V to the minimum recommended voltage as specified in the section [Recommended Operating Conditions](#) (see page 6). All supplies must rise and fall monotonically.

Table 10 • Power-Supply Ramp Times

Parameter	Symbol	Min	Max	Unit
FPGA core supply	V _{DD}	0.2	50	ms
Transceiver core supply	V _{DDA}	0.2	50	ms
Must connect to 1.8 V supply	V _{DD18}	0.2	50	ms
Must connect to 2.5 V supply	V _{DD25}	0.2	50	ms
Must connect to 2.5 V supply	V _{DDA25}	0.2	50	ms
HSIO bank I/O power supplies	V _{DDI} [0,1,6,7]	0.2	50	ms
GPIO bank I/O power supplies	V _{DDI} [2,4,5]	0.2	50	ms
Bank 3 dedicated I/O buffers (GPIO)	V _{DDI3}	0.2	50	ms
GPIO bank auxiliary power supplies	V _{DDAUX} [2,4,5]	0.2	50	ms
Transceiver reference clock supply	V _{DD_XCVR_CLK}	0.2	50	ms
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	0.2	50	ms

Note: For proper operation of programming recovery mode, if a VDD supply brownout occurs during programming, a minimum supply ramp down time for only the VDD supply is recommended to be 10 ms or longer by using a programmable regulator or on-board capacitors.

6.2.2.2 Hot Socketing

The following table lists the hot-socketing DC characteristics over recommended operating conditions.

Table 11 • Hot Socketing DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Current per transceiver Rx input pin (P or N single-ended) ^{1, 2}	XCVR _{RX_HS}			±4	mA	V _{DDA} = 0 V
Current per transceiver Tx output pin (P or N single-ended) ³	XCVR _{TX_HS}			±10	mA	V _{DDA} = 0 V
Current per transceiver reference clock input pin (P or N single-ended) ⁴	XCVR _{REF_HS}			±1	mA	V _{DD_XCVR_CLK} = 0 V
Current per GPIO pin (P or N single-ended) ⁵	I _{GPIO_HS}			±1	mA	V _{DDIX} = 0 V
Current per HSIO pin (P or N single-ended)						Hot socketing is not supported in HSIO.

- Assumes that the device is powered-down, all supplies are grounded, AC-coupled interface, and input pin pairs are driven by a CML driver at the maximum amplitude (1 V pk–pk) that is toggling at any rate with PRBS7 data.
- Each P and N transceiver input has less than the specified maximum input current.
- Each P and N transceiver output is connected to a 40 Ω resistor (50 Ω CML termination – 20% tolerance) to the maximum allowed output voltage (V_{DDAmax} + 0.3 V = 1.4 V) through an AC-coupling capacitor with all PolarFire device supplies grounded. This shows the current for a worst-case DC coupled interface. As an AC-coupled interface, the output signal will settle at ground and no hot socket current will be seen.
- V_{DD_XCVR_CLK} is powered down and the device is driven to –0.3 V < V_{IN} < V_{DD_XCVR_CLK}.
- V_{DDIX} is powered down and the device is driven to –0.3 V < V_{IN} < GPIO V_{DDI}max.

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
PCI	3.15	3.3	3.45	-0.3	0.3 x V _{DDI}	0.5 x V _{DDI}	3.45
LVTTTL	3.15	3.3	3.45	-0.3	0.8	2	3.45
LVC MOS33	3.15	3.3	3.45	-0.3	0.8	2	3.45
LVC MOS25	2.375	2.5	2.625	-0.3	0.7	1.7	2.625
LVC MOS18	1.71	1.8	1.89	-0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.89
LVC MOS15	1.425	1.5	1.575	-0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.575
LVC MOS12	1.14	1.2	1.26	-0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.26
SSTL25I ²	2.375	2.5	2.625	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	2.625
SSTL25II ²	2.375	2.5	2.625	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	2.625
SSTL18I ²	1.71	1.8	1.89	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	1.89
SSTL18II ²	1.71	1.8	1.89	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
SSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL18II	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.

2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

Table 13 • DC Output Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
PCI ¹	3.15	3.3	3.45		0.1 x V _{DDI}	0.9 x V _{DDI}		1.5	0.5
LVTTTL	3.15	3.3	3.45		0.4	2.4			
LVC MOS33	3.15	3.3	3.45		0.4	V _{DDI} – 0.4			
LVC MOS25	2.375	2.5	2.625		0.4	V _{DDI} – 0.4			
LVC MOS18	1.71	1.8	1.89		0.45	V _{DDI} – 0.45			
LVC MOS15	1.425	1.5	1.575		0.25 x V _{DDI}	0.75 x V _{DDI}			
LVC MOS12	1.14	1.2	1.26		0.25 x V _{DDI}	0.75 x V _{DDI}			
SSTL25I ³	2.375	2.5	2.625		V _{TT} – 0.608	V _{TT} + 0.608		8.1	8.1
SSTL25II ³	2.375	2.5	2.625		V _{TT} – 0.810	V _{TT} + 0.810		16.2	16.2
SSTL18I ³	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603		6.7	6.7
SSTL18II ³	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603		13.4	13.4
SSTL15I ⁴	1.425	1.5	1.575		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL15II ⁴	1.425	1.5	1.575		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34
SSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34
HSTL15I	1.425	1.5	1.575		0.4	V _{DDI} – 0.4		8	8
HSTL15II	1.425	1.5	1.575		0.4	V _{DDI} – 0.4		16	16

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
HSTL135I ⁴	1.283	1.35	1.418	0.2	0.8	x	x	V _{OL} /50	(V _{DDI} - V _{OH})/50
HSTL135II ⁴	1.283	1.35	1.418	0.2	0.8	x	x	V _{OL} /25	(V _{DDI} - V _{OH})/25
HSTL12I ⁴	1.14	1.2	1.26	0.1	0.9	x	x	V _{OL} /50	(V _{DDI} - V _{OH})/50
HSTL12II ⁴	1.14	1.2	1.26	0.1	0.9	x	x	V _{OL} /25	(V _{DDI} - V _{OH})/25
HSUL18I ⁴	1.71	1.8	1.89	0.1	0.9	x	x	V _{OL} /55	(V _{DDI} - V _{OH})/55
HSUL18II ⁴	1.71	1.8	1.89	0.1	0.9	x	x	V _{OL} /25	(V _{DDI} - V _{OH})/25
HSUL12I ⁴	1.14	1.2	1.26	0.1	0.9	x	x	V _{OL} /40	(V _{DDI} - V _{OH})/40
POD12I ^{4,5}	1.14	1.2	1.26	0.5	x	x	x	V _{OL} /48	(V _{DDI} - V _{OH})/48
POD12II ^{4,5}	1.14	1.2	1.26	0.5	x	x	x	V _{OL} /34	(V _{DDI} - V _{OH})/34

1. Drive strengths per PCI specification V/I curves.
2. Refer to [UG0686: PolarFire FPGA User I/O User Guide](#) for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).
5. VOH_MAX based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
 - a. HSIO lane: 120 mA per 12 IO buffers.
 - b. GPIO lane: 160 mA per 12 IO buffers.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

Table 14 • Differential DC Input Levels

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 ⁴	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS18	HSIO	Low	0.05	0.4	0.8	0.1	0.35	0.6
		Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
LCMDS33	GPIO	Low	0.05	0.4	0.8	0.1	0.35	0.6
		Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
LCMDS18	HSIO	Low	0.05	0.4	0.8	0.1	0.35	0.6
		Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
LCMDS25	GPIO	Low	0.05	0.4	0.8	0.1	0.35	0.6
		Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
RSDS33	GPIO	Low	0.05	0.4	0.8	0.1	0.2	0.6
		Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
RSDS25	GPIO	Low	0.05	0.4	0.8	0.1	0.2	0.6
		Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
RSDS18 ⁵	HSIO	Low	0.05	0.4	0.8	0.1	0.2	0.6
		Mid (default)	0.6	1.25	1.65	0.1	0.2	0.6
MINILVDS33	GPIO	Low	0.05	0.4	0.8	0.1	0.3	0.6
		Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
MINILVDS25	GPIO	Low	0.05	0.4	0.8	0.1	0.3	0.6
		Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
MINILVDS18 ⁵	HSIO	Low	0.05	0.4	0.8	0.1	0.3	0.6
		Mid (default)	0.6	1.25	1.65	0.1	0.3	0.6
SUBLVDS33	GPIO	Low	0.05	0.4	0.8	0.1	0.15	0.3
		Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
SUBLVDS25	GPIO	Low	0.05	0.4	0.8	0.1	0.15	0.3
		Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
SUBLVDS18 ⁵	HSIO	Low	0.05	0.4	0.8	0.1	0.15	0.3
		Mid (default)	0.6	0.9	1.65	0.1	0.15	0.3
PPDS33	GPIO	Low	0.05	0.4	0.8	0.1	0.2	0.6
		Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
PPDS25	GPIO	Low	0.05	0.4	0.8	0.1	0.2	0.6
		Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
PPDS18 ⁵	HSIO	Low	0.05	0.4	0.8	0.1	0.2	0.6
		Mid (default)	0.6	0.8	1.65	0.1	0.2	0.6
SLVS33 ⁶	GPIO	Low	0.05	0.2	0.8	0.1	0.2	0.3
		Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
SLVS25 ⁶	GPIO	Low	0.05	0.2	0.8	0.1	0.2	0.3
		Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
SLVS18 ⁵	HSIO	Low	0.05	0.4	0.8	0.1	0.2	0.3
		Mid (default)	0.6	1.00	1.65	0.1	0.2	0.3
HCSL33 ⁶	GPIO	Low	0.05	0.35	0.8	0.1	0.55	1.1
		Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
HCSL25 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1
HCSL18 ⁵	HSIO	Mid (default)	0.6	1.0	1.65	0.1	0.55	1.1
		Low	0.05	0.4	0.8	0.1	0.55	1.1
BUSLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.1	V _{DDIn}
		Low	0.05	0.4	0.8	0.05	0.1	V _{DDIn}
MLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.35	2.4
		Low	0.05	0.4	0.8	0.05	0.35	2.4
LVPECL33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
LVPECLE33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
MIPI25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.2	0.3
		Low	0.05	0.2	0.8	0.05	0.2	0.3

- V_{ICM} is the input common mode.
- V_{ID} is the input differential voltage.
- V_{ICM} rules are as follows:
 - V_{ICM} must be less than V_{DDI} – 0.4 V;
 - V_{ICM} + V_{ID}/2 must be <V_{DDI} + 0.4 V;
 - V_{ICM} – V_{ID}/2 must be >V_{SS} – 0.3 V;
 - Any differential input with V_{ICM} ≤ 0.6 V requires the low common mode setting in Libero (VICM_RANGE=LOW).
- V_{DDI} = 1.8 V, V_{DDAUX} = 2.5 V.
- HSIO receiver only.
- GPIO receiver only.

Table 15 • Differential DC Output Levels

I/O Standard	Bank Type	V _{OCM} ¹ Min (V)	V _{OCM} Typ (V)	V _{OCM} Max (V)	V _{OD} ² Min (V)	V _{OD} ² Typ (V)	V _{OD} ² Max (V)
LVDS33	GPIO		1.2		0.25	0.35	0.45
LVDS25	GPIO		1.2		0.25	0.35	0.45
LCMDS33	GPIO		0.6		0.25	0.35	0.45
LCMDS25	GPIO		0.6		0.25	0.35	0.45
RSDS33	GPIO		1.2		0.17	0.2	0.23
RSDS25	GPIO		1.2		0.17	0.2	0.23
MINILVDS33	GPIO		1.2		0.3	0.4	0.6
MINILVDS25	GPIO		1.2		0.3	0.4	0.6
SUBLVDS33	GPIO		0.9		0.1	0.15	0.3
SUBLVDS25	GPIO		0.9		0.1	0.15	0.3
PPDS33	GPIO		0.8		0.17	0.2	0.23
PPDS25	GPIO		0.8		0.17	0.2	0.23
SLVSE15 ³	GPIO, HSIO		0.2		0.12	0.135	0.15
BUSLVDSE25 ³	GPIO		1.25		0.24	0.262	0.272

I/O Standard	Bank Type	V _{ocm} ¹ Min (V)	V _{ocm} Typ (V)	V _{ocm} Max (V)	V _{od} ² Min (V)	V _{od} ² Typ (V)	V _{od} ² Max (V)
MLVDSE25 ³	GPIO		1.25		0.396	0.442	0.453
LVPECLE33 ³	GPIO		1.65		0.664	0.722	0.755
MIPIE25 ³	GPIO		0.25		0.1	0.22	0.3

1. V_{ocm} is the output common mode voltage.
2. V_{od} is the output differential voltage.
3. Emulated output only.

6.3.3 Complementary Differential DC Input and Output Levels

The following tables list the complementary differential DC I/O levels.

Table 16 • Complementary Differential DC Input Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Max (V)
SSTL25I	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL25II	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
SSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
HSUL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
POD12I	1.14	1.2	1.26	0.787	0.840	0.895	0.1	
POD12II	1.14	1.2	1.26	0.787	0.840	0.895	0.1	

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
 - a. V_{ICM} must be less than V_{DDI} - 0.4V;
 - b. V_{ICM} + V_{ID}/2 must be < V_{DDI} + 0.4 V;
 - c. V_{ICM} - V_{ID}/2 must be > V_{SS} - 0.3 V.

Table 17 • Complementary Differential DC Output Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} ^{1,3} Min (V)	I _{OL} ² Min (mA)	I _{OH} ² Min (mA)
SSTL25I	2.375	2.5	2.625		V _{TT} – 0.608	V _{TT} + 0.608	8.1	8.1
SSTL25II	2.375	2.5	2.625		V _{TT} – 0.810	V _{TT} + 0.810	16.2	16.2
SSTL18I	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603	6.7	6.7
SSTL18II	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603	13.4	13.4
SSTL15I ⁴	1.425	1.5	1.575		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL15II ⁴	1.425	1.5	1.575		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /34	(V _{DDI} – V _{OH})/34
SSTL135I ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL135II ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /34	(V _{DDI} – V _{OH})/34
HSTL15I	1.425	1.5	1.575		0.4	V _{DDI} – 0.4	8	8
HSTL15II	1.425	1.5	1.575		0.4	V _{DDI} – 0.4	16	16
HSTL135I ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /50	(V _{DDI} – V _{OH})/50
HSTL135II ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /25	(V _{DDI} – V _{OH})/25
HSTL12I ⁴	1.14	1.2	1.26		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /50	(V _{DDI} – V _{OH})/50
HSUL18I ⁴	1.71	1.8	1.89		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /55	(V _{DDI} – V _{OH})/55
HSUL18II ⁴	1.71	1.8	1.89		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /25	(V _{DDI} – V _{OH})/25
HSUL12I ⁴	1.14	1.2	1.26		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /40	(V _{DDI} – V _{OH})/40
POD12I ^{3,4}	1.14	1.2	1.26		0.5 × V _{DDI}		V _{OL} /48	(V _{DDI} – V _{OH})/48
POD12II ^{3,4}	1.14	1.2	1.26		0.5 × V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34

- V_{OH} is the single-ended high-output voltage.
- The total DC sink/source current of all IOs within a lane is limited as follows:
 - HSIO lane: 120 mA per 12 IO buffers.
 - GPIO lane: 160 mA per 12 IO buffers
- V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
- I_{OL}/I_{OH} units for impedance standards in amps (not mA).

6.3.4 HSIO On-Die Termination

The following tables lists the on-die termination calibration accuracy specifications for HSIO bank.

Table 18 • Single-Ended Thevenin Termination (Internal Parallel Thevenin Termination)

Min (%)	Typ	Max (%)	Unit	Condition
–40	50	20	Ω	V _{DDI} = 1.8 V/1.5 V/1.35 V/1.2 V
–40	75	20	Ω	V _{DDI} = 1.8 V
–40	150	20	Ω	V _{DDI} = 1.8 V
–20	20	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	30	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	40	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	60	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	120	20	Ω	V _{DDI} = 1.5 V/1.35 V

Min (%)	Typ	Max (%)	Unit	Condition
-20	60	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	120	20	Ω	$V_{DDI} = 1.2\text{ V}$

Note: Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI} . For 50 Ω /75 Ω /150 Ω cases, nearest supported values of 40 Ω /60 Ω /120 Ω are used.

Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)

Min (%)	Typ	Max (%)	Unit	Condition
-20	34	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	40	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	48	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	60	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	80	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	120	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	240	20	Ω	$V_{DDI} = 1.2\text{ V}$

Note: Measured at 80% of V_{DDI} .

Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)

Min (%)	Typ	Max (%)	Unit	Condition
-20	120	20	Ω	$V_{DDI} = 1.8\text{ V}/1.5\text{ V}$
-20	240	20	Ω	$V_{DDI} = 1.8\text{ V}/1.5\text{ V}$
-20	120	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	240	20	Ω	$V_{DDI} = 1.2\text{ V}$

Note: Measured at 50% of V_{DDI} .

6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Differential termination ¹	Internal differential termination	-20	100	20	Ω	$V_{ICM} < 0.8\text{ V}$
		-20	100	40	Ω	$0.6\text{ V} < V_{ICM} < 1.65\text{ V}$
		-20	100	80	Ω	$1.4\text{ V} < V_{ICM}$
Single-ended thevenin termination ^{2,3}	Internal parallel thevenin termination	-40	50	20	Ω	$V_{DDI} = 1.8\text{ V}/1.5\text{ V}$
		-40	75	20	Ω	$V_{DDI} = 1.8\text{ V}$
		-40	150	20	Ω	$V_{DDI} = 1.8\text{ V}$
		-20	20	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	30	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	40	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	60	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	120	20	Ω	$V_{DDI} = 1.5\text{ V}$

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Single-ended termination to $V_{SS}^{4,5}$	Internal	-20	120	20	Ω	$V_{DDI} = 2.5\text{ V}/1.8\text{ V}/1.5\text{ V}/1.2\text{ V}$
	parallel termination to V_{SS}	-20	240	20	Ω	$V_{DDI} = 2.5\text{ V}/1.8\text{ V}/1.5\text{ V}/1.2\text{ V}$

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI} .
3. For 50 Ω /75 Ω /150 Ω cases, nearest supported values of 40 Ω /60 Ω /120 Ω are used.
4. Measured at 50% of V_{DDI} .
5. Supported terminations vary with the IO type regardless of V_{DDI} nominal voltage. Refer to Libero for available combinations.