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PL360

PL360 Datasheet

Description

The PL360 is a programmable modem for narrow-band Power Line Communication (PLC), able to run any PLC protocol in the frequency band below 500 kHz.

This device has been designed to comply with FCC, ARIB, KN60 and CENELEC EN50065 regulations matching requirements of Internet of Things and Smart Energy applications. It supports state-of-the-art narrow-band PLC standards such as ITU G.9903 (G3-PLC®), ITU G.9904 (PRIME) as well as any other narrowband PLC protocols, being at the same time a future-proof platform able to support the evolution of these standards.

The PL360 has been conceived to be driven by external Microchip host devices, thus providing an additional level of flexibility on the host side. The Microchip host device loads the proper PLC-protocol firmware before modem operation and controls the PL360 modem.

Features

- Programmable Narrow-Band Power Line Communication (PLC) Modem
- Integrated PLC Front End:
  - PGA with automatic gain control and ADC
  - DAC and transmission driver supports direct line driving or external Class-D amplifier driving
  - Digital transmission level control
  - Supports two independent transmission branches for the PLC signal
  - Up to 500 kHz PLC signal bandwidth
- Architecture
  - High performance architecture combining CPU, specific co-processors for digital signal processing and dedicated hardware accelerators for common narrow-band PLC tasks
  - Dedicated SRAM memories for code and data
- ARM® 32-bit Cortex®-M7 Core Managing PL360 System: Co-Processors, Hardware Accelerators and Peripherals
  - 216 MHz maximum frequency
  - 192 kB of SRAM for data and code
  - Bootloader allows loading plain programs or authenticated and encrypted programs
  - 12 multiplexed GPIOs
  - 1 SPI, 1 UART, 2 PWM
  - Serial wire debug port
  - Zero-Crossing Detection on the mains
- Cryptographic Engine and Secure Boot

  - AES 128, 192, 256 supported
  - Secure boot: supports AES-128 CMAC for authentication, AES-128 CBC for decryption
  - Fuse programming control for decryption and authentication 128-bit keys
- Clock Management
  - 24 MHz external crystal for system clock
- Power Management
  - 3.3 V external supply voltage for I/O, digital and analog
  - 1.25 V internal voltage regulator for the core
  - Optimized power modes for specific operation profiles, including Low Power mode
- Available in TQFP-48 and QFN-48 Packages
- -40ºC to +85ºC Temperature Range

Table of Contents

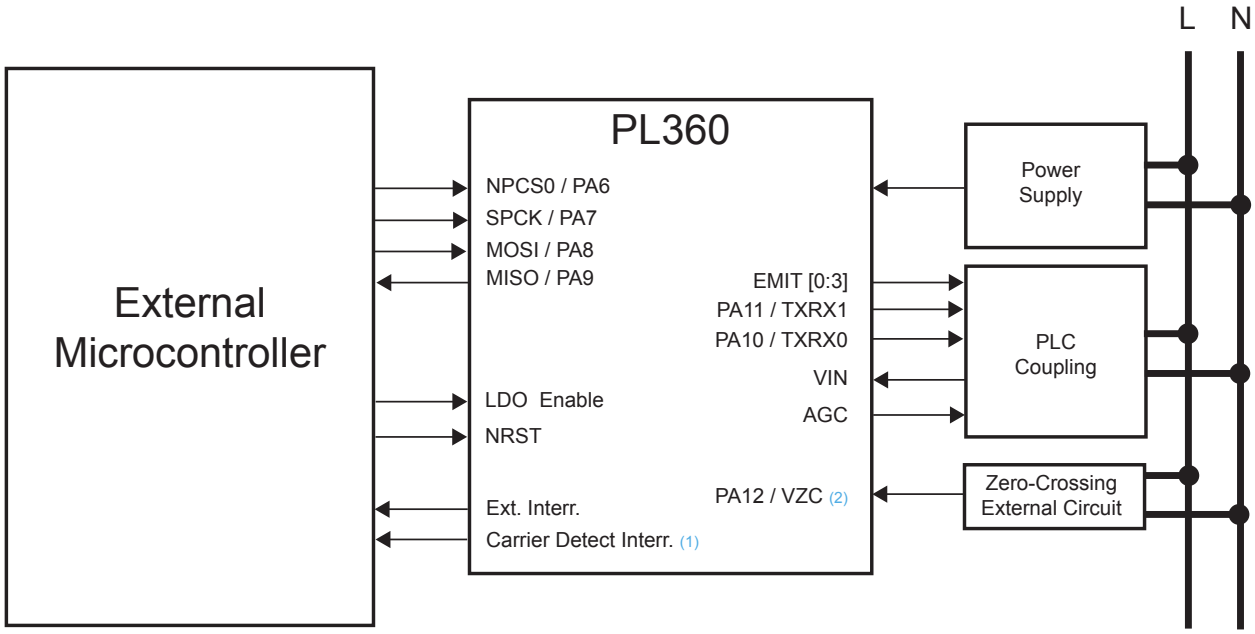
1. PL360 Application Block Diagram

PL360 transceiver has been conceived to be easily managed by an external microcontroller through a 4-line standard Serial Peripheral Interface (SPI). By means of the SPI, the external microcontroller can fully manage and control the PL360 by accessing the internal peripheral registers.

Two additional signals are used by the host to control the PL360: LDO enable and NRST.

Some GPIOs can be used as interrupt signals from the PL360 to the external microcontroller depending on the requirements of the protocol being used.

Figure 1-1. PL360 Application Example

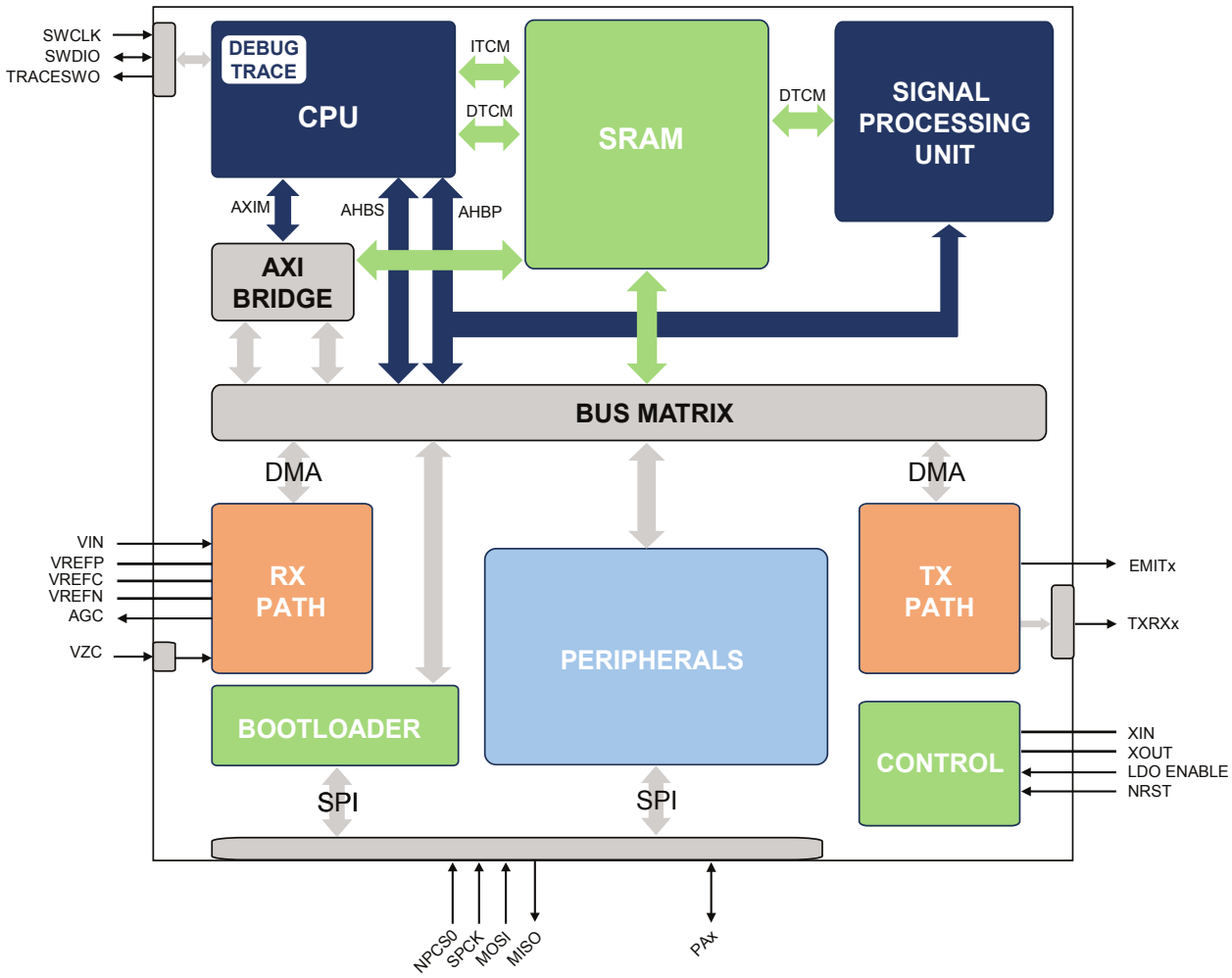


Notes:

1. Used by protocols requiring carrier detection signaling
2. Used by applications requiring phase detection

2. Block Diagram

Figure 2-1. PL360 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Power Supplies					
VDDIO	3.3V Digital supply. Digital power supply must be decoupled by external capacitors	Power			3.0V to 3.6V
VDDIN	3.3V Voltage Regulator Input	Power			3.0V to 3.6V
VDDIN_AN	3.3V Analog supply (ADC + PGA)	Power			3.0V to 3.6V
VDDCORE	Core power supply with internal connection to 1.25V voltage regulator output. Decoupling capacitors required	Power			1.25V
VDDPLL	1.25V Voltage Regulator Output. Connected to VDDCORE through a LP filter (Cut off frequency: <40 kHz)	Power			1.25V
GND	Digital Ground	Power			(1)
AGND	Analog Ground	Power			(1)
Clocks, Oscillators and PLLs					
XIN	Crystal Oscillator Input	Input		VDDIO	
XOUT	Crystal Oscillator Output	Output		VDDIO	
Reset/Test					
NRST	System Reset	Input	Low	VDDIO	
TST	Test Mode	Input	High	VDDIO	
LDO ENABLE	Enable Internal LDO regulator	Input			
Power Line Communications					
EMIT [0:3]	PLC Tri-state Transmission ports	Output		VDDIO	
VIN	PLC signal reception input	Input		VDDIN_AN	
AGC	Automatic Gain Control: • This digital tri-state output is managed by AGC hardware logic to drive external circuitry when input signal attenuation is needed	Output		VDDIO	(3)
VZC	Mains Zero-Cross Detection Signal: • This input detects the zero-crossing of the mains voltage	Input		VDDIO	External Protection Resistor (2) (3)
TXRX0	Analog Front-End Transmission/ Reception for TXDRV0	Output		VDDIO	

	• This digital output is used to modify external coupling behavior in Transmission/Reception				
TXRX1	Analog Front-End Transmission/ Reception for TXDRV1 • This digital output is used to modify external coupling behavior in Transmission/Reception. The suitable value depends on the external circuitry configuration. The polarity of this pin can be inverted by software	Output		VDDIO	
VREFP	Internal Reference “Plus” Voltage. Bypass to analog ground with an external decoupling capacitor. Connect an external decoupling capacitor between VREFP and VREFN.	Analog		VDDIN_AN	
VREFN	Internal Reference “Minus” Voltage. Bypass to analog ground with an external decoupling capacitor. Connect an external decoupling capacitor between VREFP and VREFN.	Analog		VDDIN_AN	
VREFC	Internal Reference Common-mode Voltage. Bypass to analog ground with an external decoupling capacitor.	Analog		VDDIN_AN	
General Purpose I/Os					
PA [0:11]	General Purpose Input / Output	I/O		VDDIO	(4)
PA [12]	General Purpose Input	Input		VDDIO	(4)
Serial Wire - Debug Port – SW-DP					
SWDIO	Serial Wire Input/Output	I/O		VDDIO	
SWCLK	Serial Wire Clock	Input		VDDIO	
TRACESWO	Trace Asynchronous Data Out	Output		VDDIO	
Serial Peripheral Interface - SPI					
NPCS	SPI Chip Select	Input	Low	VDDIO	Internal pull up (4)
SPCK	SPI Clock signal	Input		VDDIO	Internal pull up (4)
MOSI	SPI Master Out Slave In	Input		VDDIO	Internal pull up (4)
MISO	SPI Master In Slave Out	Output		VDDIO	

Notes:

1. Separate pins are provided for GND and AGND grounds. Layout considerations should be taken into account to reduce interference. Ground pins should be connected as short as possible to the

system ground plane. For more details about EMC Considerations, please refer to AVR040 application note

2. Depending on whether an isolated or a non-isolated power supply is being used, isolation of this pin should be taken into account in the circuitry design. Please refer to the Reference Design for further information
3. See Table 13-4
4. See Table 13-5

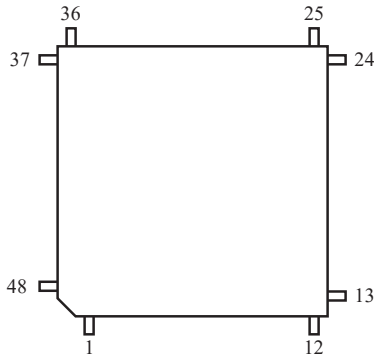
4. Package and Pinout

4.1 48–Lead TQFP Package Outline

The 48-lead TQFP package has a 0.5 mm pitch and respects Green standards.

Figure 4-1 shows the orientation of the 48-lead TQFP package. Refer to the section 14. Mechanical Characteristics for the 48-lead TQFP package mechanical drawing.

Figure 4-1. Orientation of the 48-Lead TQFP Package



4.2 48–Lead TQFP Pinout

Table 4-1. 48 - Lead TQFP Pinout

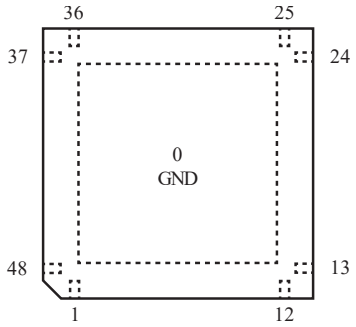
1	NRST	13	PA0	25	EMIT1	37	GND
2	XIN	14	PA1	26	VDDIO	38	AGND
3	XOUT	15	PA2/TRACESWO	27	EMIT2	39	VIN
4	VDDIO	16	PA3	28	VDDIO	40	VDDIN_AN
5	VDDPLL	17	PA6/NPCS0	29	VDDCORE	41	VREFP
6	GND	18	PA7/SPCK	30	GND	42	VREFC
7	VDDCORE	19	PA8/MOSI	31	EMIT3	43	VREFN
8	VDDIN	20	PA9/MISO	32	VDDIO	44	AGND
9	LDO ENABLE	21	VDDIO	33	PA11/TXRX1	45	VDDIN_AN
10	PA4/SWDIO	22	GND	34	PA10/TXRX0	46	VDDIO
11	PA5/SWCLK	23	EMIT0	35	AGC	47	PA12/VZC
12	VDDIO	24	VDDIO	36	VDDIO	48	TST

4.3 48–Lead QFN Package Outline

The 48-lead QFN package has a 0.4 mm pitch and respects Green standards.

Figure 4-1 shows the orientation of the 48-lead QFN package. Refer to the section 14. Mechanical Characteristics for the 48-lead QFN package mechanical drawing.

Figure 4-2. Orientation of the 48-Lead QFN Package



4.4 48–Lead QFN Pinout

Table 4-2. 48 - Lead QFN Pinout

0	GND						
1	NRST	13	PA0	25	EMIT1	37	GND
2	XIN	14	PA1	26	VDDIO	38	AGND
3	XOUT	15	PA2/TRACESWO	27	EMIT2	39	VIN
4	VDDIO	16	PA3	28	VDDIO	40	VDDIN_AN
5	VDDPLL	17	PA6/NPCS0	29	VDDCORE	41	VREFP
6	GND	18	PA7/SPCK	30	GND	42	VREFC
7	VDDCORE	19	PA8/MOSI	31	EMIT3	43	VREFN
8	VDDIN	20	PA9/MISO	32	VDDIO	44	AGND
9	LDO ENABLE	21	VDDIO	33	PA11/TXRX1	45	VDDIN_AN
10	PA4/SWDIO	22	GND	34	PA10/TXRX0	46	VDDIO
11	PA5/SWCLK	23	EMIT0	35	AGC	47	PA12/VZC
12	VDDIO	24	VDDIO	36	VDDIO	48	TST

4.5 Pinout Specification

Table 4-3. Pinout Specification

Pin	Power Rail	I/O Type	Primary		PIO Peripheral A		Reset State
			Signal	Dir	Signal	Dir	Signal, Dir, Hiz, ST
1	VDDIO	RST	NRST	I			I, Hiz
2	VDDIO	CLOCK	XIN	I			I, Hiz
3	VDDIO	CLOCK	XOUT	O			O
4	VDDIO	Power	VDDIO	-			

Pin	Power Rail	I/O Type	Primary		PIO Peripheral A		Reset State
			Signal	Dir	Signal	Dir	Signal, Dir, Hiz, ST
5	VDDPLL	Power	VDDPLL	-			
6	GNDOSC	Power	GNDOSC	-			
7	VDDCORE	Power	VDDCORE	-			
8	VDDIN	Power	VDDIN	-			
9	VDDIO	LDO	LDO ENABLE	I			I, Hiz
10	VDDIO	GPIO	PA4	I/O	SWDIO	I/O	SWDIO, I, Hiz
11	VDDIO	GPIO	PA5	I/O	SWCLK	I	SWCLK, I, Hiz
12	VDDIO	Power	VDDIO	-			
13	VDDIO	GPIO	PA0	I/O			PIO, I, Hiz
14	VDDIO	GPIO	PA1	I/O			PIO,I, Hiz
15	VDDIO	GPIO	PA2	I/O	TRACESWO	O	PIO, I, Hiz
16	VDDIO	GPIO	PA3	I/O			PIO, I, Hiz
17	VDDIO	GPIO	PA6	I/O	NPCS0	I	NPCS0, I, Hiz
18	VDDIO	GPIO	PA7	I/O	SPCK	I	SPCK, I, Hiz
19	VDDIO	GPIO	PA8	I/O	MOSI	I	MOSI, I, Hiz
20	VDDIO	GPIO	PA9	I/O	MISO	O	MISO, O, ST1
21	VDDIO	Power	VDDIO	-			
22	GND	Power	GND	-			
23	VDDIO	PLC	EMIT0	O			O, Hiz
24	VDDIO	Power	VDDIO	-			
25	VDDIO	PLC	EMIT1	O			O, Hiz
26	VDDIO	Power	VDDIO	-			
27	VDDIO	PLC	EMIT2	O			O, Hiz
28	VDDIO	Power	VDDIO	-			
29	VDDCORE	Power	VDDCORE	-			
30	GND	Power	GND	-			
31	VDDIO	PLC	EMIT3	O			O, Hiz
32	VDDIO	Power	VDDIO	-			
33	VDDIO	GPIO	PA11	I/O	TXRX1	O	PIO, I, Hiz

Pin	Power Rail	I/O Type	Primary		PIO Peripheral A		Reset State
			Signal	Dir	Signal	Dir	Signal, Dir, Hiz, ST
34	VDDIO	GPIO	PA10	I/O	TXRX0	O	PIO, I, Hiz
35	VDDIO	AGC	AGC	O			O, ST0
36	VDDIO	Power	VDDIO	-			
37	GND	Power	GND	-			
38	AGND	Ground	AGND	-			
39	VDDIN_AN	PLC	VIN	I			I, Hiz
40	VDDIN_AN	Power	VDDIN_AN	-			
41	VDDIN_AN	Analog	VREFP	-			
42	VDDIN_AN	Analog	VREFC	-			
43	VDDIN_AN	Analog	VREFN	-			
44	AGND	Ground	AGND	-			
45	VDDIN_AN	Power	VDDIN_AN	-			
46	VDDIO	Power	VDDIO	-			
47	VDDIO	GPIO	VZC/PA12	I			VZC/PIO, I, Hiz
48	VDDIO	TST	TST	I			

Note:

HiZ = High Impedance, ST = Set To.

5. Analog Front-End

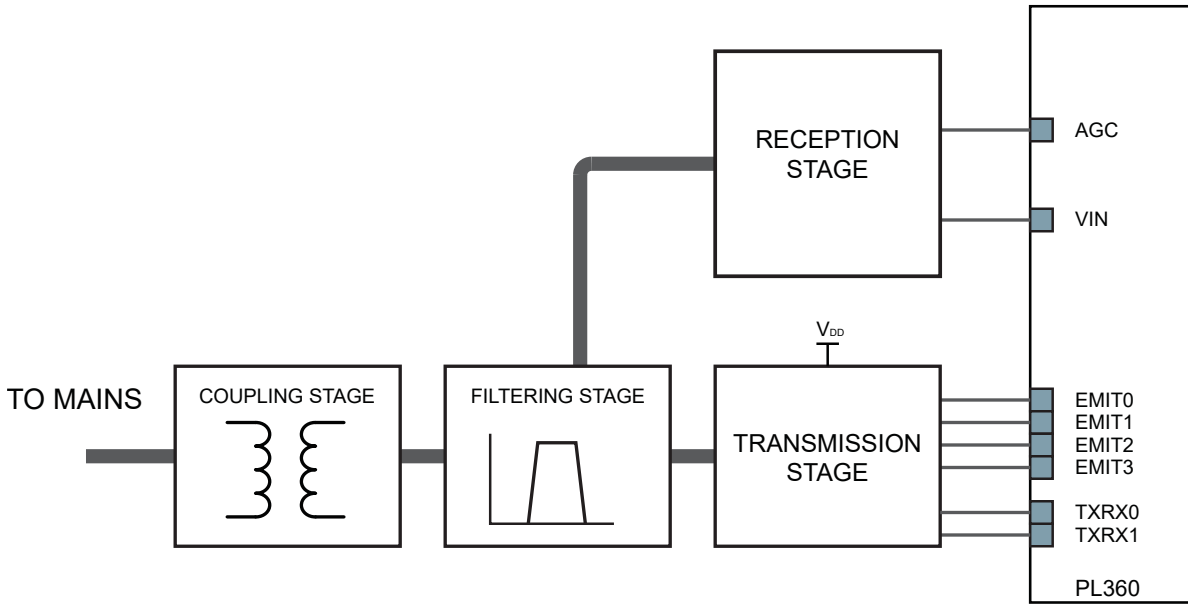
5.1 PLC Coupling Circuitry Description

Microchip PLC technology is purely digital and does not require external DAC/ADC, thus simplifying the external required circuitry. Generally, Microchip PLC coupling reference designs make use of few passive components plus a Class D amplification stage for transmission.

All PLC coupling reference designs are generally composed by the same sub-circuits:

- Transmission Stage
- Reception Stage
- Filtering Stage
- Coupling Stage

Figure 5-1. PLC Coupling Block Diagram



5.1.1 Transmission Stage

The transmission stage adapts the EMIT signals and amplifies them if required. It can be composed by:

- Driver: It adapts the EMIT signals to either control the amplifier or to be filtered by the next stage
- Amplifier: If required, a Class-D amplifier which generates a square waveform from 0 to VDD is included
- Bias and protection: It provides a DC component and provides protection from received disturbances

The transmission stage must be always followed by a filtering stage.

5.1.2 Filtering Stage

The in-band flat response filtering stage does not distort the injected signal, it reduces spurious emission to the limits set by the corresponding regulation and blocks potential interferences from other transmission channels.

The filtering stage has three aims:

- Band-pass filtering of high frequency components of the square waveform generated by the transmission stage
- Adapt Input/Output impedance for optimal reception/transmission. This is controlled by TXRX0 and TXRX1 signals
- In some cases, Band-pass filtering for received signals

When the system is intended to be connected to a physical channel with high voltage or which is not electrically referenced to the same point, then the filtering stage must be always followed by a coupling stage.

5.1.3 Coupling Stage

The coupling stage blocks the DC component of the line to/from which the signal is injected/received (i.e. 50/60 Hz of the mains). This is typically carried out by a high voltage capacitor.

The coupling stage can also electrically isolate the coupling circuitry from the external world by means of a 1:1 signal transformer.

5.1.4 Reception Stage

The reception stage adapts the received analog signal to be properly captured by the PL360 internal reception chain. The reception circuit is independent of the PLC channel which is being used. It basically consists of:

- Anti aliasing filter (RC Filter)
- Attenuation resistor for AGC circuit
- Driver of the internal ADC

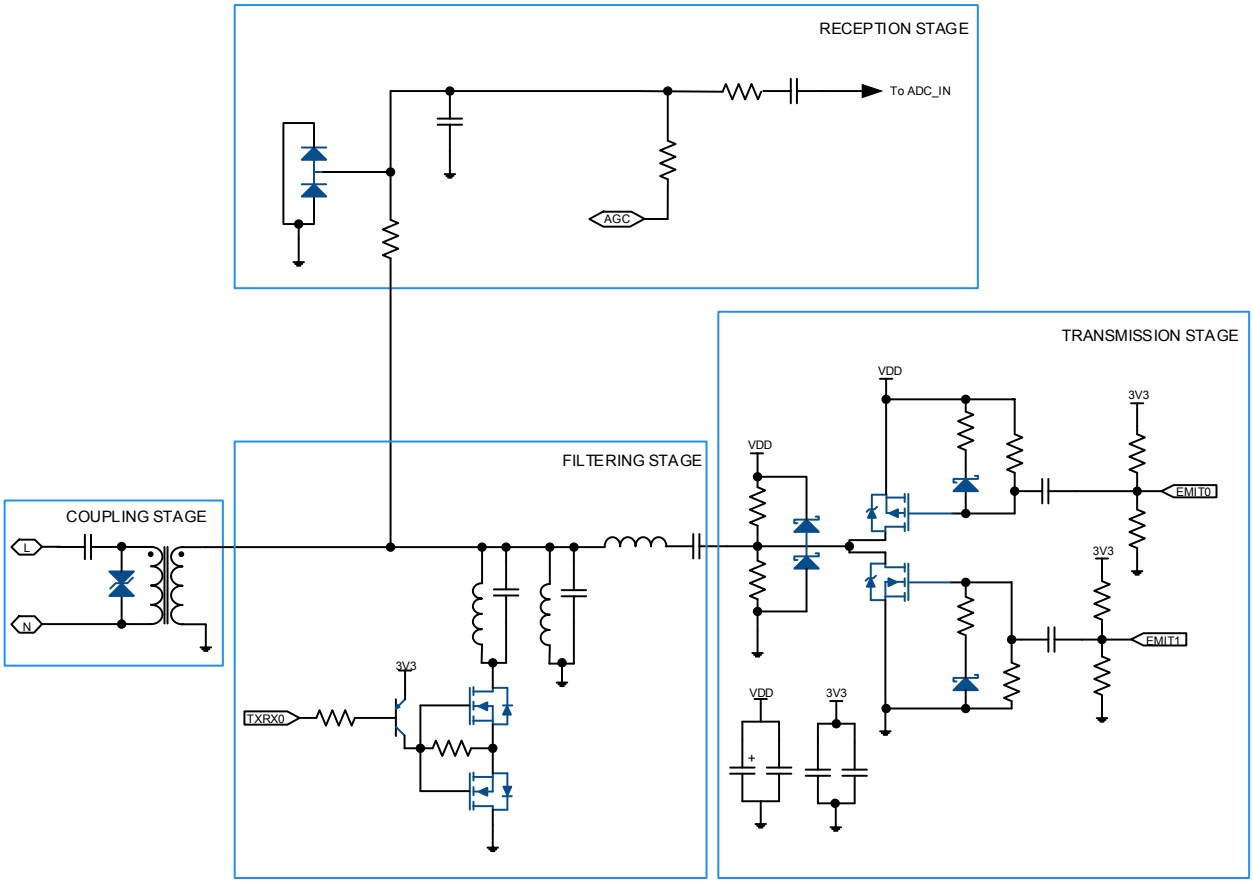
The AGC circuit avoids distortion on the received signal that may arise when the input signal is high enough to polarize the protection diodes in direct region.

The driver to the internal ADC comprises several resistors and capacitors, which provide a DC component and adapt the received signal to be converted by the internal reception chain.

5.1.5 Generic PLC Coupling

The figure below shows an example of a typical PLC coupling circuit, including all the stages previously described.

Figure 5-2. Single Branch PLC Coupling Block Diagram Example



5.2 Coupling Reference Designs

Microchip provides PLC coupling reference designs (usually refered to as ATPLCOUPxxx) for different applications and frequency bands up to 500 kHz, which have been designed to achieve high performance, low cost and simplicity.

6. Power Considerations

6.1 Power Supplies

The following table defines the power supply requirements of the PL360.

Table 6-1. Power Supplies

Name	Associated Ground	Powers
VDDCORE	GND	Core power supply with internal connection to 1.25V voltage regulator output. Decoupling capacitors required.
VDDIO	GND	3.3V Digital supply. Digital power supply must be decoupled by external capacitors.
VDDIN	GND	3.3V Voltage regulator input.
VDDIN_AN	AGND	3.3V Analog supply (ADC + PGA).
VDDPLL	GND	1.25V Voltage Regulator Output. Connected to VDDCORE through a LP filter.

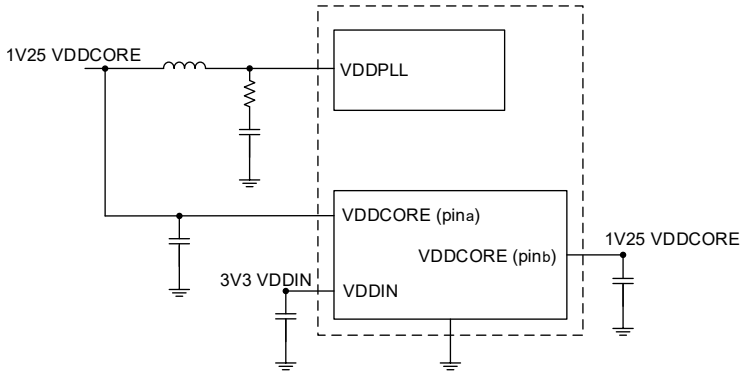
The PL360 embeds a voltage regulator to supply the core. The Voltage Regulator state is controlled by the external LDO ENABLE pin. The two VDDCORE pins in the package must be populated with external decoupling capacitors, the VDDCORE pin close to the VDDPLL pin should be populated with a 4.7µF low ESR capacitor, an 1.0µF or 2.2µF capacitor should be connected to the second VDDCORE pin.

6.2 Power Constraints

The following power constraints apply to PL360 device. Deviating from these constraints may lead to unwanted device behavior.

- VDDIN and VDDIO must have the same level, 3.3V
- VDDPLL voltage must be derived from VDDCORE through a low-pass filter. A second order LC with cutoff frequency equal to 25 KHz should be used. The inductor can be replaced by a ferrite bead, then a cutoff frequency equal to 75 KHz could be acceptable. In those cases, it is mandatory to check the communication performances of the system to detect problems originated from poor PLL supply filtering

Figure 6-1. Voltage Regulator Connectivity(1)



Note:

1. Please refer to the schematics of the evaluation board for further information about correct values of decoupling capacitors and low-pass filter components

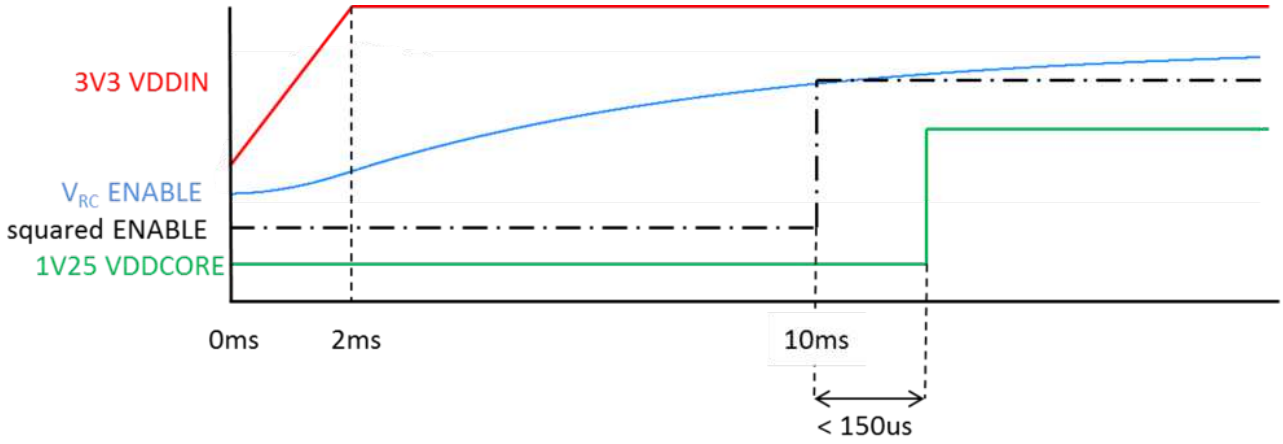
For more information on power considerations, refer to section 13.8 Power On Considerations.

6.2.1 Power-up

VDDIO and VDDIN must rise simultaneously, prior to VDDCORE and VDDPLL rising. This is respected if VDDCORE and VDDPLL are supplied by the embedded voltage regulator and the voltage regulator is turned on after VDDIN reaches 3.3V.

The figure below shows system response when an RC delay line (R = 6K8Ω, C = 1µF) is used to derive ENABLE control from VDDIN.

Figure 6-2. Power-up Sequence



6.2.2 Power-down

VDDIO and VDDIN should fall simultaneously, VDDCORE and VDDPLL will fall later as the regulator VDDIN decreases.

7. Input/Output Lines

The PL360 has several kinds of input/output (I/O) lines such as general purpose I/Os (PA) and system I/Os. PAs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in I/O mode or by the multiplexed peripheral.

7.1 General-Purpose I/O Lines

PA Lines are managed and configured internally.

7.2 System I/O Lines

System I/O lines are pins used by oscillators, Test mode and Reset.

7.2.1 Test Mode (TST) Pin

The TST pin is used to set the circuit in manufacturing Test mode. It must be tied to ground for normal operation.

7.2.2 Reset (NRST) Pin

The NRST pin is unidirectional. It is controlled externally and can be driven low to provide a Reset signal to reset the PL360. It resets the core and the peripherals. There is no constraint on the length of the Reset pulse.

8. Bootloader

8.1 Description

The bootloader loads the program from an external master to the internal memory of PL360. It allows loading of plain programs or secured programs. When a secured program is loaded, the original program length must be padded to become a multiple of 16 bytes, and the length (number of blocks, where a block is 16 bytes set) must be specified for a correct signature validation and decryption.

Signature uses AES128 CMAC. Signature can be calculated over the {Encrypted Software} or over {Encrypted Software + Initialization Vector + Number of Blocks}. The number of blocks, for signature calculation, will be specified as 16 bytes integer number in the {image}, although the number is programmed as a 16-bit integer in the corresponding register of the bootloader.

Decryption of the secured program uses AES128 CBC.

System operation, when secured software transfer has been selected, will not start unless signature validation and decryption pass correctly.

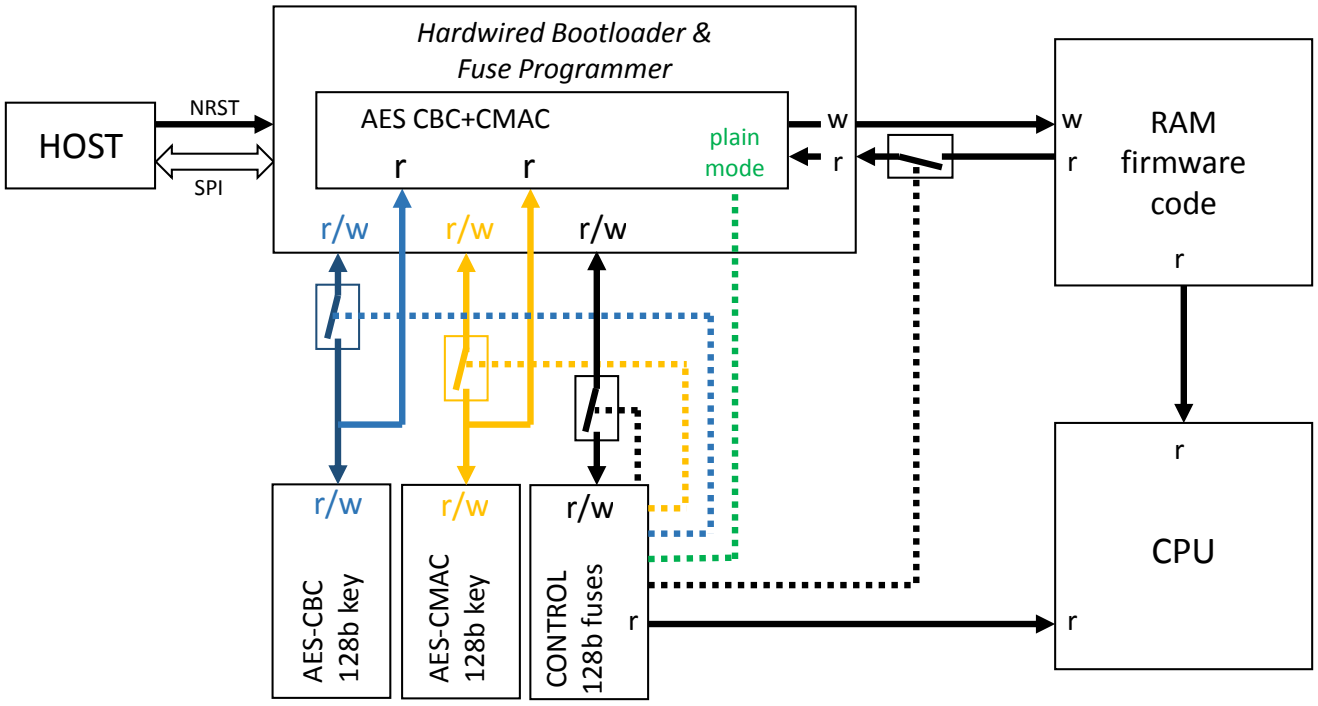
The bootloader also allows programming of security keys and security control fuses.

8.2 Embedded Characteristics

- Bootloader operates on SCK (typ.freq. 12Mhz, max.freq≤16Mhz), synchronously with core and bus clocks
- Fixed phase and polarity SPI control protocol
- Password to unlock bootloader
- Fuse programming control

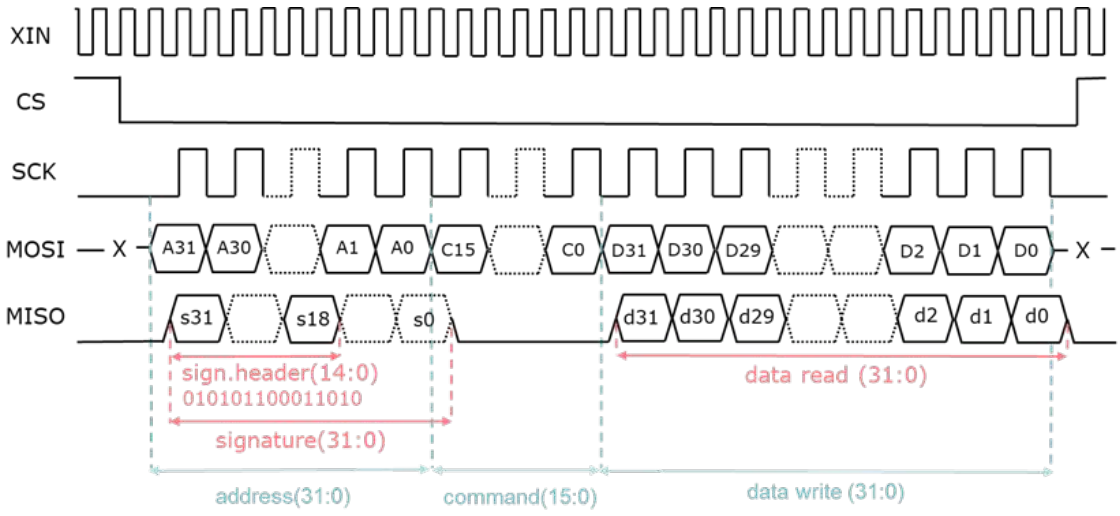
8.3 Block Diagram

Figure 8-1. Block Diagram



8.4 Functional Description

The bootloader loads the program from an external master to the internal memory of PL360. The external master can access instruction memory, data memory and registers through SPI. The bootloader only works in SPI Mode 0 (CPHA=1 and CPOL=0). The basic data transfer is:



The basic frame sent from the master through the MOSI signal is composed as shown in the following table:

Address	Command	Data
32 bits	16 bits	n words of 32 bits

Each frame received from the master will be acknowledged with a 32 signature through the MISO signal.

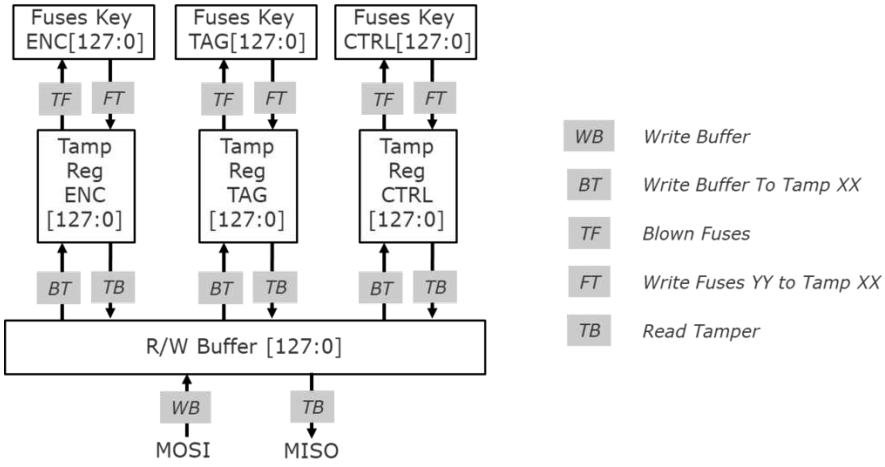
There is a series of SPI commands supported by the bootloader. The commands are:

Command	Description	addr(31:0)	data(n*32-1:0)
0x0000	Write word on one address	0xAAAAAAAA(1)	0xDDDDDDDD(2)
0x0001	Write words on consecutive address	0xAAAAAAAA(1)	0xDDD…DDD(2) (3)
0x0002	Read words on consecutive address	0xAAAAAAAA(1)	0x000…000(4)
0x0003	Read word on one address	0xAAAAAAAA(1)	0x00000000
0x0004	Write number of decryption packets	0x00000000	0x0000DDDD(2)
0x0005	Write decryption initial vector	0x00000000	0xDDD…DDD(2) (3)
0x0006	Write decryption signature	0x00000000	0xDDD…DDD(2) (3)
0x0007	Write 128 bits fuses value to Buffer register	0x00000000	0xDDD…DDD(2) (3)
0x0008	Write Buffer register to Tamper register for KEY_ENC_FUSES	0x00000000	0x00000000
0x0009	Write Buffer register to Tamper register for KEY_TAG_FUSES	0x00000000	0x00000000
0x000B	Write Buffer register to Tamper register for CONTROL_FUSES	0x00000000	0x00000000
0x000C	Blow desired fuses	0x00000000	0x00000000
0x000D	Write KEY_ENC_FUSES to the corresponding Tamper register	0x00000000	0x00000000
0x000E	Write KEY_TAG_FUSES to the corresponding Tamper register	0x00000000	0x00000000
0x0010	Write CONTROL_FUSES to the corresponding Tamper register	0x00000000	0x00000000
0x0011	Read Tamper register	0x00000000	0x000…000(4)
0x0012	Read bootloader status	0x00000000	0x00000000
0x0013	Start Decryption	0x00000000	0x00000000
0x0014	Start/Stop BOOTLOADER access window in Master mode	0x00000000	0x00000000
0x0015	Start Decryption Plus	0x00000000	0x00000000
0xA55A	Control of MISO signal transferred to M7-SPI	0x00000000	0x00000000
0xDE05	Unblock bootloader	0x00000000	0x00000000

Notes:

1. 'AA' is an address byte
2. 'DD' is a data byte
3. Command contains as many bytes as needed to send
4. Command contains as many '00's as bytes wanted to be read

Figure below shows the structure of the registers and data transfers for fuses and their control logic.



8.4.1 Unlock, Load Program and Start Loaded Program

After Reset, the bootloader is locked, and the master must send two frames as password to unlock the bootloader. These frames are:

Order	Address	Command	Data
1	0x00000000	0xDE05	0x5345ACBA
2	0x00000000	0xDE05	0xACBA5345

At this point, the master sends commands to the bootloader and it can start loading the program to PL360. The program must be loaded starting in address 0x00000000.

After loading the program, it must be started. To start the loaded program requires clearing of the CPUWAIT bit of MSSC Miscellaneous register (Address 0x400E1800) and transferring the control of MISO signal to M7-SPI peripheral:

Order	Address	Command	Data
1	0x400E1800	0x0000	0x00000000
2	0x00000000	0xA55A	0x00000000

If this action is not done, MISO signal will remain controlled by the BOOTLOADER.

8.4.2 Bootloader Hardware Signature

Each frame received from the master (write or read frame), will be acknowledged with a 32 bits signature through the MISO signal. This is used to give the bootloader's signature and the state of the system to the master.

This frame is composed of:

Bit	Name	Value
31..17	BOOT_SIGN	010101100011010
16	RST_STATUS	USER_RST
15		CM7_RESET
14		WDT_RESET
13	BOOT_FUSE	
12	CHIP_ID	
11	RESERVED	
10	HSM_FUSE	
9	AES_FUSES	AES_DIS
8		AES_128
7..2	RESERVED	
1..0	FREE_FUSES	

8.4.3 Write Process

The command used to write on a unique address is CMD=0x0000.

The command used to write on several consecutive addresses is CMD=0x0001. In this case, it will be sent the 32 bits of the initial address, 16 bits of command (0x0001) and as many consecutive words (32 bits) as are wanted to write.

Regarding the decryption packets, the commands to write the number of decryption packets (CMD=0x0004), the initial vector of decryption (CMD=0x0005) or the decryption signature to test if decryption is correct (CMD=0x0006), the address of the frame is not taken into account and it can be composed with any address value. To write the decryption packet, only the last 15 bits are taken into account. In the case of decryption initial vector and decryption signature where it is necessary to send as data the 128 bit value, it is made in the same way than the write process at consecutive addresses, sending 4 consecutive words (32 bits).

To write a fuse box, the Buffer register must be written in advance (CMD=0x0007) and then the Tamper registers of KEY_ENC_BOX, KEY_TAG_BOX or CONTROL_BOX must be written with the content of the buffer (CMD=0x0008, CMD=0x0009 and CMD=0x000B respectively). Finally, to blow the desired fuses with the values in the corresponding Tamper register, the command (CMD=0x000C) must be sent with any address and any data value.

The end of this writing process is indicated in the answer of the bootloader status command (CMD=0x0012). If the writing process is active, bit 0 of the answer is ‘1’. In other case, all data of the answer is 0.

In the case of CONTROL_BOX, to activate the new values, it is also necessary to write the CONTROL_FUSES values to the corresponding Tamper register (CMD=0x0010).

8.4.4 Read Process

The command used to read an unique address is CMD=0x0003.

The command used to read several consecutive addresses is CMD=0x0002. In this case the frame will be composed of 32 bits for the address, 16 bits for the command and as many SCK pulses (always multiple of 32) as needed to read data.