Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MPQ8632

High Efficiency 18V Synchronous Step-down Converter Family for 4A to 20A

The Future of Analog IC Technology

Part Number	Current Rating (A)	Input Voltage	OVP Mode
MPQ8632GLE-4	4	2.5V to 18V	Non-Latch
MPQ8632GLE-6	6	2.5V to 18V	Non-Latch
MPQ8632GLE-8	8	2.5V to 18V	Non-Latch
MPQ8632HGLE-10	10	2.5V to 18V	Non-Latch
MPQ8632GLE-10	10	2.5V to 18V	Latch-Off
MPQ8632GLE-12	12	2.5V to 18V	Non-Latch
MPQ8632GVE-15	15	2.5V to 18V	Non-Latch
MPQ8632GVE-20	20	2.5V to 18V	Non-Latch

DESCRIPTION

The MPQ8632 is a fully integrated high frequency synchronous rectified step-down switch mode converter. It offers a very compact solution to achieve 4A/6A/8A/10A/12A/15A/20A output current over a wide input supply range with excellent load and line regulation.

The MPQ8632 uses Constant-On-Time (COT) control mode to provide fast transient response and ease loop stabilization.

An external resistor programs the operating frequency from 200kHz to 1MHz and the frequency keeps nearly constant as input supply varies with the feedforward compensation.

The default under voltage lockout threshold is internally set at 4.1V, but a resistor network on the enable pin can increase this threshold. The soft start pin controls the output voltage startup ramp. An open drain power good signal indicates that the output is within nominal voltage range.

It has fully integrated protection features that include over-current protection, over-voltage protection and thermal shutdown.

The MPQ8632 requires a minimal number of readily available standard external components and is available in a 16-Pin QFN 3mm×4mm or a 29-Pin QFN 5mm×4mm package.

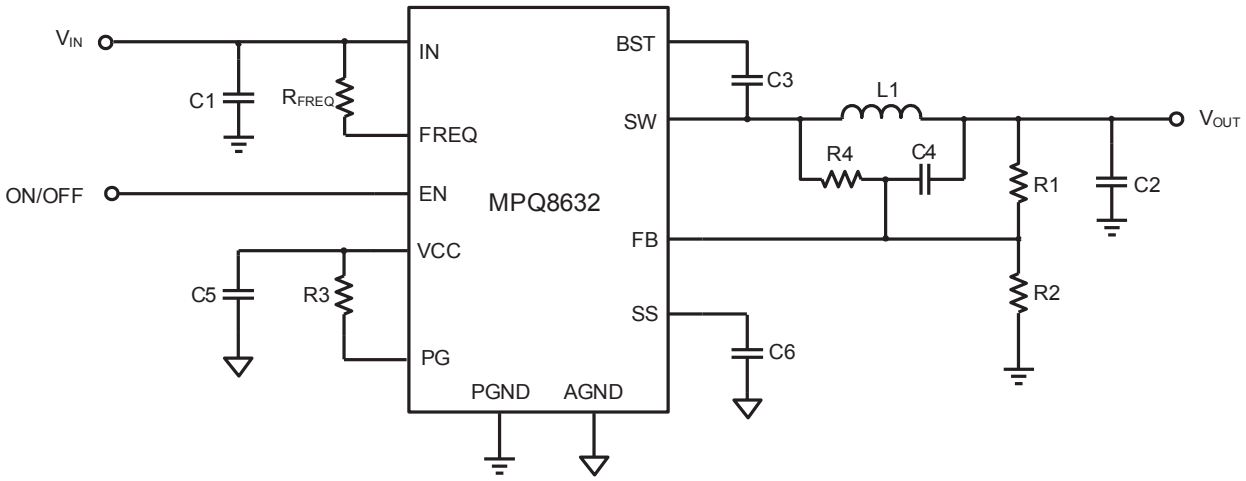
FEATURES

- Low Input Voltage Range from 2.5V:
  -- 2.5V to 18V with External 5V Bias
  -- 4.5V to 18V with Internal Bias
- Scalable Family of Products for 4A to 20A Output Current Applications
  -- 4A/6A/8A/10A/12A Share the Same Footprint
  --15A/20A Share the Same Footprint, with Slight Change on Power Stage Section from 4A/6A/8A/10A/12A
- Optimal Low R_{DS}(ON) Internal Power MOSFETs Per Device
- Proprietary Switching Loss Reduction Technique
- Adaptive COT for Ultrafast Transient Response
- 0.5% Reference Voltage Over 0°C to 70°C Junction Temperature Range
- Programmable Soft Start Time
- Pre-Bias Start up
- Programmable Switching Frequency from 200kHz to 1MHz
- Non-latch OCP, OVP and Thermal Shutdown Protection
- Output Adjustable from 0.611V to 13V

APPLICATIONS

- Telecom and Networking Systems
- Base Stations
- Servers
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION



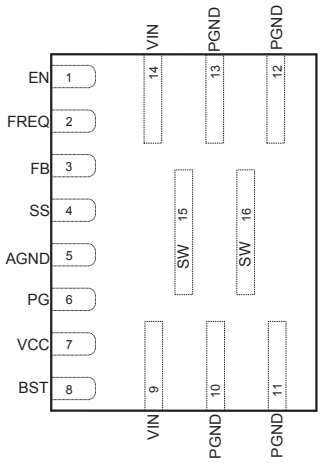
ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ8632GLE-4*	QFN(3X4mm)	MP8632 E4
MPQ8632GLE-6	QFN(3X4mm)	MP8632 E6
MPQ8632GLE-8	QFN(3X4mm)	MP8632 E8
MPQ8632GLE-10	QFN(3X4mm)	MP8632 E10
MPQ8632HGLE-10	QFN(3X4mm)	MP8632H E10
MPQ8632GLE-12	QFN(3X4mm)	MP8632 E12
MPQ8632GVE-15	QFN(5X4mm)	MP8632 E15
MPQ8632GVE-20	QFN(5X4mm)	MP8632 E20

* For Tape & Reel, add suffix –Z (e.g. MPQ8632GLE–4–Z)

PACKAGE REFERENCE

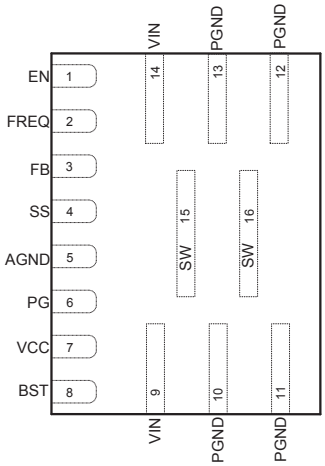
TOP VIEW



Part Number*	Package
MPQ8632GLE-4	QFN (3x4mm)
Junction Temperature	**Top Marking**
–40°C to +125°C	MP8632 E4

* For Tape & Reel, add suffix –Z (eg. MPQ8632GLE-4–Z)

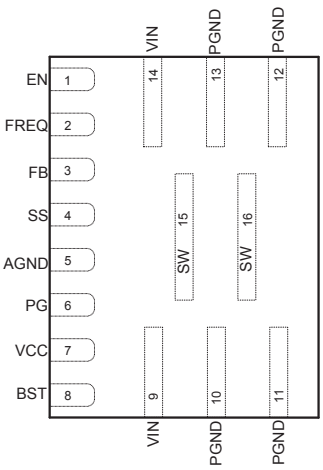
TOP VIEW



Part Number*	Package
MPQ8632GLE-6	QFN (3x4mm)
Junction Temperature	**Top Marking**
–40°C to +125°C	MP8632 E6

* For Tape & Reel, add suffix –Z (eg. MPQ8632GLE-6–Z)

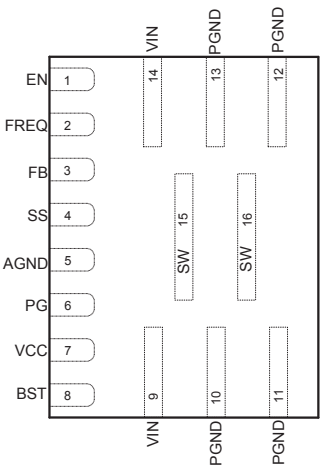
TOP VIEW



Part Number*	Package
MPQ8632GLE-8	QFN (3x4mm)
Junction Temperature	**Top Marking**
–40°C to +125°C	MP8632 E8

***** For Tape & Reel, add suffix –Z (eg. MPQ8632GLE-8–Z)

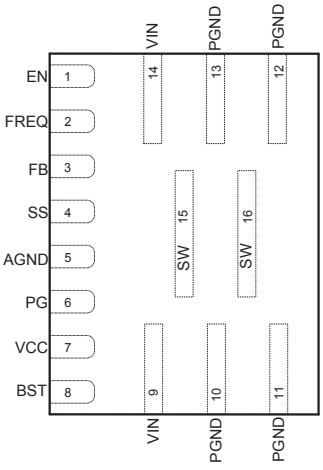
TOP VIEW



Part Number*	Package
MPQ8632GLE-10	QFN (3x4mm)
Junction Temperature	**Top Marking**
–40°C to +125°C	MP8632 E10

***** For Tape & Reel, add suffix –Z (eg. MPQ8632GLE-10–Z)

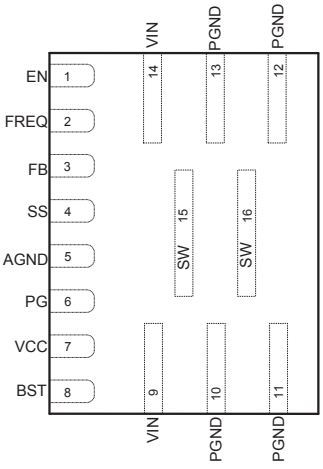
TOP VIEW



Part Number*	Package
MPQ8632HGLE-10	QFN (3x4mm)
Junction Temperature	**Top Marking**
–40°C to +125°C	MP8632H E10

***** For Tape & Reel, add suffix –Z (eg. MPQ8632HGLE-10–Z)

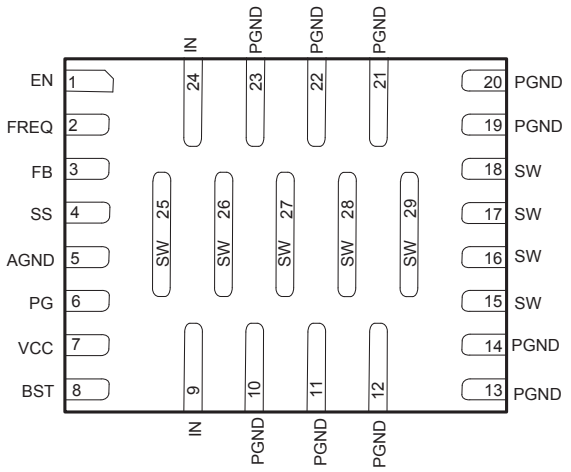
TOP VIEW



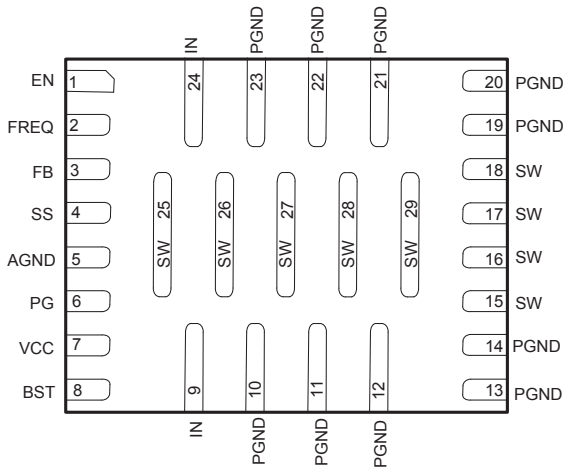
Part Number*	Package
MPQ8632GLE-12	QFN (3x4mm)
Junction Temperature	**Top Marking**
–40°C to +125°C	MP8632 E12

***** For Tape & Reel, add suffix –Z (eg. MPQ8632GLE-12–Z)

TOP VIEW



TOP VIEW



Part Number*	Package	Part Number*	Package
MPQ8632GVE-15	QFN (5x4mm)	MPQ8632GVE-20	QFN (5x4mm)
Junction Temperature	**Top Marking**	**Junction Temperature**	**Top Marking**
–40°C to +125°C	MP8632 E15	–40°C to +125°C	MP8632 E20
* For Tape & Reel, add suffix –Z (eg. MPQ8632GVE-15–Z)		* For Tape & Reel, add suffix –Z (eg. MPQ8632GVE-20–Z)	

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 21V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{SW} (30ns) ..... -3V to V_{IN} + 3V
V_{BST} ..... V_{SW} + 6V
V_{BST} (30ns) ..... V_{SW} + 6.5V
Enable Current I_{EN} (2) 2.5mA
All Other Pins ..... –0.3V to +6V
Continuous Power Dissipation (T_A=+25°) (3)
QFN3X4 ..... 2.7W
QFN5X4 ..... 3.3W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 18V
Output Voltage V_{OUT} ..... 0.611V to 13V
Enable Current I_{EN} 1mA
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
QFN (3x4mm)	46	9	°C/W
QFN (5x4mm)	38	6	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Refer to the section “Configuring the EN Control”.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		0	1	μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V	700	860	1000	μA
MOSFET						
High-side Switch On Resistance	HS_{RDS-ON}	MPQ8632GLE-4,6,8, T_J =25°C		28		mΩ
		MPQ8632GLE-10,12, MPQ8632HGLE-10, T_J =25°C		19.6		mΩ
		MPQ8632GVE-15,20, T_J =25°C		9.9		mΩ
Low-side Switch On Resistance	LS_{RDS-ON}	MPQ8632GLE-4, T_J =25°C		16.4		mΩ
		MPQ8632GLE-6, T_J =25°C		15.8		
		MPQ8632GLE-8, T_J =25°C		15.3		
		MPQ8632GLE-10, MPQ8632HGLE-10, T_J =25°C		5.7		
		MPQ8632GLE-12, T_J =25°C		5.2		
		MPQ8632GVE-15, T_J =25°C		3		
		MPQ8632GVE-20, T_J =25°C		2.4		
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	10	μA
Current Limit						
High-side Peak Current Limit	I_{LIMIT_PEAK}	MPQ8632GLE-10	13	17.3	21.6	A
Low-side Valley Current Limit(6)	I_{LIMIT_VALLEY}	MPQ8632GLE-4	4	5	6	A
		MPQ8632GLE-6	6.5	7.5	8.5	
		MPQ8632GLE-8	8	10	12	
		MPQ8632GLE-10	9.5	11	12.5	
		MPQ8632HGLE-10	10	13	16	
		MPQ8632GLE-12	12	15	18	
		MPQ8632GVE-15	15	20	25	
		MPQ8632GVE-20	20	25	30	
Low-side Negative Current Limit(6)	$I_{LIMIT\_NEGATIVE}$	MPQ8632GVE-15	-6.6	-5.6	-4.6	A
		All other parts	-4	-2.5	-1	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Timer						
One-Shot On Time	T_{ON}	R_{FREQ}=453kΩ, V_{OUT}=1.2V		250		ns
Minimum On Time(6)	T_{ON_MIN}		20	30	40	ns
Minimum Off Time(6)	T_{OFF_MIN}	MPQ8632GLE-10	50	100	150	ns
		Other parts	200	360	420	
Over-voltage and Under-voltage Protection						
OVP Latch Threshold(6)	$V_{OVP\ LATCH}$	MPQ8632GLE-10	127%	130%	133%	V_{FB}
OVP Non-latch Threshold	$V_{OVP\_NON-LATCH}$		117%	120%	123%	V_{FB}
OVP Delay	T_{OVP}			2		µs
UVP Threshold(6)	V_{UVP}		47%	50%	53%	V_{FB}
Reference And Soft Start						
Reference Voltage	V_{REF}	T_J = 0°C to +70°C	608	611	614	mV
		T_J = 0°C to +125°C	605	611	617	mV
		T_J = -40°C to +125°C	602	611	620	mV
Feedback Current	I_{FB}	V_{FB} = 611mV		50	100	nA
Soft Start Charging Current	I_{SS}	V_{SS}=0V	16	20	25	µA
Enable And UVLO						
Enable Input Low Voltage	VIL_{EN}		1.1	1.3	1.5	V
Enable Hysteresis	V_{EN-HYS}			250		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		0		µA
		V_{EN} = 0V		0		
VCC Regulator						
VCC Under Voltage Lockout Threshold Rising	VCC_{Vth}			3.8		V
VCC Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}			500		mV
VCC Regulator	V_{CC}			4.8		V
VCC Load Regulation		Icc=5mA		0.5		%
Power Good						
Power Good Rising Threshold	PG_{Vth-Hi}		87%	91%	94%	V_{FB}
Power Good Falling Threshold	PG_{Vth-Lo}			80%		V_{FB}
Power Good Lower to High Delay	PG_{Td}			2.5		ms
Power Good Sink Current Capability	I_{OL}	V_{OL}=600mV			12	mA
Power Good Leakage Current	$I_{PG\ LEAK}$	V_{PG} = 3.3V		10		nA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection (6)						
Thermal Shutdown	T_{SD}		150			°C
Thermal Shutdown Hysteresis				25		°C

Note:

6) Guaranteed by design.

PIN FUNCTIONS

MPQ8632GLE-4, MPQ8632GLE-6, MPQ8632GLE-8, MPQ8632GLE-10, MPQ8632HGLE-10, MPQ8632GLE-12

PIN #	Name	Description
1	EN	Enable. Digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Connect EN to IN through a pull-up resistor or a resistive voltage divider for automatic startup. Do not float this pin.
2	FREQ	Frequency Set. Require a resistor connected between FREQ and IN to set the switching frequency. The input voltage and the resistor connected to the FREQ pin determine the ON time. The connection to the IN pin provides line feed-forward and stabilizes the frequency during input voltage's variation.
3	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. FB is also configured to realize over-voltage protection (OVP) by monitoring output voltage. MPQ8632 and MPQ8632H provide different OVP mode. Please refer to the section "Over-Voltage-Protection (OVP)". Place the resistor divider as close to FB pin as possible. Avoid using vias on the FB traces.
4	SS	Soft Start. Connect an external capacitor to program the soft start time for the switch mode regulator.
5	AGND	Analog ground. The control circuit reference.
6	PG	Power Good. The output is an open drain signal. Require a pull-up resistor to a DC voltage to indicate high if the output voltage exceeds 91% of the nominal voltage. There is a delay from FB ≥ 91% to PG goes high.
7	VCC	Internal 4.8V LDO Output. Power the driver and control circuits. 5V external bias can disable the internal LDO. Decouple with a ≥ 1μF ceramic capacitor as close to the pin as possible. For best results, use X7R or X5R dielectric ceramic capacitors for their stable temperature characteristics.
8	BST	Bootstrap. Require a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
9, 14	IN	Supply Voltage. Supply power to the internal MOSFET and regulator. The MPQ8632 operates from a +2.5V to +18V input rail with 5V external bias and a +4.5V to +18V input rail with internal bias. Require an input decoupling capacitor. Connect using wide PCB traces and multiple vias.
10-13	PGND	System Ground. Reference ground of the regulated output voltage. PCB layout requires extra care. Connect using wide PCB traces.
15, 16	SW	Switch Output. Connect to the inductor and bootstrap capacitor. The high-side switch drives the pin up to the V_{IN} during the PWM duty cycle's ON time. The inductor current drives the SW pin negative during the OFF-time. The low-side switch's ON-resistance and the internal Schottky diode clamp the negative voltage. Connect using wide PCB traces.

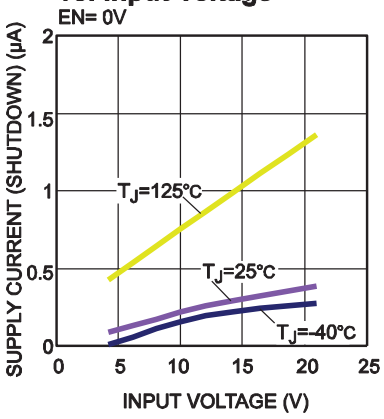
MPQ8632GVE-15, MPQ8632GVE-20

PIN #	Name	Description
1	EN	Enable. Digital input that turns the regulator on or off. Drive EN high to turn on the regulator; drive it low to turn it off. Connect EN to IN through a pull-up resistor or a resistive voltage divider for automatic startup. Do not float this pin.
2	FREQ	Frequency Set. Require a resistor connected between FREQ and IN to set the switching frequency. The input voltage and the resistor connected to the FREQ pin determine the ON time. The connection to the IN pin provides line feed-forward and stabilizes the frequency during input voltage's variation.
3	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. Place the resistor divider as close to FB pin as possible. Avoid using vias on the FB traces.
4	SS	Soft-Start. Connect an external capacitor to program the soft start time for the switch mode regulator.
5	AGND	Analog Ground. The control circuit reference.
6	PG	Power-Good. The output is an open drain signal. Requires a pull-up resistor to a DC voltage to indicate HIGH if the output voltage exceeds 91% of the nominal voltage. There is a delay from FB ≥ 91% to when PG goes high.
7	VCC	Internal 4.8V LDO Output. Powers the driver and control circuits. 5V external bias can disable the internal LDO. Decouple with a ≥1μF ceramic capacitor as close to the pin as possible. For best results, use X7R or X5R dielectric ceramic capacitors for their stable temperature characteristics.
8	BST	Bootstrap. Require a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
15-18, 25-29	SW	Switch Output. Connect to the inductor and bootstrap capacitor. The high-side switch drives these pins up to V_{IN} during the PWM duty cycle's ON time. The inductor current drives the SW pin negative during the OFF-time. The low-side switch's ON-resistance and the internal Schottky diode holds the negative voltage. Connect all SW pins using wide PCB traces.
10-14, 19-23	PGND	System Ground. Reference ground of the regulated output voltage. PCB layout requires extra care. Connect using wide PCB traces.
9, 24	IN	Supply Voltage. Supplies power to the internal MOSFET and regulator. The MPQ8632GVE operate from a 4.5V-to-18V input rail. If 5V external bias is tied to VCC pin, the input voltage can be low as 2.5V. Requires an input decoupling capacitor. Connect using wide PCB traces and multiple vias.

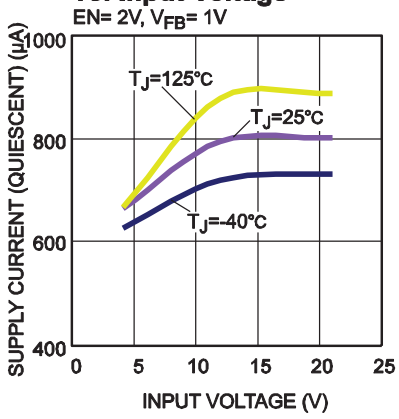
TYPICAL CHARACTERISTICS

MPQ8632GLE-10, VIN = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25ºC, unless otherwise noted.

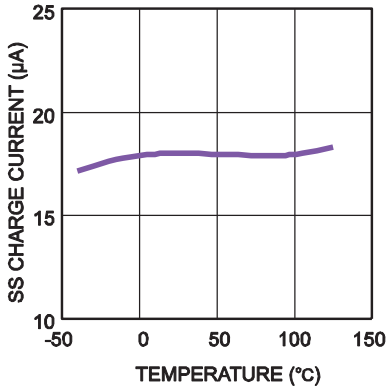
Supply Current (Shutdown) vs. Input Voltage



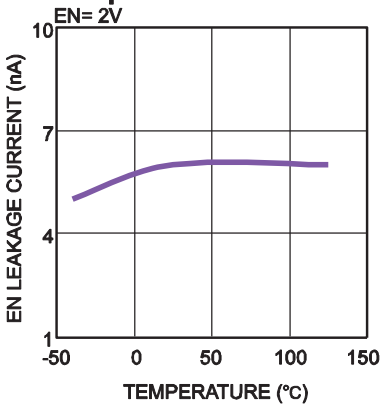
Supply Current (Quiescent) vs. Input Voltage



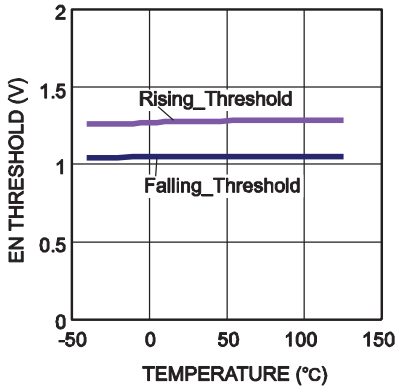
SS Charge Current vs. Temperature



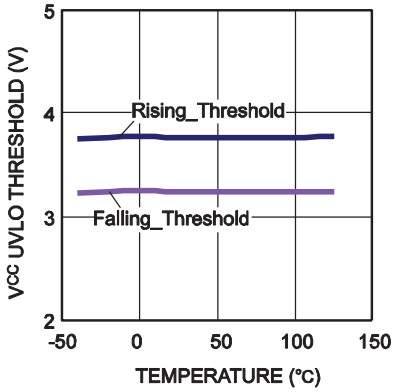
EN Leakage Current vs. Temperature



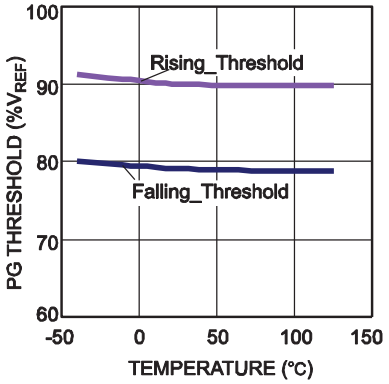
EN Threshold vs. Temperature



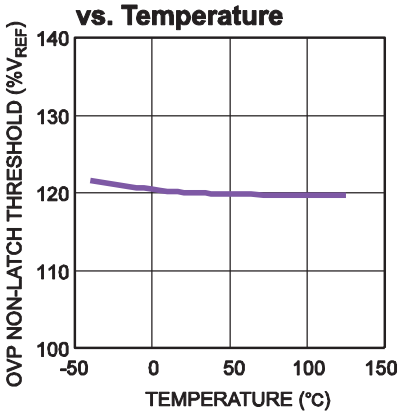
V_{CC} UVLO Threshold vs. Temperature



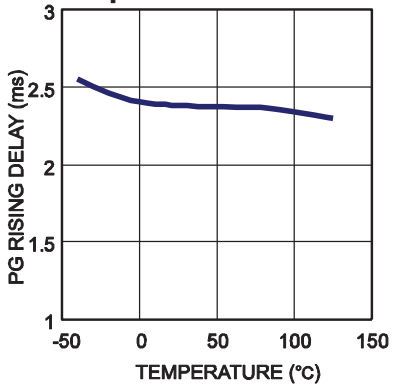
PG Threshold vs. Temperature



OVP Non-Latch Threshold vs. Temperature



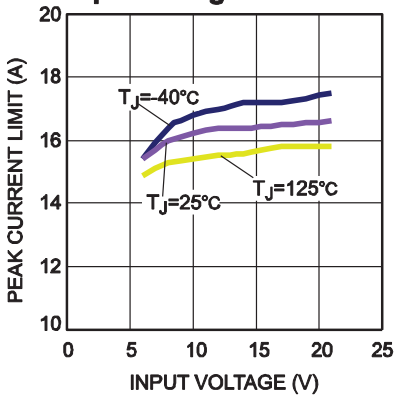
PG Rising Delay vs. Temperature



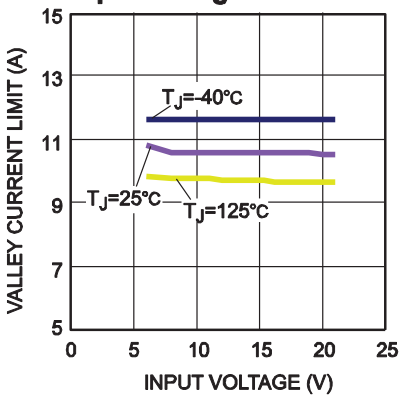
TYPICAL CHARACTERISTICS *(continued)*

MPQ8632GLE-10, V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25ºC, unless otherwise noted.

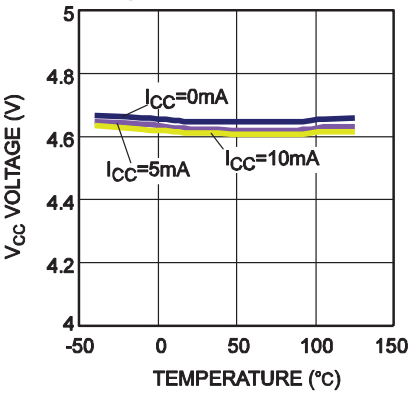
Peak Current Limit vs. Input Voltage



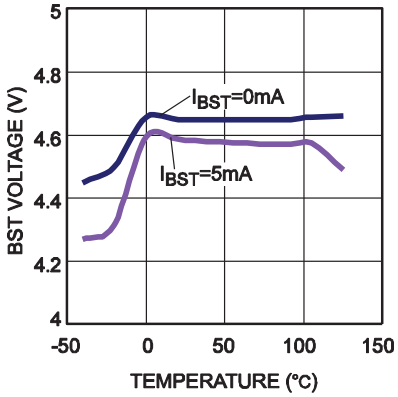
Valley Current Limit vs. Input Voltage



V_{CC} Voltage vs. Temperature

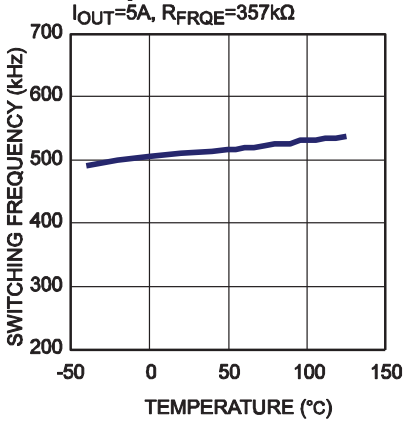


BST Voltage vs. Temperature

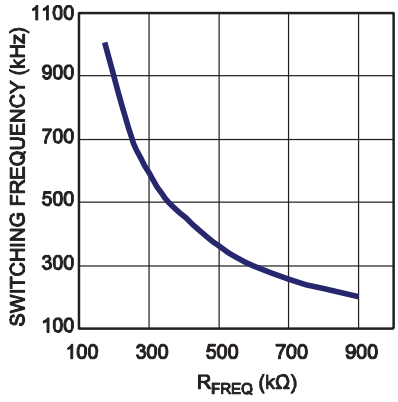


Switching Frequency vs. Temperature

I_{OUT}=5A, R_{FRQE}=357kΩ

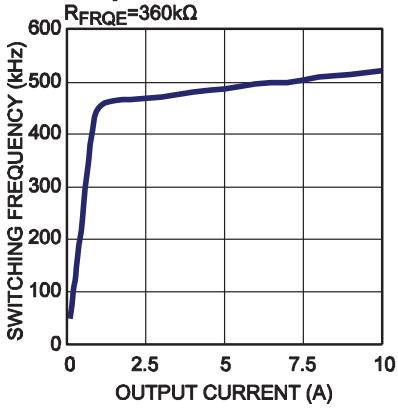


Switching Frequency vs. R_{FREQ}



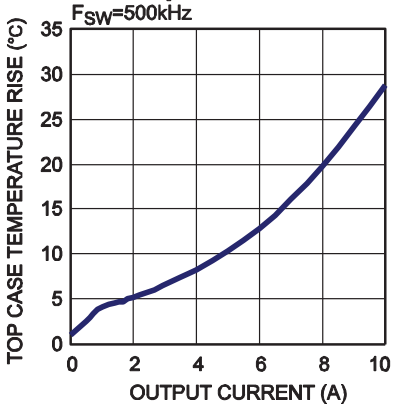
Switching Frequency vs. Output Current

R_{FRQE}=360kΩ



Case Temperature Rise vs. Output Current

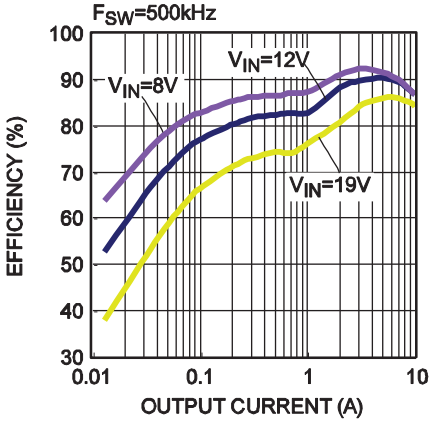
F_{SW}=500kHz



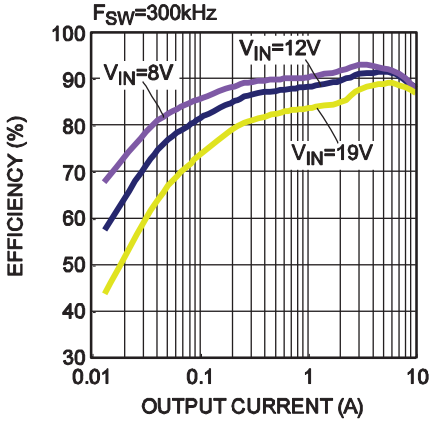
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8632GLE-10, V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25ºC, unless otherwise noted.

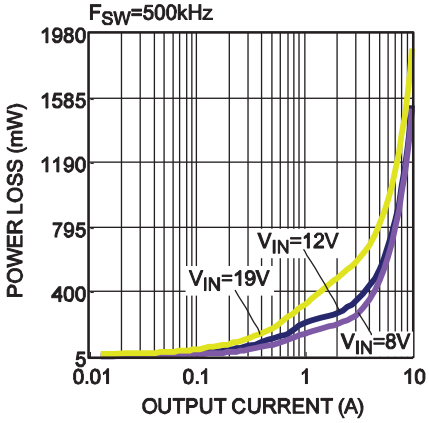
Efficiency vs. Output Current



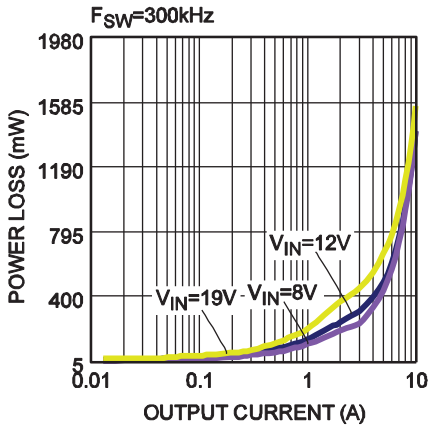
Efficiency vs. Output Current



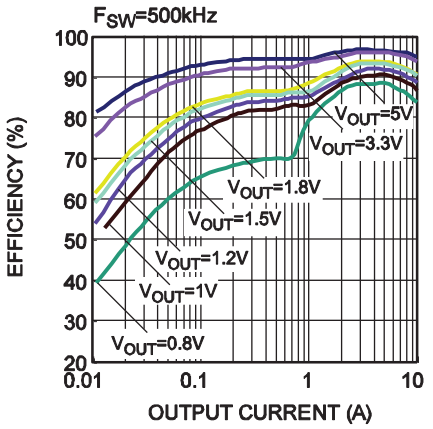
Power Loss vs. Output Current



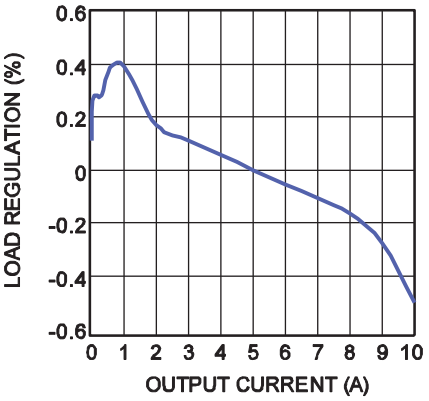
Power Loss vs. Output Current



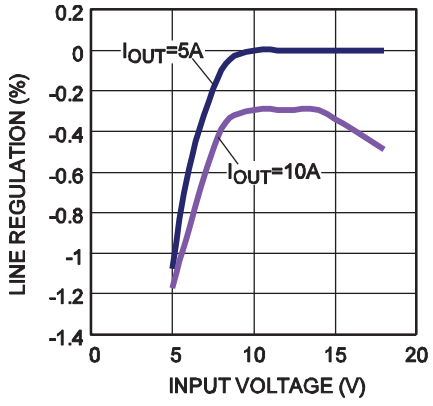
Efficiency vs. Output Current



Load Regulation



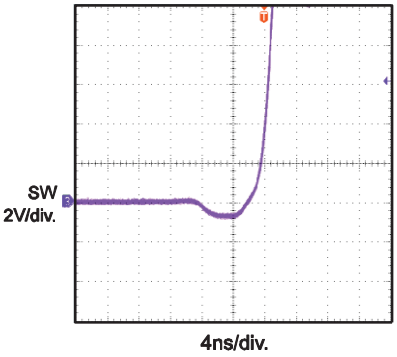
Line Regulation vs. Input Voltage



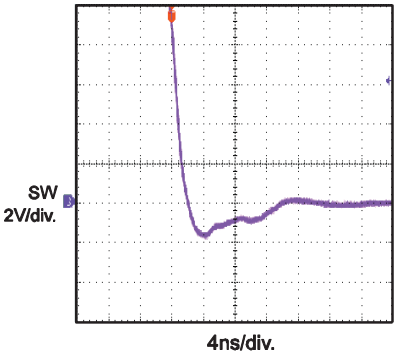
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8632GLE-10, V_{IN}=12V, V_{OUT} =1V, L=1µH, T_A=+25°C, unless otherwise noted.

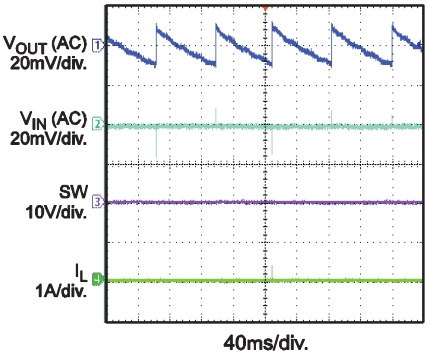
Dead Time (on)
I_{OUT} = 10A



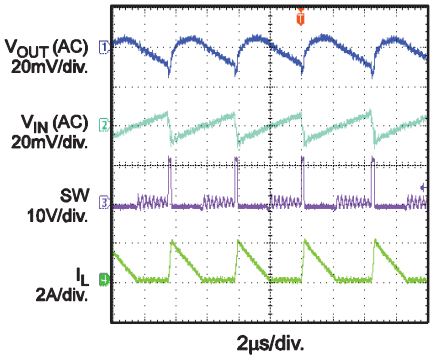
Dead Time (off)
I_{OUT} = 10A



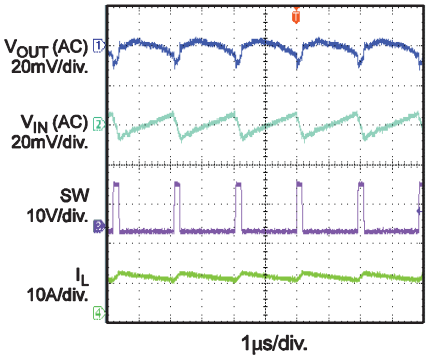
Input/Output Voltage Ripple
I_{OUT} = 0A



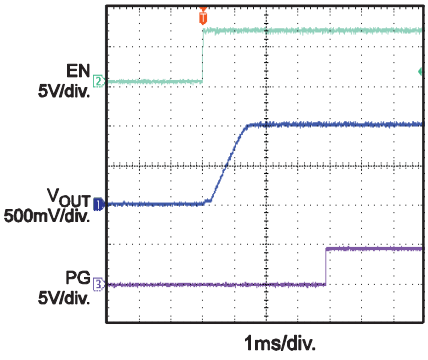
Input/Output Voltage Ripple
I_{OUT} = 0.5A



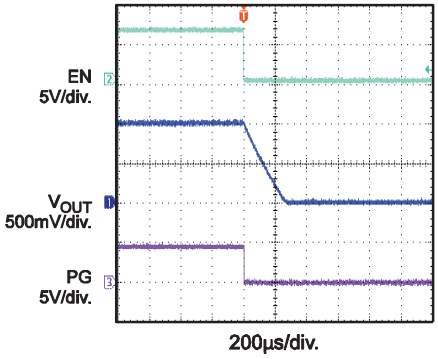
Input/Output Voltage Ripple
I_{OUT} = 10A



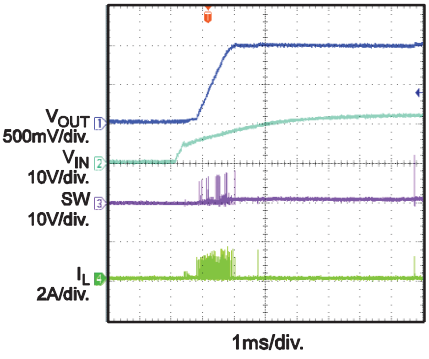
Power Good through EN Start Up
I_{OUT} = 0.5A, C_{SS} = 33nF,



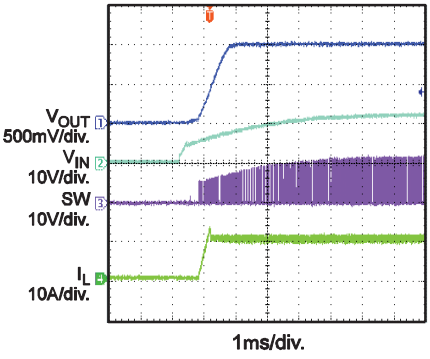
Power Good through EN Shutdown
I_{OUT} = 0.5A, C_{SS} = 33nF,



Start Up Through V_{IN}
I_{OUT} = 0A



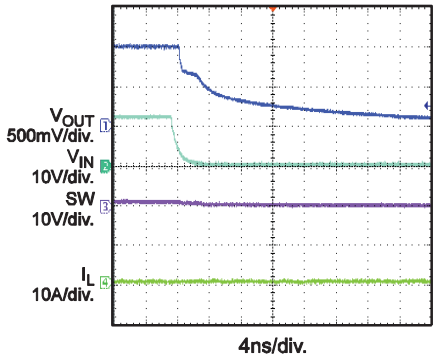
Start Up Through V_{IN}
I_{OUT} = 10A



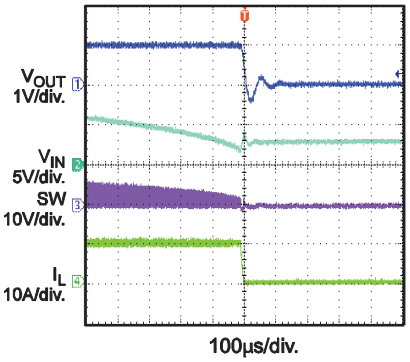
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8632GLE-10, V_{IN}=12V, V_{OUT} =1V, L=1µH, T_A=+25°C, unless otherwise noted.

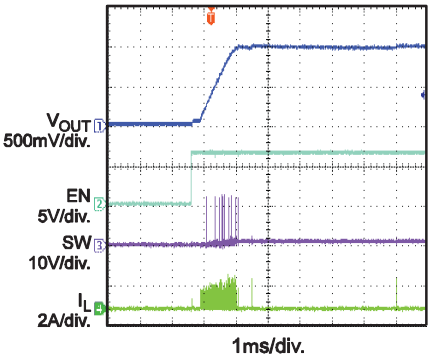
Shutdown Through V_{IN}
I_{OUT} = 0A



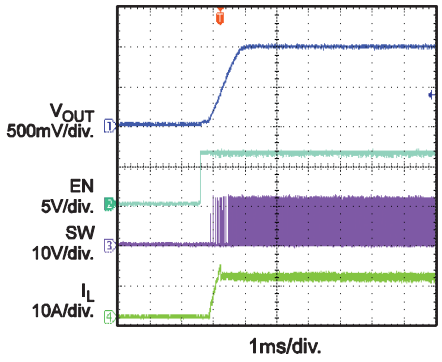
Shutdown Through V_{IN}
I_{OUT} = 10A



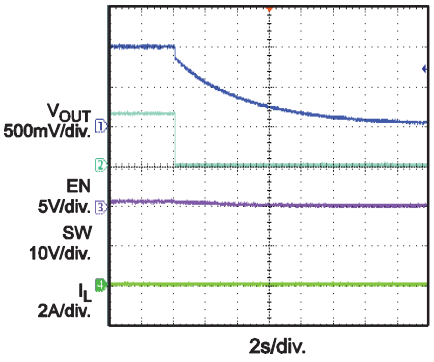
Start up through EN
I_{OUT} = 0A



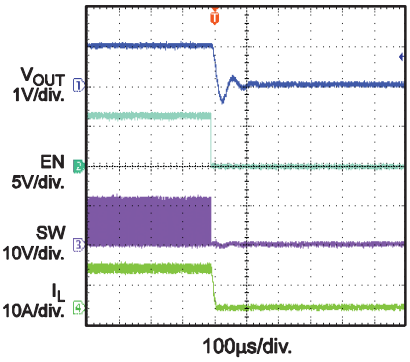
Start up through EN
I_{OUT} = 10A



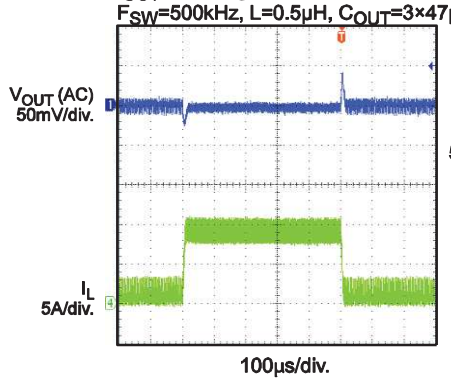
Shutdown Through EN
I_{OUT} = 0A



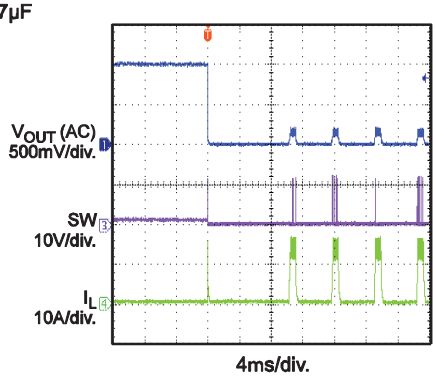
Shutdown Through EN
I_{OUT} = 10A



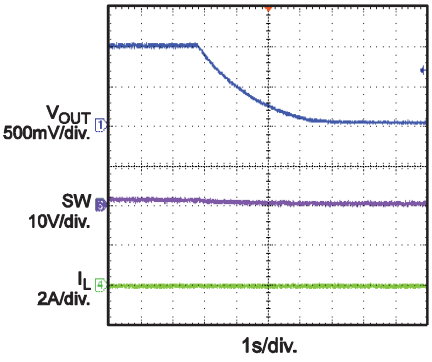
Transient
V_{IN} = 12V, V_{OUT} = 1V,
I_{OUT} = 1-9A @1.6A/µs,
F_{SW}=500kHz, L=0.5µH, C_{OUT}=3×47µF



Short Circuit Protection



Thermal Shutdown
I_{OUT} = 0A

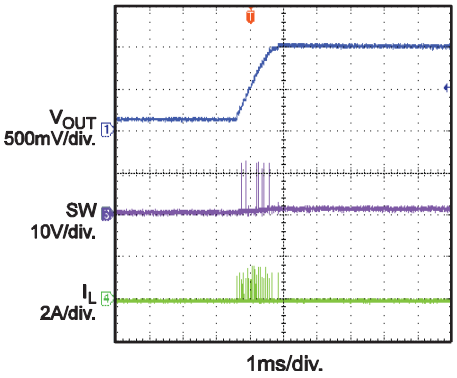


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8632GLE-10, V_{IN}=12V, V_{OUT} =1V, L=1µH, T_A=+25°C, unless otherwise noted.

Thermal Recovery

I_{OUT} = 0A



BLOCK DIAGRAM

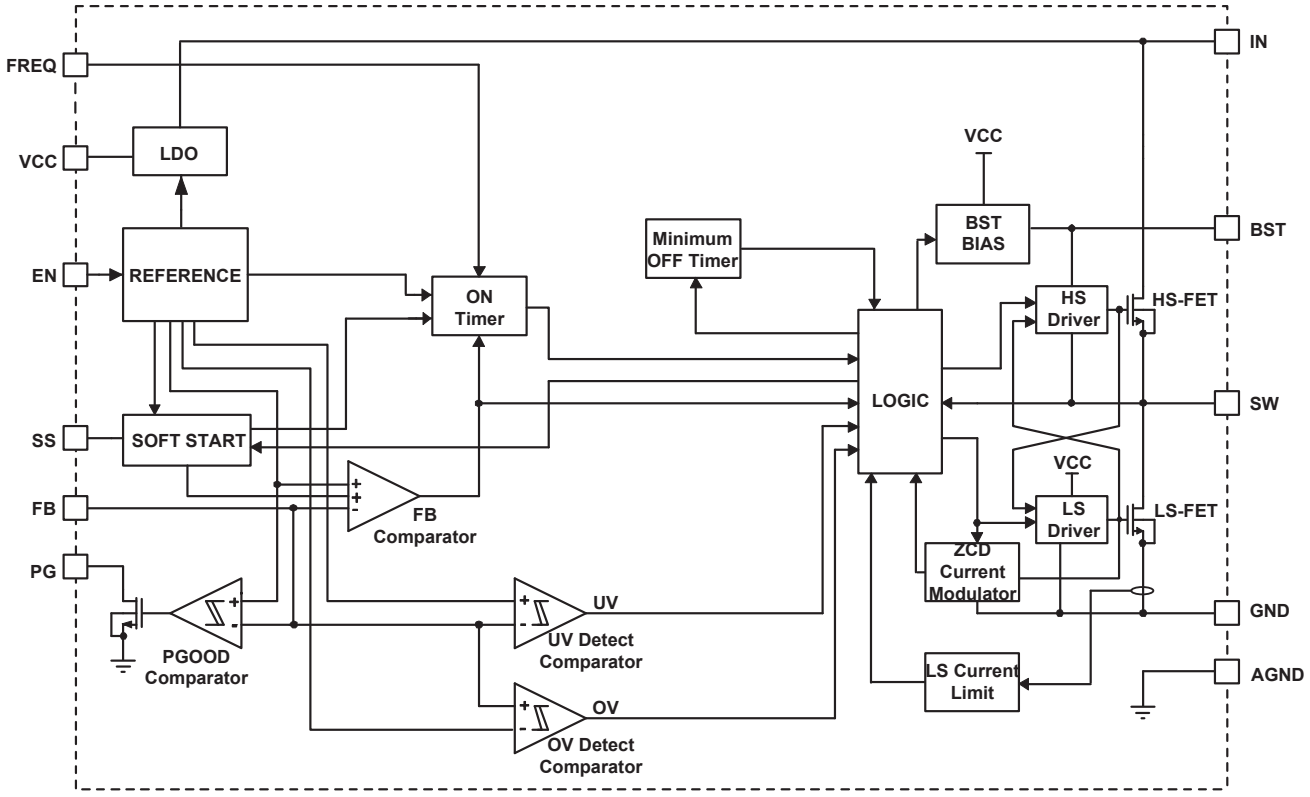


Figure 1—Functional Block Diagram

OPERATION

PWM Operation

The MPQ8632 is a fully integrated synchronous rectified step-down switch mode converter. It uses Constant-on-time (COT) control to provide a fast transient response and ease loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The input voltage and the frequency-set resistor determine the ON period as follows:

$$T_{ON}(ns) = \frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \quad (1)$$

After the ON period elapses, the HS-FET turns off. It turns ON again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is OFF to minimize the conduction loss. There is a dead short (or shoot-through) between input and GND if both HS-FET and LS-FET turn on at the same time. A dead-time (DT) internally generated between HS-FET OFF and LS-FETON, or LS-FET OFF and HS-FET ON avoids shoot-through.

Heavy-Load Operation

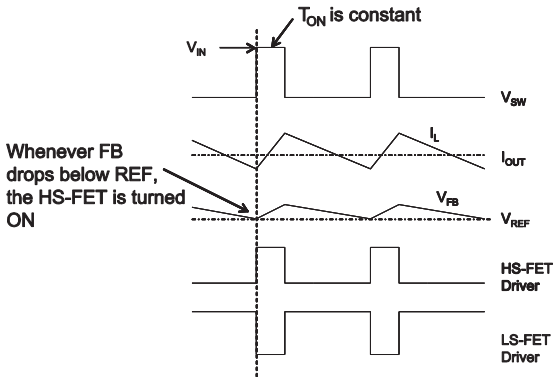


Figure 2—Heavy Load Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). Figure 2 shows the CCM operation. When V_{FB} is below V_{REF}, HS-FET turns on for a fixed interval determined by the one- shot on-timer as per equation 1. When the HS-FET turns off, the LS-FET turns on until the next period.

In CCM operation, the switching frequency is fairly constant and is also called PWM mode.

Light-Load Operation

As the load decreases, the inductor current decreases too. When the inductor current touches zero, the operation is transited from continuous-conduction-mode (CCM) to discontinuous-conduction-mode (DCM).

Figure 3 shows the light load operation. When V_{FB} drops below V_{REF}, HS-FET turns on for a fixed interval determined by the one- shot on-timer as per equation 1. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero. A current modulator takes over the control of LS-FET and limits the inductor current less than -1mA. Hence, the output capacitors discharge slowly to GND through LS-FET. As a result, this mode improves greatly the light load efficiency. At light load condition, the HS-FET does not turns ON as frequently as at heavy load condition. This is called skip mode.

At light load or no load condition, the output drops very slowly and the MPQ8632 reduces the switching frequency naturally and then achieves high efficiency at light load.

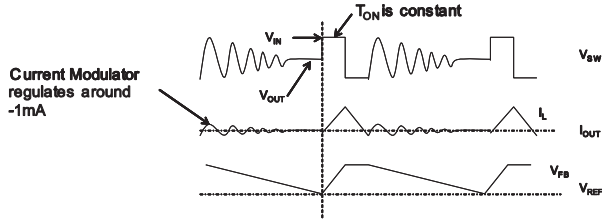


Figure 3—Light Load Operation

As the output current increases from the light load condition, the current modulator regulates the operating period that becomes shorter. The HS-FET turns ON more frequently. Hence, the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time decreases to zero. Determine the critical output current level as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (2)$$

Where F_{SW} is the switching frequency.

The IC turns into PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Switching Frequency

Selecting the switching frequency requires trading off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values to minimize the output voltage ripple.

For MPQ8632，set the on time using the FREQ pin to set the frequency for steady state operation at CCM.

The MPQ8632 uses adaptive constant-on-time (COT) control, though the IC lacks a dedicated oscillator. Connect the FREQ pin to the IN pin through the resistor (R_{FREQ}) so that the input voltage is feed-forwarded to the one-shot on-time timer. When operating in steady state at CCM, the duty ratio stays at V_{OUT}/V_{IN}, so the switching frequency is fairly constant over the input voltage range. Set the switching frequency as follows:

$$F_{SW}(kHz) = \frac{10^6}{\frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (3)$$

Where T_{DELAY} is the comparator delay of about 5ns.

Typically, the MPQ8632 is set to 200kHz to 1MHz applications. It is optimized to operate at high switching frequencies at high efficiency: high switching frequencies allow for physically smaller LC filter components to reduce the PCB footprint.

Jitter and FB Ramp Slope

Figure 4 and Figure 5 show jitter occurring in both PWM mode and skip mode. When there is noise on the V_{FB} descending slope, the HS-FET ON time deviates from its intended point and produces jitter and influences system stability. The V_{FB} ripple's slope steepness dominates the noise immunity though its magnitude has no direct effect.

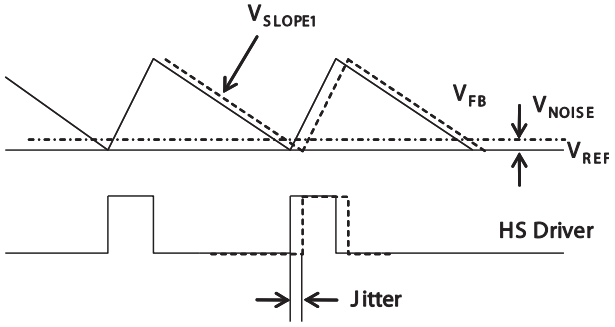


Figure 4—Jitter in PWM Mode

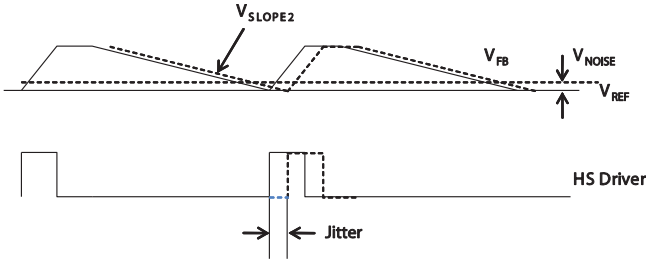


Figure 5—Jitter in Skip Mode

Ramp with a Large ESR Capacitor

Using POSCAPs or other large-ESR capacitors as the output capacitor results in the ESR ripple dominating the output ripple. The ESR also significantly influences the V_{FB} slope. Figure 6 shows the simplified equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit.

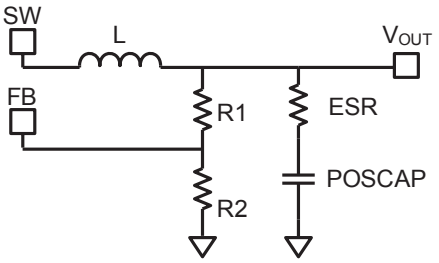


Figure 6—Simplified Circuit in PWM Mode without External Ramp Compensation

To realize the stability without an external ramp, usually select the ESR value as follows:

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2}}{C_{OUT}} \quad (4)$$

Where T_{SW} is the switching period.

Ramp with a Small ESR Capacitor

Use an external ramp when using ceramic output capacitors, because the ESR ripple is not high enough to stabilize the system.

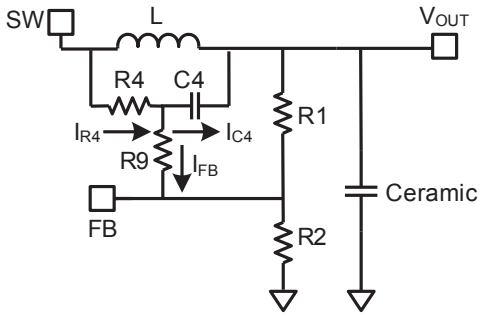


Figure 7—Simplified Circuit in PWM Mode with External Ramp Compensation

Figure 7 shows the simplified circuit in PWM mode with the HS-FET OFF and an external ramp compensation circuit (R4, C4). Design the external ramp based on the inductor ripple current. Select C4, R9, R1 and R2 to meet the following condition:

$$\frac{1}{2\pi \times F_{SW} \times C4} < \frac{1}{5} \times \left(\frac{R1 \times R2}{R1 + R2} + R9 \right) \quad (5)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (6)$$

Then estimate the ramp on V_{FB} as:

$$V_{RAMP} = \frac{V_{IN} - V_{OUT}}{R4 \times C4} \times T_{ON} \times \left(\frac{R1 // R2}{R1 // R2 + R9} \right) \quad (7)$$

The V_{FB} ripple's descending slope then follows:

$$V_{SLOPE1} = \frac{V_{RAMP}}{T_{OFF}} = \frac{-V_{OUT}}{R4 \times C4} \quad (8)$$

Equation 8 shows that if there is instability in PWM mode, reduce either R4 or C4. If C4 is irreducible due to equation 5 limitations, then reduce R4. For a stable PWM operation, design V_{slope1} based on equation 9.

$$-V_{SLOPE1} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2} - R_{ESR} \times C_{OUT}}{2 \times L \times C_{OUT}} \times V_{OUT} + \frac{I_{OUT} \times 10^{-3}}{T_{SW} - T_{ON}} \quad (9)$$

Where I_{OUT} is the load current.

In skip mode, The V_{FB} ripple's descending slope is almost same whether the external ramp is used or not. Figure 8 shows the simplified circuit in skip mode when both the HS-FET and LS-FET are off.

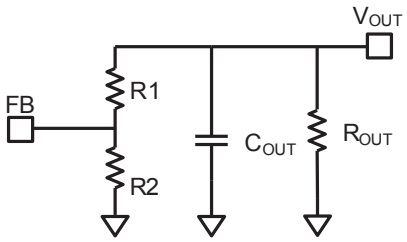


Figure 8—Simplified Circuit in skip Mode

Determine the V_{FB} ripple's descending slope in skip mode as follows:

$$V_{SLOPE2} = \frac{-V_{REF}}{[(R1 + R2) // R_{OUT}] \times C_{OUT}} \quad (10)$$

Where R_{OUT} is the equivalent load resistor.
Figure 5 shows that V_{SLOPE2} in skip mode is lower than that is in PWM mode, so it is

reasonable that the jitter in skip mode is larger To achieve less jitter during ultra light load condition, reduce R1 and R2, but that will decrease the light load efficiency.

Configuring the EN Control

The regulator turns on when En goes high; conversely it turns off when EN goes low. Do not float the pin.

For automatic start-up, pull the EN pin up to input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from the IN pin to the EN pin) and the pull-down resistor (R_{DOWN} from the EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.5 \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}} (V) \quad (11)$$

For example, for R_{UP}=100kΩ and R_{DOWN}=51kΩ, the $V_{IN-START}$ is set at 4.44V.

To reduce noise, add a 10nF ceramic capacitor from EN to GND.

An internal zener diode on the EN pin clamps the EN pin voltage to prevent run away. The maximum pull up current assuming the worst case 6V for the internal zener clamp should be less than 1mA.

Therefore, when driving EN with an external logic signal, use an EN voltage less than 6V. When connecting EN to IN through a pull-up resistor or a resistive voltage divider, select a resistance that ensures a maximum pull-up current less than 1mA.

If using a resistive voltage divider and V_{IN} exceeds 6V, then the minimum resistance for the pull-up resistor R_{UP} should meet:

$$\frac{V_{IN} - 6V}{R_{UP}} - \frac{6V}{R_{DOWN}} \le 1mA \quad (12)$$

With only R_{UP} (the pull-down resistor, R_{DOWN}, is not connected), then the VCC UVLO threshold determines $V_{IN-START}$, so the minimum resistor value is:

$$R_{UP} \ge \frac{V_{IN} - 6V}{1mA} (\Omega) \quad (13)$$

A typical pull-up resistor is 100kΩ.

External VCC bias

An external 5V VCC bias can disable the internal LDO, in this case, Vin can be as low as 2.5V.

Soft Start

The MPQ8632 employs a soft start (SS) mechanism to ensure a smooth output during power-up. When the EN pin goes high, an internal current source (20μA) charges the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the REF voltage, it continues ramping up while V_{REF} takes over the PWM comparator. At this point, soft start finishes and the device enters steady state operation.

Determine the SS capacitor value as follows:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (14)$$

If the output capacitors are large, then avoid setting a short SS time or risk hitting the current limit during SS. Use a minimum value of 4.7nF if the output capacitance value exceeds 330μF.

Pre-Bias Startup

The MPQ8632 has been designed for monotonic startup into pre-biased loads. If the output is pre-biased to a certain voltage during startup, the IC will disable switching for both high-side and low-side switches until the voltage on the soft-start capacitor exceeds the sensed output voltage at the FB pin.

Power Good (PG)

The MPQ8632 has a power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect it to VCC or some other voltage source that measures less than 5.5V through a pull-up resistor (typically 100kΩ). After applying the input voltage, the MOSFET turns on so that the PG pin is pulled to GND before the SS is ready. After the FB voltage reaches 91% of the REF voltage, the PG pin is pulled high after a 2.5ms delay.

When the FB voltage drops to 80% of the REF voltage or exceeds 120% of the nominal REF voltage, the PG pin is pulled low.

If the input supply fails to power the MPQ8632, the PG pin is also pulled low even though this pin is tied to an external DC source through a pull-up resistor (typically 100kΩ).

Over-Current Protection (OCP)

The MPQ8632 features three current limit levels for over-current conditions: high-side peak current limit, low-side valley current limit and low-side negative current limit.

However, the OCP operation mechanism of MPQ8632GL-10 is different from other parts in this family.

For MPQ8632GLE-10:

High-Side Peak Current Limit: The part has a cycle-by-cycle over-current limiting function. The device monitors the inductor current during the HS-FET ON state. When the sensed inductor current hits the peak current limit, the output over-current comparator goes high, the device enters OCP mode immediately and turns off the HS-FET and turns on the LS-FET.

Low-Side Valley Current Limit: The device also monitors the inductor current during the LS-FET ON state. When ILIM=1 and at the end of the OFF time, the LS-FET sourcing current is compared to the internal positive-valley–current limit. If the valley current limit is less than the LS-FET sourcing current, the HS-FET remains OFF and the LS-FET remains ON for the next ON time. When the LS-FET sourcing current drops below the valley current limit, the HS-FET turns on again.

For other parts except MPQ8632GLE-10:

These parts enter OCP mode if only the LS-FET sourcing valley current exceeds the valley current limit. Once the OCP is triggered, the LS-FET keeps ON state until the LS-FET sourcing valley current is less than the valley current limit. And then the LS-FET turns off, the HS-FET turns on for a fixed time determined by frequency-set resistor R_{FREQ} and input voltage.

During OCP, the device tries to recover from the over-current fault with hiccup mode: the chip disables the output power stage, discharges the soft-start capacitor and then automatically retries soft-start. If the over-current condition still holds after soft-start ends, the device repeats this operation cycle until the over-current conditions disappear and then output rises back to regulation level. OCP offers non-latch protection.

Low-Side Negative Current Limit: If the sensed LS-FET negative current exceeds the negative current limit, the LS-FET turns off immediately and stays OFF for the remainder of the OFF period. In this situation, both MOSFETs are OFF until the end of a fixed interval. The HS-FET body diode conducts the inductor current for the fixed time.

Over -Voltage Protection (OVP)

The MPQ8632 monitors the output voltage using the FB pin connected to the tap of a resistor divider to detect over-voltage. MPQ8632 and MPQ8632H provide non-latch and latch off OVP mode as showed in Table 1.

Table 1—OVP Mode

OVP Mode	Non-Latch Mode	Latch-Off Mode
Part #	MPQ8632-4 MPQ8632-6 MPQ8632-8 MPQ8632H-10 MPQ8632-12 MPQ8632-15 MPQ8632-20	MPQ8632-10

For MPQ8632GLE-10:

If the FB voltage exceeds the nominal REF voltage but remains lower than 120% of the REF voltage (0.611V), both MOSFETs are off.

If the FB voltage exceeds 120% of the REF voltage but remains below 130%, the LS-FET turns on while the HS-FET remains off. The LS-FET remains on until the FB voltage drops below 110% of the REF voltage or the low-side negative current limit is hit.

If the FB voltage exceeds 130% of the REF voltage, then the device is latched off. Need cycle the input power supply or EN to restart.

For other parts except MPQ8632GLE-10:

Even the FB voltage exceeds 130% of the REF voltage, these parts enter a non-latch off mode. Once the FB voltage comes back to the reasonable value, they will exit this OVP mode and operate normally again.

UVLO protection

The MPQ8632 has under-voltage lock-out protection (UVLO). When the VCC voltage exceeds the UVLO rising threshold voltage, the MPQ8632 powers up. It shuts off when the VCC voltage falls below the UVLO falling threshold voltage. This is non-latch protection.

The MPQ8632 is disabled when the VCC voltage falls below 3.3 V. If an application requires a higher UVLO threshold, use the two external resistors connected to the EN pin as shown in Figure 9 to adjust the startup input voltage. For best results, use the enable resistors to set the input voltage falling threshold (V_{STOP}) above 3.6 V. Set the rising threshold (V_{START}) to provide enough hysteresis to account for any input supply variations.

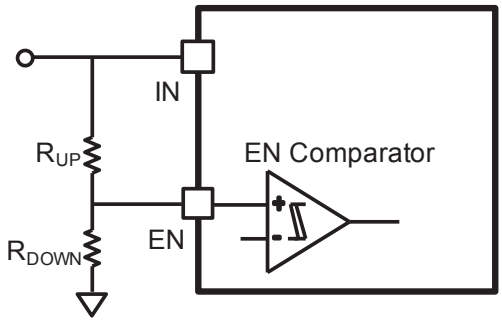


Figure 9—Adjustable UVLO Threshold

Thermal Shutdown

The MPQ8632 has thermal shutdown. The IC internally monitors the junction temperature. If the junction temperature exceeds the threshold value (minimum 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a soft startup.

APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Capacitors

For applications that electrolytic capacitor or POS capacitor with a large ESR is set as output capacitors. The feedback resistors—R1 and R2 as shown in Figure 10—set the output voltage.

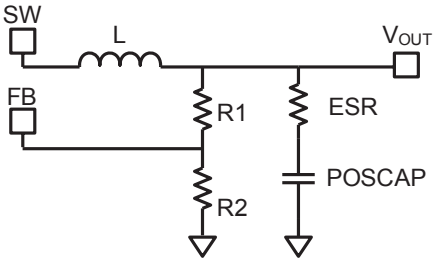


Figure10—Simplified POSCAP Circuit

First, choose a value for R2 that balances between high quiescent current loss (low R2) and high noise sensitivity on FB (high R2). A typical value falls within 5kΩ to 50kΩ, using a comparatively larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. Then calculate R1 as follows, which considers the output ripple:

$$R1 = \frac{V_{OUT} - \frac{1}{2} \times \Delta V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (15)$$

Where ΔV_{OUT} is the output ripple determined by equation 24.

Setting the Output Voltage-Small ESR Capacitors

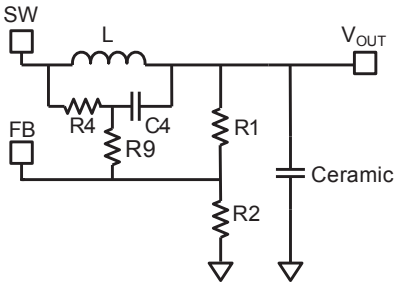


Figure11—Simplified Ceramic Capacitor Circuit

When using a low ESR ceramic capacitor on the output, add an external voltage ramp to the FB pin consisting of R4 and C4.The ramp voltage, V_{RAMP}, and the resistor divider influence the output voltage as shown in Figure 11. Calculate V_{RAMP} as shown in equation 7. Select R2 to balance between high quiescent current loss and FB noise sensitivity. Choose R2 within 5kΩ to 50kΩ, using a larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. Determine the value of R1 as follows:

$$R1 = \frac{R2}{\frac{V_{FB(AVG)}}{V_{OUT} - V_{FB(AVG)}} - \frac{R2}{R4 + R9}} \quad (16)$$

Where $V_{FB(AVG)}$ is the average FB voltage. $V_{FB(AVG)}$ varies with the V_{IN}, V_{OUT}, and load condition, where the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$; improving the load or line regulation involves a lower V_{RAMP} that meets equation 9.

For PWM operation, estimate $V_{FB(AVG)}$ from equation 17.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} \times V_{RAMP} \times \frac{R1 // R2}{R1 // R2 + R9} \quad (17)$$

Usually, R9 is 0Ω, though it can also be set following equation 18 for better noise immunity. It should also be less than 20% of R1//R2 to minimize its influence on V_{RAMP}.

$$R9 < \frac{1}{5} \times \frac{R1 \times R2}{R1 + R2} \quad (18)$$

Using equations 16 and 17 to calculate the output voltage can be complicated. To simplify the R1 calculation in equation 16, add a DC-blocking capacitor, C_{DC}, to filter the DC influence from R4 and R9. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. The addition of this capacitor, simplifies the R1 calculation as per equation 19 for PWM mode operation.