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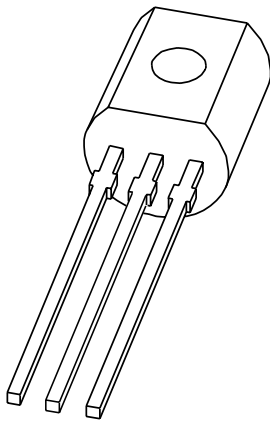
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DATA SHEET



MPSA64 PNP Darlington transistor

Product specification
Supersedes data of 1997 Apr 23

1999 Apr 27

PNP Darlington transistor

MPSA64

FEATURES

- Low current (max. 500 mA)
- Low voltage (max. 30 V)
- High DC current gain (min. 10000).

APPLICATIONS

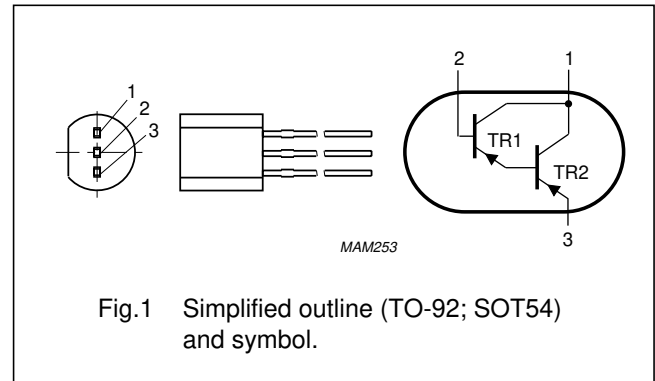
- High gain amplification.

DESCRIPTION

PNP Darlington transistor in a TO-92; SOT54 plastic package. NPN complement: MPSA14.

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–30	V
V_{CES}	collector-emitter voltage	$V_{BE} = 0$	–	–30	V
V_{EBO}	emitter-base voltage	open collector	–	–10	V
I_C	collector current (DC)		–	–500	mA
I_{CM}	peak collector current		–	–1	A
I_B	base current (DC)		–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$
T_{amb}	operating ambient temperature		–65	+150	$^\circ\text{C}$

Note

1. Transistor mounted on an FR4 printed-circuit board.

PNP Darlington transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	250	K/W

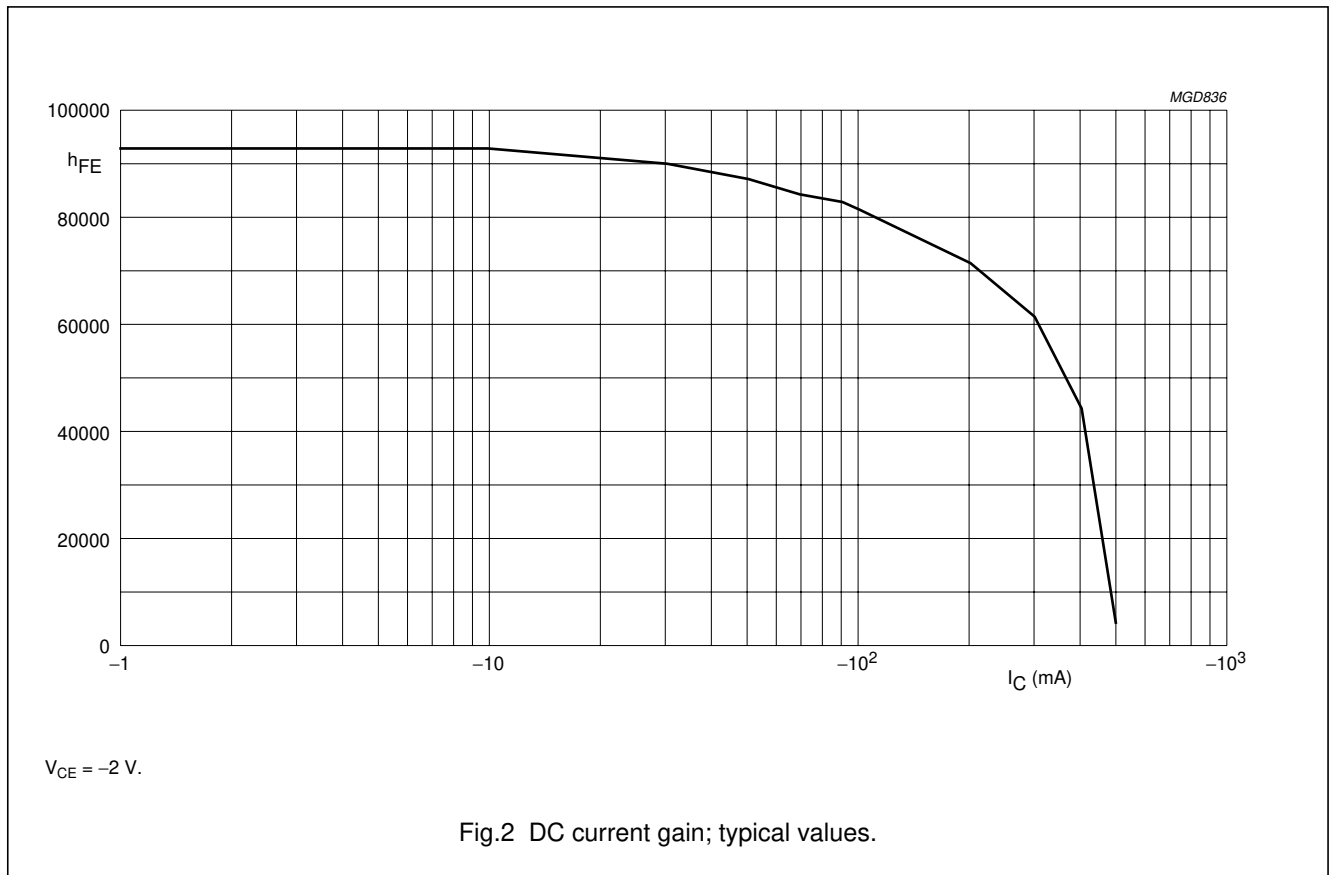
Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = -30\text{ V}$	-	-100	nA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = -10\text{ V}$	-	-100	nA
h_{FE}	DC current gain	$I_C = -10\text{ mA}; V_{CE} = -5\text{ V}; \text{ see Fig.2}$	10000	-	
		$I_C = -100\text{ mA}; V_{CE} = -5\text{ V}; \text{ see Fig.2}$	20000	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -0.1\text{ mA}$	-	-1.5	V
V_{BEsat}	base-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -0.1\text{ mA}$	-	-1.5	V
V_{BEon}	base-emitter on-state voltage	$I_C = -100\text{ mA}; V_{CE} = -5\text{ V}$	-	-2	V
f_T	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	125	-	MHz



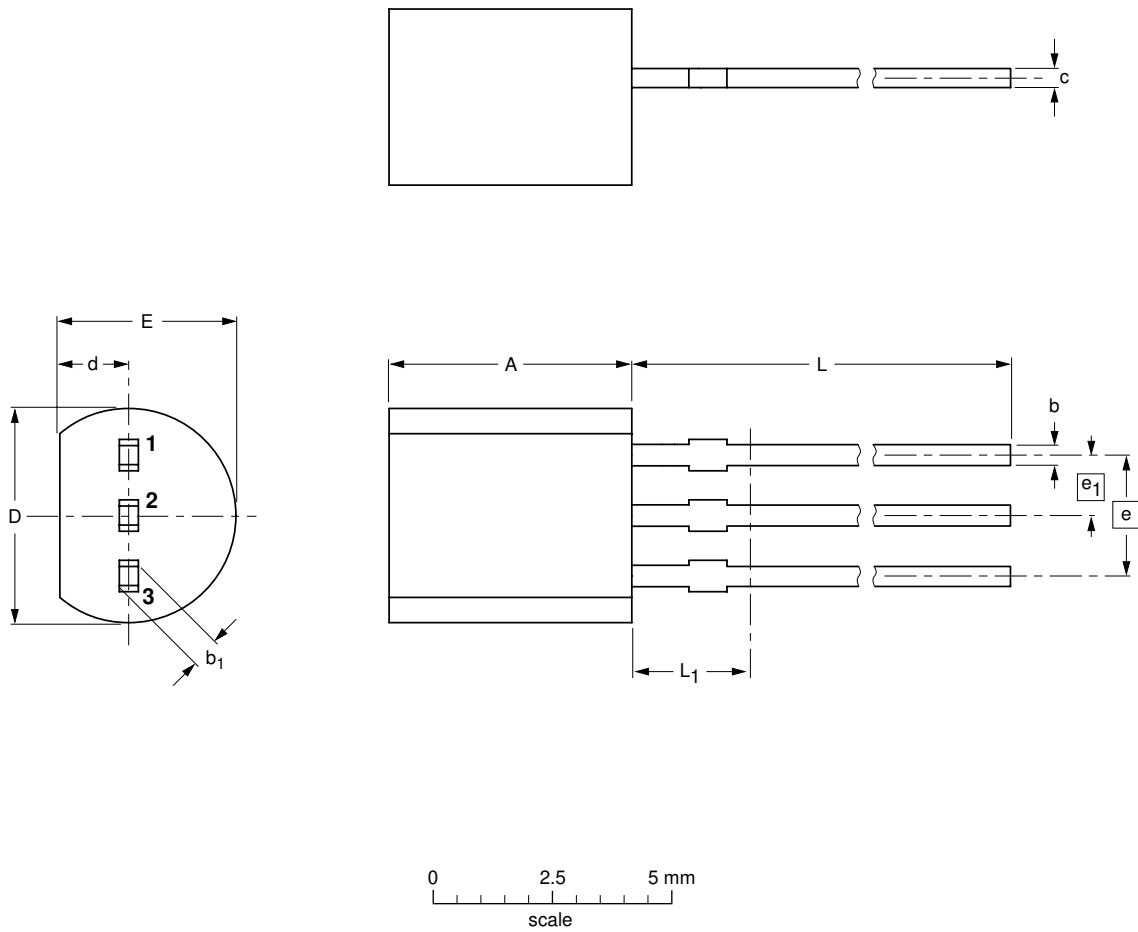
PNP Darlington transistor

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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54		TO-92	SC-43		97-02-28

PNP Darlington transistor

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

PNP Darlington transistor

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