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MPU-3050
Motion Processing Unit
Product Specification

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TABLE OF CONTENTS

1 Introduction

1.1 Purpose and Scope

This document provides a description, specifications, and design-related information for the MPU-3050 Motion Processing Unit ®. References [1], [2] and [3] provide a complementary set of software guides for the Motion Processing Library (MPL) and describe in detail the API and System Layer routines needed for interfacing to the MPU-3050.

Electrical characteristics are based upon simulation results and limited characterization data. Specifications are subject to change without notice.

1.2 Product Overview

The MPU-3050 Motion Processing Unit (MPU) is the world's first motion processing solution with integrated 6-axis sensor fusion for smartphone applications. The MPU-3050 has an embedded 3-axis gyroscope and Digital Motion Processor ® (DMP) hardware accelerator engine with a secondary I^2C port that interfaces to third party digital accelerometers to deliver a complete 6-axis sensor fusion output to its primary I^2C port. This combines both linear and rotational motion into a single data stream for the application. This breakthrough in gyroscope technology provides a dramatic 68% smaller footprint, 40% thinner package, consumes 55% less power, and has inherent cost advantages compared to the latest competitive gyro solutions to uniquely address the fast-growing demand for 6-axis motion processing in mobile handsets.

The MPU-3050 significantly extends and transforms motion sensing features provided by accelerometers beyond portrait and landscape orientation, to motion processing functionality. The MPU measures and processes both linear and rotational movements, creating a higher degree of 1:1 motion interactivity between the user and their handset. Similar to the proliferation of Bluetooth, camera phone image sensors and Wi-Fi, motion processing is becoming a "must-have" function in mobile handsets benefitting wireless carriers, mobile handset OEMs, application developers and end-users. By providing an integrated sensor fusion output, the DMP in the MPU-3050 offloads the intensive motion processing computation requirements from the applications processor, reducing the need for frequent polling of the motion sensor output and enabling use of low-cost, low-power application processors, thereby increasing overall battery life of handsets. Since handsets today are of multi-function nature, MPU-3050 not only provides accurate 1:1 motion tracking for some of the more common applications such as still/video image stabilization, gaming and dead reckoning, the 32-bit DMP can be programmed to deliver advanced UI, e.g. multiple kinds of gestures and character recognition leading to applications such as *Airsign* ®, *TouchAnywhere* ®, *MotionCommand* ®.

By leveraging its patented and volume-proven Nasiri-Fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the MPU-3050 package size down to a revolutionary footprint of 4x4x0.9mm (QFN), while providing the highest performance, lowest noise, and the lowest cost semiconductor packaging to address a wide range of handheld consumer electronic devices.

The MPU-3050 integrates 16-bit analog-to-digital converters (ADCs), selectable low-pass filters, FIFO, embedded temperature sensor, and Fast Mode I^2C interface. Performance features include programmable full-scale range from 250 degrees-per-second up to 2000 degrees-per-second (º/s or dps), and low-noise of 0.01º/s/√Hz, while providing the highest robustness supporting 10,000*g* shock in operation. The highest cross-axis isolation is achieved by design from its single silicon integration. Factory-calibrated initial sensitivity reduces production-line calibration requirements. The part's on-chip FIFO and dedicated I^2C-master accelerometer sensor bus simplifies system timing and lowers system power consumption. The sensor bus allows the MPU-3050 to directly acquire data from the off-chip

[1] MPL Programmer's Guide – Application Note (AN-MPL-3000-UG-01 or later)
[2] MPL Functional Specification (DOC-MPL-FS-V2.3 or later)
[3] MPL Product Specification (PS-MPL-3000-v2.0 or later)

accelerometer without intervention from an external processor. Other industry-leading features include a small 4 mm x 4 mm x 0.9 mm plastic QFN package, an embedded temperature sensor, programmable interrupts, and a low 13 mW power consumption. Parts are available with I²C serial interface, a VDD operating range of 2.1 V to 3.6 V, and a VLOGIC interface voltage from 1.71 V to 3.6 V.

The MPU-3050 supports the I²C serial interface and has a separate VLOGIC reference pin (in addition to its analog supply pin, VDD), which sets the logic levels of its I²C interface. The VLOGIC voltage may be between 1.71 V min to VDD max. The table below outlines these details:

Power Supply and supported interface for MPU-3050

Part / Item	MPU-3050
VDD	2.1 V to 3.6 V
VLOGIC	1.71 V to VDD
Serial Interfaces Supported	I²C
Pin 8	VLOGIC
Pin 9	AD0
Pin 23	SCL
Pin 24	SDA

1.3 Applications

- Handset gaming
- Location-based services, points of interest, and dead reckoning
- Improved camera image quality through image stabilization
- Health and sports monitoring

2 Features

The MPU-3050 Motion Processing Unit includes a wide range of features:

2.1 Sensors

- X-, Y-, Z-Axis angular rate sensors (gyros) on one integrated circuit
- Digital-output temperature sensor
- External sync signal connected to the FSYNC pin supports image, video and GPS synchronization
- 6-axis motion processing capability using secondary I^2C interface to directly connect to a digital 3-axis third-party accelerometer
- Factory calibrated scale factor
- High cross-axis isolation via proprietary MEMS design
- 10,000*g* shock tolerant

2.2 Digital Output

- Fast Mode (400 kHz) I^2C serial interface
- 16-bit ADCs for digitizing sensor outputs
- Angular rate sensors (gyros) with applications-programmable full-scale-range of ±250°/sec, ±500°/sec, ±1000°/sec, or ±2000°/sec.

2.3 Motion Processing

- Embedded Digital Motion Processing engine supports 3D motion processing and gesture recognition algorithms
- When used together with a digital 3-axis third party accelerometer, the MPU-3050 collects the accelerometer data via a dedicated interface, while synchronizing data sampling at a user defined rate. The total data set obtained by the MPU-3050 includes 3-axis gyroscope data and 3-axis accelerometer data, temperature data, and the one bit external sync signal connected to the FSYNC pin. The MPU also downloads the results calculated by the digital 3-axis third party accelerometer internal registers.
- FIFO buffers complete data set, reducing timing requirements on the system processor and saving power by letting the processor burst read the FIFO data, and then go into a low-power sleep mode while the MPU collects more data.
- Programmable interrupt supports features such as gesture recognition, panning, zooming, scrolling, zero-motion detection, tap detection, and shake detection
- Hand jitter filter
- Programmable low-pass filters
- Feature extraction for peak and zero-crossing detection
- Pedometer functionality

2.4 Clocking

- On-chip timing generator clock frequency +/-2% over full temperature range
- Optional external clock inputs of 32.768kHz or 19.2 MHz
- 1 MHz clock output to synchronize with digital 3-axis accelerometer

2.5 Power

- VDD supply voltage range of 2.1 V to 3.6 V
- Flexible VLOGIC reference voltage allows for multiple I^2C interface voltage
- Power consumption with all three axis and DMP active: 6.1 mA
- Sleep mode: 5 µA
- Each axis can be individually powered down

2.6 Package

- 4 x 4 x 0.9 mm QFN plastic package
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 Electrical Characteristics

3.1 Sensor Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5 V, VLOGIC = 2.5 V, T_A=25°C.

Parameter	Conditions	Min	Typical	Max	Unit	Notes
GYRO SENSITIVITY						
Full-Scale Range	FS_SEL = 0		±250		º/s	4, 7
	FS_SEL = 1		±500			4, 7
	FS_SEL = 2		±1000			4, 7
	FS_SEL = 3		±2000			4, 7
Gyro ADC Word Length			16		Bits	3
Sensitivity Scale Factor	FS_SEL = 0		131		LSB/(º/s)	1
	FS_SEL = 1		65.5			3
	FS_SEL = 2		32.8			3
	FS_SEL = 3		16.4			3
Sensitivity Scale Factor Tolerance	25°C	-6	±2	+6	%	1
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±2		%	8
Nonlinearity	Best fit straight line; 25°C		0.2		%	6
Cross-Axis Sensitivity			2		%	6
GYRO ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±20		º/s	1
ZRO Variation Over Temperature	-40°C to +85°C		±0.15		º/s/°C	8
Power-Supply Sensitivity (1-10 Hz)	Sine wave, 100mVpp; VDD = 2.2 V		0.2		º/s	5
Power-Supply Sensitivity (10 – 250 Hz)	Sine wave, 100mVpp; VDD = 2.2 V		0.2		º/s	5
Power-Supply Sensitivity (250 Hz – 100 kHz)	Sine wave, 100mVpp; VDD = 2.2 V		4		º/s	5
Linear Acceleration Sensitivity	Static		0.1		º/s/*g*	6
GYRO NOISE PERFORMANCE	**FS_SEL=0**					
Total RMS Noise	DLPFCFG = 2 (100 Hz)		0.1		º/s-rms	1
Low-frequency RMS noise	Bandwidth 1 Hz to 10 Hz		0.033		º/s-rms	1
Rate Noise Spectral Density	At 10 Hz		0.01		º/s/√Hz	3
GYRO MECHANICAL FREQUENCIES						
X-Axis		30	33	36	kHz	1
Y-Axis		27	30	33	kHz	1
Z-Axis		24	27	30	kHz	1
GYRO START-UP TIME	**DLPFCFG = 0**					
ZRO Settling	to ±1º/s of Final		50		ms	5
TEMPERATURE RANGE						
Specified Temperature Range		-40		85	ºC	2

Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Based on design, through modeling and simulation across PVT
4. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
5. Based on characterization of 5 parts over temperature
6. Tested on 20 parts at room temperature
7. Part is characterized to Full-Scale Range. Maximum ADC output is [2^{16} / (Sensitivity x 2)]
   Example: For Sensitivity of 131 LSB/(º/s), [2^{16} / (131 x 2)] = ±250 º/s.
8. Based on characterization of 48 parts on evaluation board or in socket

3.2 Electrical Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5 V, VLOGIC = 2.5 V, T_A = 25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
VDD POWER SUPPLY						
Operating Voltage Range		2.1		3.6	V	2
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value (see Figure in Section 4.4)	0		5	ms	2
Normal Operating Current	DMP disabled		6.1 5.9		mA mA	1
Sleep Mode Current			5		µA	4
VLOGIC REFERENCE VOLTAGE						
Voltage Range	VLOGIC must be ≤VDD at all times	1.71		VDD	V	
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value			1	ms	3, 5
Normal Operating Current	(see Figure in Section 4.4)		100		µA	
START-UP TIME FOR REGISTER READ/WRITE			20	100	ms	4
I²C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			1
DIGITAL INPUTS (SDI, SCLK, FSYNC, AD0, /CS, CLKIN)						
V_{IH}, High Level Input Voltage		0.7*VDD			V	4
V_{IL}, Low Level Input Voltage				0.3*VDD	V	4
DIGITAL OUTPUT (INT)						
V_{OH}, High Level Output Voltage	R_{LOAD} = 1 MΩ	0.9*VLOGIC			V	2
V_{OL1}, LOW-Level Output Voltage	R_{LOAD} = 1 MΩ			0.1*VLOGIC	V	2
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN =1, 0.3 mA sink current			0.1	V	2
Output Leakage Current	OPEN = 1		100		nA	3
t_{INT}, INT Pulse Width	LATCH_INT_EN = 0		50		µs	3

Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
4. Based on characterization of 5 parts over temperature
5. Refer to Section 4.4 for the recommended power-on procedure

3.3 Electrical Specifications, continued

Typical Operating Circuit of Section 4.2, VDD = 2.5 V, VLOGIC = 2.5 V, T_A=25°C.

Parameters	Conditions	Typical	Units	Notes
Primary I²C I/O (SCL, SDA)				
V_{IL}, LOW Level Input Voltage	MPU-3050	0.5V to 0.3*VLOGIC	V	1
V_{IH}, HIGH-Level Input Voltage	MPU-3050	0.7*VLOGIC to VLOGIC + 0.5 V	V	1
V_{hys}, Hysteresis	MPU-3050	0.1*VLOGIC	V	1
V_{OL1}, LOW-Level Output Voltage	3mA sink current	0 to 0.4	V	1
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6V	3 5	mA mA	1 1
Output Leakage Current		100	nA	2
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b to 250	ns	1
Secondary I²C I/O (AUX_CL, AUX_DA)	**ACCEL_VDDIO=0**			
V_{IL}, LOW-Level Input Voltage		-0.5 V to 0.3*VLOGIC	V	1
V_{OL1}, LOW-Level Output Voltage	VLOGIC > 2V; 1mA sink current	0 to 0.4	V	1
V_{OL3}, LOW-Level Output Voltage	VLOGIC < 2V; 1mA sink current	0 to 0.2*VLOGIC	V	1
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6V	1 1	mA mA	1 1
Output Leakage Current		100	nA	2
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1C_b to 250	ns	1
Secondary I²C I/O (AUX_CL, AUX_DA)	**ACCEL_VDDIO = 1**			
V_{IL}, LOW-Level Input Voltage		-0.5 to 0.3*VDD	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDD to VDD + 0.5 V	V	1
V_{OL1}, LOW-Level Output Voltage	1mA sink current	0 to 0.4	V	1
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4 V V_{OL} = 0.6 V	1 1	mA mA	1 1
Output Leakage Current		100	nA	2
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus cap. in pF	20+0.1C_b to 250	ns	1

Notes:

1. Based on characterization of 5 parts over temperature.
2. Typical. Randomly selected part measured at room temperature on evaluation board or in socket.

3.4 Electrical Specifications, continued

Typical Operating Circuit of Section 4.2, VDD = 2.5 V, VLOGIC = 2.5 V, T_A=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
INTERNAL CLOCK SOURCE	**CLK_SEL = 0,1,2,3**					
Sample Rate, Fast	DLPFCFG = 0 SAMPLERATEDIV = 0		8		kHz	3
Sample Rate, Slow	DLPFCFG = 1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1		kHz	3
Reference Clock Output	CLKOUTEN = 1		1.024		MHz	3
Clock Frequency Initial Tolerance	CLK_SEL = 0, 25°C	-5		+5	%	1
	CLK_SEL = 1,2,3; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL = 0		-15 to +10		%	2
	CLK_SEL =1,2,3		+/-1		%	2
PLL Settling Time	CLK_SEL=1,2,3		1		ms	3
EXTERNAL 32.768kHz CLOCK	**CLK_SEL=4**					
External Clock Frequency			32.768		kHz	
External Clock Jitter	Cycle-to-cycle rms		1 to 2		µs	
Sample Rate, Fast	DLPFCFG = 0 SAMPLERATEDIV = 0		8.192		kHz	
Sample Rate, Slow	DLPFCFG = 1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1.024		kHz	
Reference Clock Output	CLKOUTEN = 1		1.0486		MHz	
PLL Settling Time			1		ms	
EXTERNAL 19.2 MHz CLOCK	**CLK_SEL = 5**					
External Clock Frequency			19.2		MHz	
Sample Rate, Fast	DLPFCFG = 0 SAMPLERATEDIV = 0		8		kHz	
Sample Rate, Slow	DLPFCFG = 1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1		kHz	
Reference Clock Output	CLKOUTEN = 1		1.024		MHz	
PLL Settling Time			1		ms	

Notes:

1. Tested in production.
2. Based on characterization of 30 parts over temperature on evaluation board or in socket.
3. Typical. Randomly selected part measured at room temperature on evaluation board or in socket.

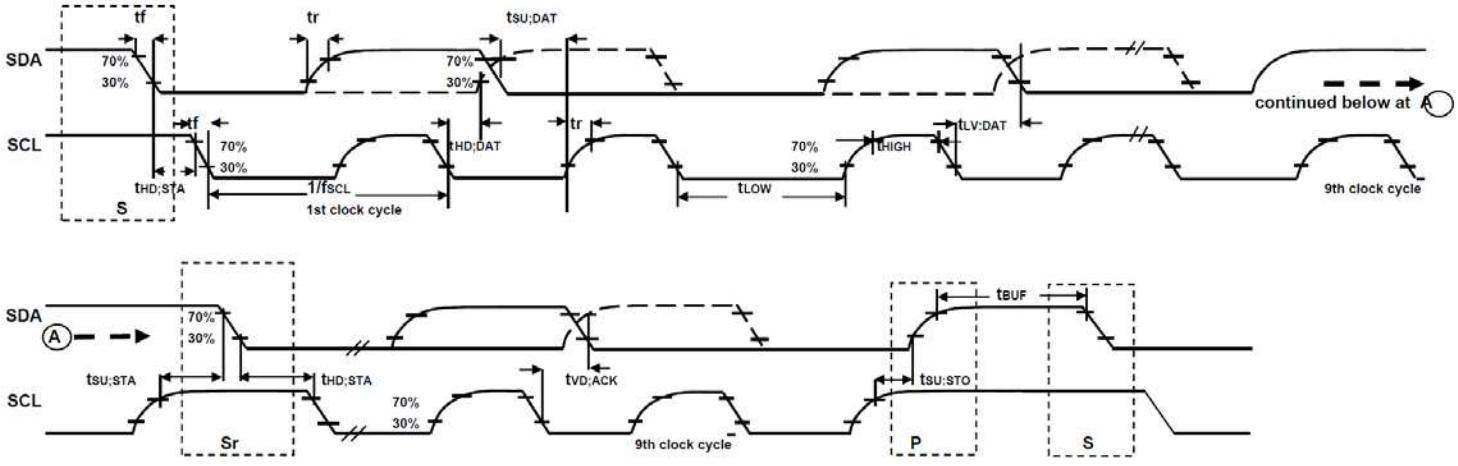
3.5 I²C Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.5 V, VLOGIC = 1.8 V ± 5%, 2.5 V ± 5%, 3.0 V ± 5%, o 3.3 V ± 5%, T_A=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency		0		400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line				400	pF	
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Notes:

1. Based on characterization of 5 parts over temperature on evaluation board or in socket.



I²C Bus Timing Diagram

3.6 Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

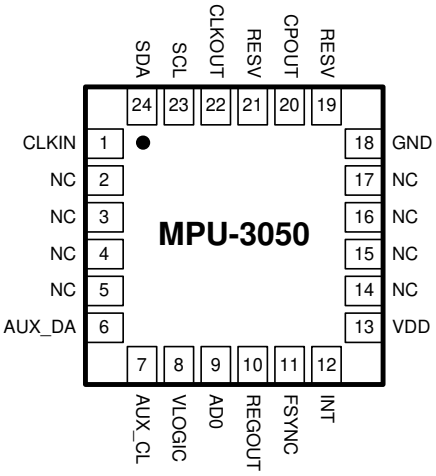
Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, VDD	-0.5 V to +6 V
VLOGIC Input Voltage Level (MPU-3050)	-0.5 V to VDD + 0.5 V
REGOUT	-0.5 V to 2 V
Input Voltage Level (CLKIN, AUX_DA, AD0, FSYNC, INT, SCL, SDA)	-0.5 V to VDD + 0.5 V
CPOUT (2.1V ≤ VDD ≤ 3.6V)	-0.5 V to 30 V
Acceleration (Any Axis, unpowered)	10,000*g* for 0.3 ms
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	1.5 kV (HBM); 200 V (MM)
Latch-up	60 mA @ 125°C JEDEC Condition “B”

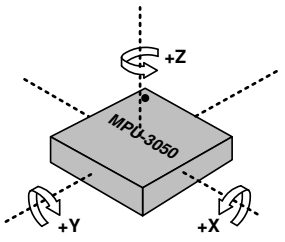
4 Applications Information

4.1 Pin Out and Signal Description

Pin Number	MPU-3050	Pin Name	Pin Description
1	Y	CLKIN	External reference clock input
6	Y	AUX_DA	Interface to a 3rd party accelerometer, SDA pin. Logic levels are set to be either VDD or VLOGIC. See Section 7 for more details.
7	Y	AUX_CL	Interface to a 3rd party accelerometer, SCL pin. Logic levels are set to be either VDD or VLOGIC. See Section 7 for more details.
8	Y	VLOGIC	Digital I/O supply voltage. VLOGIC must be ≤ VDD at all times.
9	Y	AD0	I²C Slave Address LSB
10	Y	REGOUT	Regulator filter capacitor connection
11	Y	FSYNC	Frame synchronization digital input
12	Y	INT	Interrupt digital output (totem pole or open-drain)
13	Y	VDD	Power supply voltage and Digital I/O supply voltage
18	Y	GND	Power supply ground
19	Y	RESV	Reserved. Do not connect.
20	Y	CPOUT	Charge pump capacitor connection
21	Y	RESV	Reserved. Do not connect.
22	Y	CLKOUT	1 MHz clock output for third-party accelerometer synchronization
23	Y	SCL	I²C serial clock
24	Y	SDA	I²C serial data
2, 3, 4, 5, 14, 15, 16, 17	Y	NC	Not internally connected. May be used for PCB trace routing.

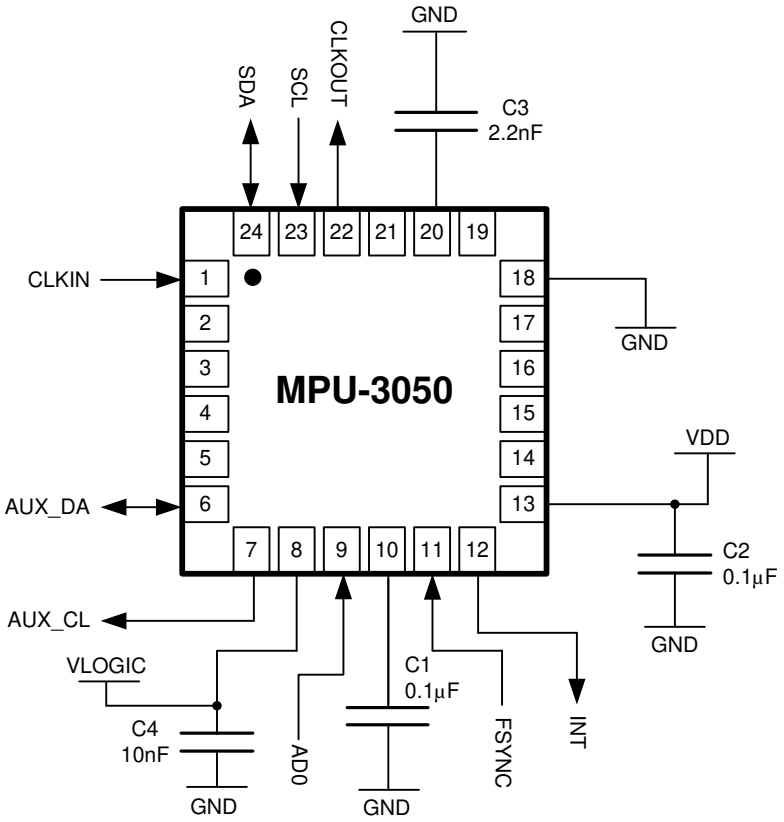


QFN Package (Top View)
24-pin, 4mm x 4mm x 0.9mm



Orientation of Axes of Sensitivity and Polarity of Rotation

4.2 Typical Operating Circuits

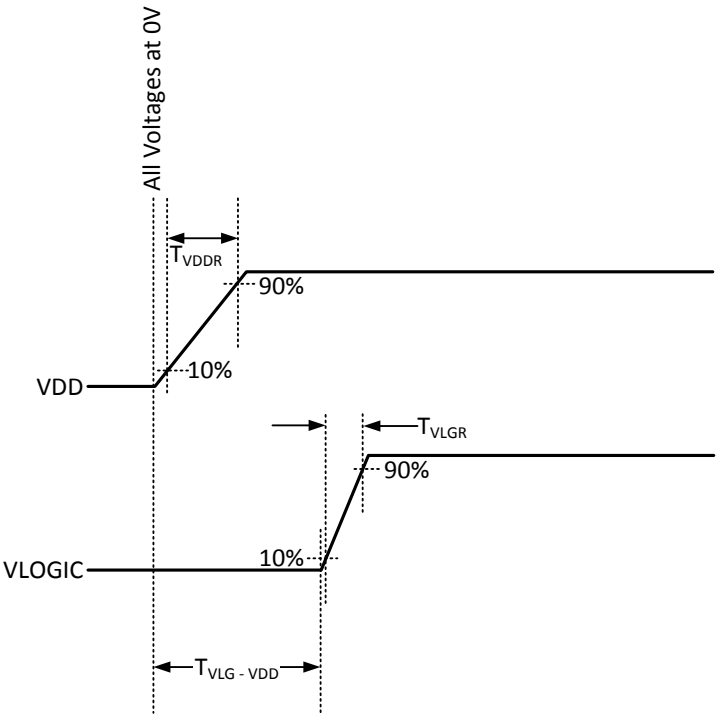


Typical Operating Circuit

4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
VDD Bypass Capacitor	C1	Ceramic, X7R, 0.1 µF ±10%, 4 V	1
Regulator Filter Capacitor	C2	Ceramic, X7R, 0.1 µF ±10%, 2 V	1
Charge Pump Capacitor	C3	Ceramic, X7R, 2.2 nF ±10%, 50 V	1
VLOGIC Bypass Capacitor	C4	Ceramic, X7R, 10 nF ±10%, 4 V	1

4.4 Recommended Power-on Procedure

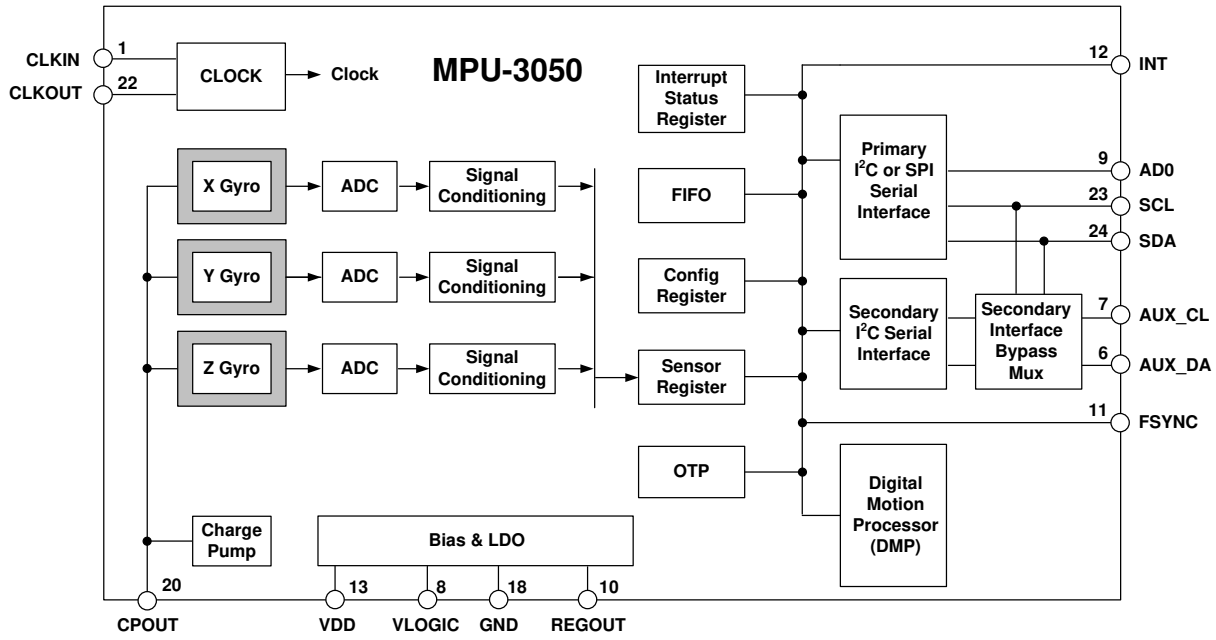


Power-Up Sequencing

1. T_{VDDR} is VDD rise time: Time for VDD to rise from 10% to 90% of its final value.
2. T_{VDDR} is ≤ 10 msec.
3. T_{VDDR} is VLOGIC rise time: Time for VLOGIC to rise from 10% to 90% of its final value.
4. T_{VLGR} is ≤ 1 msec.
5. $T_{VLG-VDD}$ is the delay from the start of VDD ramp to the start of VLOGIC rise.
6. $T_{VLG-VDD}$ is 0 to 20 msec but VLOGIC amplitude must always be ≤ VDD amplitude.
7. VDD and VLOGIC must be monotonic ramps.

5 Functional Overview

5.1 Block Diagram



5.2 Overview

The MPU-3050 is comprised of the following key blocks / functions:

- Three-axis MEMS rate gyroscope sensors with 16-bit ADCs and signal conditioning
- Digital Motion Processor (DMP)
- Primary I²C serial communications interface
- Secondary I²C serial interface for 3rd party accelerometer
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDO
- Charge Pump

5.3 Three-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The MPU-3050 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X, Y, and Z axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps). ADC sample rate is

programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

5.4 Digital Motion Processor

The embedded Digital Motion Processor (DMP) is located within the MPU-3050 and offloads computation of motion processing algorithms from the host processor. The DMP acquires data from accelerometers, gyroscopes, and additional sensors such as magnetometers, and processes the data. The resulting data can be read from the DMP's registers, or can be buffered in a FIFO. The DMP has access to some of MPU's external pins, which can be used for synchronizing external devices to the motion sensors, or generating interrupts for the application.

The purpose of the DMP is to offload both timing requirements and processing power from the host processor. Typically, motion processing algorithms should be run at a high rate, often around 200 Hz, in order to provide accurate results with low latency. This is required even if the application updates at a much lower rate; for example, a low power user interface may update as slowly as 5 Hz, but the motion processing should still run at 200 Hz. The DMP can be used as a tool in order to minimize power, simplify timing and software architecture, and save valuable MIPS on the host processor for use in the application.

5.5 Primary I²C Serial Communications Interface

The MPU-3050 communicates to a system processor using I²C serial interface, and the device always acts as a slave when communicating to the system processor. The logic level for communications to the master is set by the voltage on the VLOGIC pin. The LSB of the I²C slave address is set by pin 9 (AD0).

5.6 Secondary I²C Serial Interface (for a third-party Accelerometer)

The MPU-3050 has a secondary I²C bus for communicating to an off-chip 3-axis digital output accelerometer. This bus has two operating modes: I²C Master Mode, where the MPU-3050 acts as a master to an external accelerometer connected to the secondary I²C bus; and Pass-Through Mode, where the MPU-3050 directly connects the primary and secondary I²C buses together, to allow the system processor to directly communicate with the external accelerometer.

Secondary I²C Bus Modes of Operation:

- I²C Master Mode: allows the MPU-3050 to directly access the data registers of an external digital accelerometer. In this mode, the MPU-3050 directly obtains sensor data from accelerometers and optionally, another sensor (such as a magnetometer), thus allowing the on-chip DMP to generate sensor fusion data without intervention from the system applications processor. In I²C master mode, the MPU-3050 can be configured to perform burst reads, returning the following data from the accelerometer:
    - X accelerometer data (2 bytes)
    - Y accelerometer data (2 bytes)
    - Z accelerometer data (2 bytes)

- Pass-Through Mode: allows an external system processor to act as master and directly communicate to the external accelerometer connected to the secondary I²C bus pins (AUX_DA and AUX_CL). This is useful for configuring the accelerometers, or for keeping the MPU-3050 in a low-power mode, when only accelerometers are to be used. In this mode, the secondary I²C bus control logic (third-party accelerometer Interface block) of the MPU-3050 is disabled, and the secondary I²C pins AUX_DA and AUX_CL (Pins 6 and 7) are connected to the main I²C bus (Pins 23 and 24) through analog switches.

Secondary I²C Bus IO Logic Levels

The logic levels of the secondary I²C bus can be programmed to be either VDD or VLOGIC (see Sections 7 and 8).

6 Clocking

6.1 Internal Clock Generation

The MPU-3050 has a flexible clocking scheme, allowing for a variety of internal or external clock sources for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, the DMP, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

- An internal relaxation oscillator
- Any of the X, Y, or Z gyros (MEMS oscillators with an accuracy of ±2% over temperature)

Allowable external clocking sources are:

- 32.768 kHz square wave
- 19.2 MHz square wave

Which source to select for generating the internal synchronous clock depends on the availability of external sources and the requirements for power consumption and clock accuracy. Most likely, these requirements will vary by mode of operation. For example, in one mode, where the biggest concern is power consumption, one may wish to operate the Digital Motion Processor of the MPU-3050 to process accelerometer data, while keeping the gyros off. In this case, the internal relaxation oscillator is a good clock choice. However, in another mode, where the gyros are active, selecting the gyros as the clock source provides for a more accurate clock source.

Clock accuracy is important, since timing errors directly affect the distance and angle calculations performed by the Digital Motion Processor (or by extension, by any processor).

There are also start-up conditions to consider. When the MPU-3050 first starts up, the device operates off of its internal clock, until programmed to operate from another source. This allows the user, for example, to wait for the MEMS oscillators to stabilize before they are selected as the clock source.

6.2 Clock Output

In addition, the MPU-3050 provides a clock output, which allows the device to operate synchronously with an external digital 3-axis accelerometer. Operating synchronously provides for higher-quality sensor fusion data, since the sampling instant for the sensor data can be set to be coincident for all sensors.

6.3 Sensor Data Registers

The sensor data registers contain the latest gyro and temperature data. They are read-only registers, and are accessed via the Serial Interface. Data from these registers may be read anytime, however, the interrupt function may be used to determine when new data is available.

6.4 FIFO

The MPU-3050 contains a 512-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines what data goes into it, with possible choices being gyro data, accelerometer data, temperature readings, auxiliary ADC readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

6.5 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) Digital Motion Processor Done (programmable function); (3) new data is available to be read (from the FIFO and Data registers); and (4) the MPU-3050 did not receive an acknowledge from the accelerometer on the Secondary I^2C bus. The interrupt status can be read from the Interrupt Status register.

6.6 Bias and LDO

The bias and LDO section generates the internal supply and the reference voltages and currents required by the MPU-3050. Its two inputs are an unregulated VDD of 2.1 V to 3.6 V and a VLOGIC logic reference supply voltage of 1.71 V to VDD. The LDO output is bypassed by a 0.1 µF capacitor at REGOUT.

6.7 Charge Pump

An on-board charge pump generates the high voltage required for the MEMS oscillators. Its output is bypassed by a 2.2 nF capacitor at CPOUT.

6.8 Chip Version

The chip version is written into OTP memory that is accessed using Register 1 (PRODUCT_ID).

7 Digital Interface

7.1 I²C Serial Interface

The internal registers and memory of the MPU-3050 can be accessed using I²C.

Serial Interface

Pin Number	MPU-3050	Pin Name	Pin Description
8	Y	VLOGIC	Digital I/O supply voltage. VLOGIC must be ≤ VDD at all times.
9	Y	AD0	I²C Slave Address LSB
23	Y	SCL	I²C serial clock
24	Y	SDA	I²C serial data

7.1.1 I²C Interface

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The MPU-3050 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

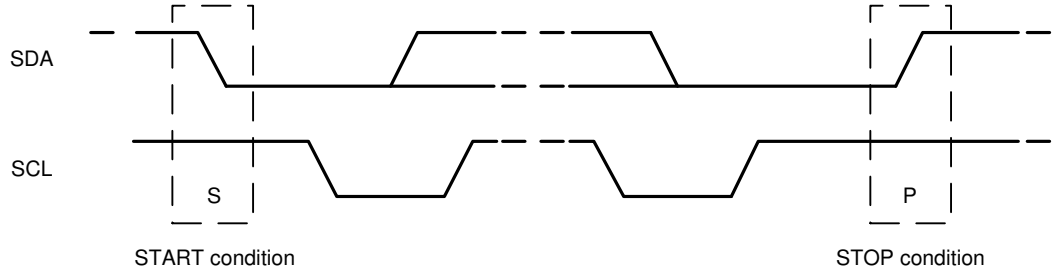
The slave address of the MPU-3050 is b110100X which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin ADO. This allows two MPU-3050s to be connected to the same I²C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin ADO is logic low) and the address of the other should be b1101001 (pin AD0 is logic high). The I²C address is stored in register 0 (WHO_AM_I register).

I²C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

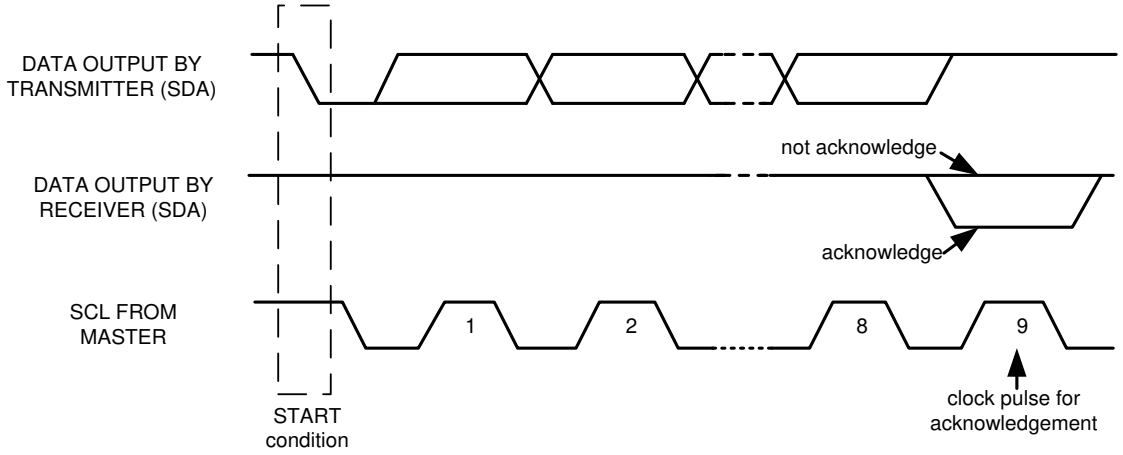


START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

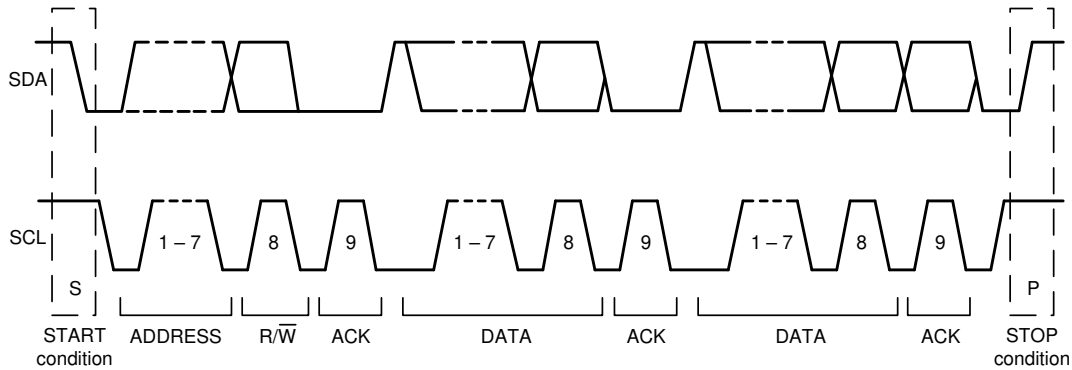
If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).



Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.



Complete I²C Data Transfer

To write the internal MPU-3050 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the MPU-3050 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the MPU-3050 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the MPU-3050 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal MPU-3050 registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the MPU-3050, the master transmits a start signal followed by the slave address and read bit. As a result, the MPU-3050 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

I²C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	MPU-3050 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

8 Serial Interface Considerations (MPU-3050)

8.1 MPU-3050 Supported Interfaces

The MPU-3050 supports I^2C communications on both its primary (microprocessor) serial interface and its secondary (accelerometer) interface.

8.2 Logic Levels

The MPU-3050 I/O logic levels are set to be either VDD or VLOGIC, as shown in the table below.

I/O Logic Levels vs. *AUX_VDDIO* (bit 2, Register 19 – Accelerometer Burst Read Address)

AUX_VDDIO	**MICROPROCESSOR LOGIC LEVELS** (Pins: SDA, SCL, AD0,CLKIN, INT)	**ACCELEROMETER LOGIC LEVELS** (Pins: AUX_DA, AUX_CL)
0	VLOGIC	VLOGIC
1	VLOGIC	VDD

Notes:
1. CLKOUT has logic levels that are always referenced to VDD.
2. The power-on-reset value for *AUX_VDDIO* is 0.

VLOGIC may be set to be equal to VDD or to another voltage, such that at all times VLOGIC is ≤ VDD. When *AUX_VDDIO* is set to 0 (its power-on-reset value), VLOGIC is the power supply voltage for both the microprocessor system bus and the accelerometer secondary bus, as shown in the figure of Section 8.2.1. When *AUX_VDDIO* is set to 1, VLOGIC is the power supply voltage for the microprocessor system bus and VDD is the supply for the accelerometer secondary bus, as shown in the figure of Section 8.2.2.