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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Freescale Semiconductor
Data Sheet: Technical Data

Document Number: PXD10
Rev. 1, 09/2011

RoHS

PXD10


416 TEPBGA
27 mm x 27 mm


208 LQFP
28 mm x 28 mm


176 LQFP
24 mm x 24 mm

PXD10 Microcontroller Data Sheet

The PXD10 family represents a new generation of 32-bit microcontrollers based on the Power Architecture®. These devices provide a cost-effective, single chip display solution for the industrial market. An integrated TFT driver with digital video input ability from an external video source, significant on-chip memory, and low power design methodologies provide flexibility and reliability in meeting display demands in rugged environments. The advanced processor core offers high performance processing optimized for low power consumption, operating at speeds as high as 64 MHz. The family itself is fully scalable from 512 KB to 1 MB internal flash memory. The memory capacity can be further expanded via the on-chip QuadSPI serial flash controller module.

The PXD10 family platform has a single level of memory hierarchy supporting on-chip SRAM and flash memories. The 1 MB flash version features 160 KB of on-chip graphics SRAM to buffer cost effective color TFT displays driven via the on-chip Display Control Unit (DCU). See Table 1 for specific memory size and feature sets of the product family members.

The PXD10 family benefits from the extensive development infrastructure for Power Architecture devices, which is already well established. This includes full support from available software drivers, operating systems, and configuration code to assist with users' implementations. See Section 3, Developer support, for more information.

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1 Overview

1.1 Document overview

This document describes the device features and highlights important electrical and physical characteristics. For functional characteristics, see the *PXD10 Microcontroller Reference Manual.*

1.2 Description

The PXD10 family of chips is designed to enable the development of industrial HMI applications by providing a single-chip solution capable of hosting real-time applications and driving a TFT display directly using an on-chip color TFT display controller.

PXD10 chips incorporate a cost-efficient host processor core compliant with the Power Architecture® embedded category. The processor is 100% user-mode compatible with the Power Architecture and capitalizes on the available development infrastructure of current Power Architecture devices with full support from available software drivers, operating systems and configuration code to assist with users' implementations.

Offering high performance processing at speeds up to 64 MHz, the PXD10 family is optimized for low power consumption and supports a range of on-chip SRAM and internal flash memory sizes. The version with 1 MB of flash memory (PXD1010) features 160 KB of on-chip graphics SRAM.

See Table 1 for specific memory and feature sets of the product family members.

1.3 Device comparison

Table 1. PXD10 family feature set

Feature	PXD1005	PXD1010
CPU	e200z0h	
Execution speed	Static – 64 MHz	
Flash (ECC)	512 KB	1 MB
EEPROM Emulation Block (ECC)	4 × 16 KB	
RAM (ECC)	48 KB	
Graphics RAM	No	160 KB
MPU	12 entry	
eDMA	16 channels	
Display Control Unit (DCU)	No	Yes
Parallel Data Interface	No	Yes
Stepper Motor Controller (SMC)	6 motors	
Stepper Stall Detect (SSD)	Yes	
Sound Generation Logic (SGL)	Yes	

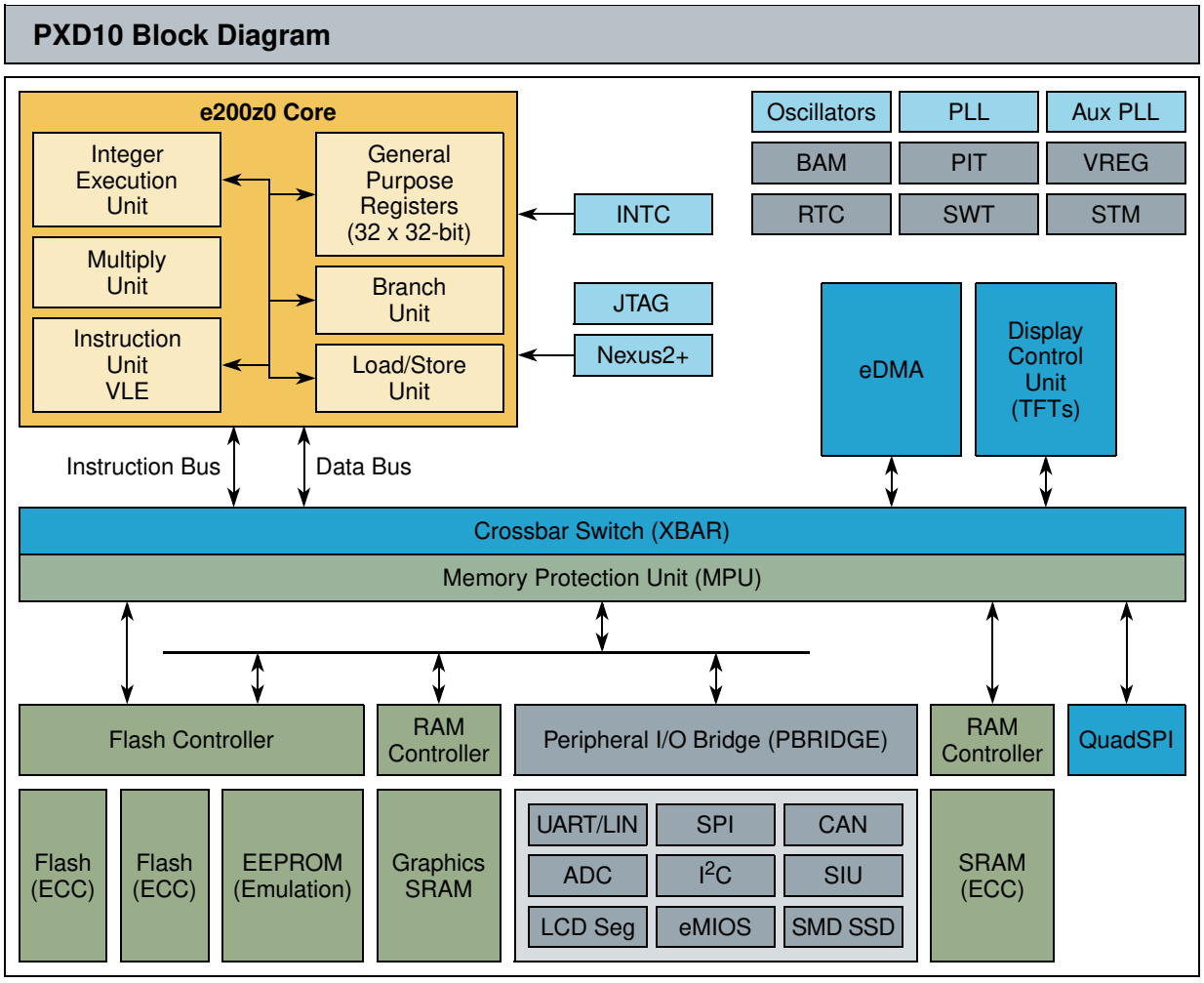
Table 1. PXD10 family feature set (continued)

Feature	PXD1005	PXD1010
LCD driver	64 × 6	40 × 4, 38 × 6
32 kHz slow external crystal oscillator	Yes	
Real-Time Counter and Autonomous Periodic Interrupt	Yes	
Periodic Interrupt Timer (PIT)	4 ch, 32-bit	
Software Watchdog Timer (SWT)	Yes	
System Timer Module (STM)	4 ch, 32-bit	
Timed I/O (eMIOS)	8 ch, 16-bit IC/OC	
	16 ch, 16-bit PWM/IC/OC	
ADC	16 channels, 10-bit	
CAN (64 Mailboxes)	2 × CAN	
CAN Sampler	Yes	
SCI	2 × UART	
SPI	2 × SPI	3 × SPI
QuadSPI Serial Flash Interface	No	Yes
I^2C	2	4
GPIO	105	105 (144-pin package) 133 (176-pin package)
Debug	Nexus 1	Nexus 2+
Package	144 LQFP	144 LQFP 176 LQFP

1.4 PXD10 series blocks

1.4.1 Block diagram

Figure 1 shows a high-level block diagram of the PXD10 series.



ADC – Analog-to-digital converter
BAM – Boot assist module
CAN – Controller area network controller
ECC – Error correction code
eDMA – Enhanced direct memory access controller
eMIOS – Timed input/output
I²C – Inter-integrated circuit controller
INTC – Interrupt controller
JTAG – Joint Test Action Group interface
LCD – Liquid crystal display
PIT – Periodic interrupt timer
PLL – Phase-locked loop
RTC – Real time clock
SIU – System integration unit
SMD SSD – Stepper motor driver/stepper stall detect
SPI – Serial peripheral interface controller
SRAM – Static random-access memory
STM – System timer module
SWT – Software watchdog timer
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
VLE – Variable-length execution set
VREG – Voltage regulator

Figure 1. PXD10 series block diagram

1.5 PXD10 features

1.5.1 Summary

- Single issue, 32-bit Power Architecture technology compliant CPU core complex (e200z0h)
  - Compatible with Power Architecture instruction set
  - Includes variable length encoding (VLE) instruction set for smaller code size footprint; with the encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction over conventional Book E compliant code
- On-chip ECC flash memory with flash controller
  - As much as 1 MB primary flash—two 512 KB modules with prefetch buffer and 128-bit data access port
  - 64 KB data flash—separate 4×16 KB flash block for EEPROM emulation with prefetch buffer and 128-bit data access port
- As much as 48 KB on-chip ECC SRAM with SRAM controller
- As much as 160 KB on-chip non-ECC graphics SRAM with SRAM controller
- Memory Protection Unit (MPU) with as many as 12 region descriptors and 32-byte region granularity to provide basic memory access permission
- Interrupt Controller (INTC) with as many as 127 peripheral interrupt sources and eight software interrupts
- Two Frequency-Modulated Phase-Locked Loops (FMPLLs)
  - Primary FMPLL provides a 64 MHz system clock
  - Auxiliary FMPLL is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules and as alternate clock to the DCU for pixel clock generation
- Crossbar switch architecture enables concurrent access of peripherals, flash memory or RAM from multiple bus masters (AMBA 2.0 v6 AHB)
- 16-channel Enhanced Direct Memory Access controller (eDMA) with multiple transfer request sources using a DMA channel multiplexer
- Boot Assist Module (BAM) supports internal flash programming via a serial link (FlexCAN or LINFlex)
- Display Control Unit to drive TFT LCD displays
  - Includes processing of as many as four planes that can be blended together
  - Offers a direct unbuffered hardware bit-blitter of as many as 16 software-configurable dynamic layers in order to drastically minimize graphic memory requirements and provide fast animations
  - Programmable display resolutions are available up to WVGA
- Parallel Data Interface (PDI) for digital video input
- LCD segment driver module with two software programmable configurations:
  - As many as 40 frontplane drivers and four backplane drivers

  - As many as 38 frontplane drivers and six backplane drivers
- Stepper Motor Controller (SMC) module with high-current drivers for as many as six stepper motors driven in full dual H-Bridge configuration including full diagnostics for short circuit detection
- Stepper motor return-to-zero and stall detection module
- Sound generation and playback utilizing PWM channels and eDMA; supports monotonic and polyphonic sound
- 24 eMIOS channels providing as many as 16 PWM and 24 input capture / output compare channels
- 10-bit Analog-to-Digital Converter (ADC)
  - Maximum conversion time of 1 µs
  - As many as 16 internal channels, expandable to 23 via external multiplexing
- As many as two Serial Peripheral Interface (DSPI) modules for full-duplex, synchronous, communications with external devices (extendable to include up to 8 multiplexed external channels)
- QuadSPI serial flash memory controller supporting single, dual and quad modes of operation to interface to external serial flash memory. QuadSPI can be configured to function as another DSPI module.
- Two Local Interconnect Network Flexible (LINFlex) controller modules capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support. Compliant with LIN protocol rev 2.1
- Two full CAN 2.0B controllers with 64 configurable buffers each; bit rate programmable as fast as 1 Mbit/s
- As many as four inter-integrated circuit (I^2C) internal bus controllers with master/slave bus interface
- As many as 133 configurable general purpose pins supporting input and output operations
- Real Time Counter (RTC) with multiple clock sources:
  - 128 kHz slow internal RC oscillator or 16 MHz fast internal RC oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
  - 32 KHz slow external crystal oscillator, supporting wakeup with 1 s resolution and maximum timeout of one hour
  - 4–16 MHz fast external crystal oscillator
- System timers:
  - Four-channel 32-bit System Timer Module (STM)—included in processor platform
  - Four-channel 32-bit Periodic Interrupt Timer (PIT) module
  - Software Watchdog Timer (SWT)
- System Integration Unit (SIU) module to manage resets, external interrupts, GPIO and pad control
- System Status and Configuration Module (SSCM) to provide information for identification of the device, last boot mode, or debug status and provides an entry point for the censorship password mechanism

- Clock Generation Module (MC_CGM) to generate system clock sources and provide a unified register interface, enabling access to all clock sources
- Clock Monitor Unit (CMU) to monitor the integrity of the main crystal oscillator and the PLL and act as a frequency meter, measuring the frequency of one clock source and comparing it to a reference clock
- Mode Entry Module (MC_ME) to control the device power mode, i.e., RUN, HALT, STOP, or STANDBY, control mode transition sequences, and manage the power control, voltage regulator, clock generation and clock management modules
- Reset Generation Module (MC_RGM) to manage reset assertion and release to the device at initial power-up
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus standard
- Device/board boundary-scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator controller for regulating the 3.3 or 5 V supply voltage down to 1.2 V for core logic (requires external ballast transistor)
- The PXD10 microcontrollers are offered in the following packages:[1]
  - 144 LQFP, 0.5 mm pitch, 20 mm × 20 mm outline
  - 176 LQFP, 0.5 mm pitch, 24 mm × 24 mm outline

1.6 Details

1.6.1 Low-power operation

PXD10 devices are designed for optimized low-power operation and dynamic power management of the core processor and peripherals. Power management features include software-controlled clock gating of peripherals and multiple power domains to minimize leakage in low-power modes.

There are two static low-power modes, STANDBY and STOP, and two dynamic power modes—RUN and HALT. Both low power modes use clock gating to halt the clock for all or part of the device. The STANDBY mode also uses power gating to automatically turn off the power supply to parts of the device to minimize leakage.

STANDBY mode turns off the power to the majority of the chip to offer the lowest power consumption mode. The contents of the cores, on-chip peripheral registers and potentially some of the volatile memory are lost. STANDBY mode is configurable to make certain features available with the disadvantage that these consume additional current:

- It is possible to retain the contents of the full RAM or only 8 KB.
- It is possible to enable the internal 16 MHz or 128 kHz RC oscillator, the external 4–16 MHz oscillator, or the external 32 KHz oscillator.
- It is possible to keep the LCD module active.

1. See the device comparison table or orderable parts summary for package offerings for each device in the family.

The device can be awakened from STANDBY mode via from any of as many as 19 I/O pins, a reset or from a periodic wake-up using a low power oscillator.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the core and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wake-up from STOP mode is triggered by an external event or by the internal periodic wake-up, if enabled.

RUN modes are the main operating mode where the entire device can be powered and clocked and from which most processing activity is done. Four dynamic RUN modes are supported—RUN0 - RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed and system clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the core system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

Table 1 summarizes the operating modes of PXD10 devices.

Table 1. Operating mode summary[1]

Operating modes	SOC features					Clock sources						Periodic Wake-up	Wake-up input	VREG mode	Wake-up time[2]						
	Core	Peripherals	Flash	RAM	Graphics RAM	Main PLL	Auxiliary PLL	16 MHz IRC	X OSC	128 kHz IRC	32 KHz X OSC				VREG start-up	IRC Wake-up	Flash Recovery	OSC Stabilization	PLL Lock	S/W Reconfig	Mode switch over
RUN	On	OP	OP	On	On	OP	OP	On	OP	On	OP	—	—	FP	—	—	—	—	—	—	—
HALT	CG	OP	OP	On	On	OP	OP	On	OP	On	OP	OP	OP	FP	—	—	—	—	—	—	TBD
STOP	CG	CG	CG	On	On	CG	CG	OP	OP	On	OP	OP	OP	LP	50 µs	4 µs	20 µs	1ms	200 µs	—	24 µs
STANDBY	Off	Off[3]	Off	CG[4]	Off	Off	Off	OP	OP	On	OP	OP	OP	LP	50 µs	8 µs	100 µs	1ms	200 µs	Var	28 µs
	Off	Off	Off	8K[5]	Off	Off	Off	OP	OP	On	OP	OP	OP	LP	50 µs	8 µs	100 µs	1ms	200 µs	Var	28 µs
POR															500 µs	8 µs	100 µs	1ms	200 µs		BAM

NOTES:

1 Table Key:

On—Powered and clocked

OP—Optionally configurable to be enabled or disabled (clock gated)

CG—Clock Gated, Powered but clock stopped

Off—Powered off and clock gated

FP—VREG Full Performance mode

LP—VREG Low Power mode, reduced output capability of VREG but lower power consumption

Var—Variable duration, based on the required reconfiguration and execution clock speed

BAM—Boot Assist Module Software and Hardware used for device start-up and configuration

2 A high level summary of some key durations that need to be considered when recovering from low power modes. This does not account for all durations at wake up. Other delays will be necessary to consider including, but not limited to the external supply start-up time.
IRC Wake-up time must not be added to the overall wake-up time as it starts in parallel with the VREG.
All other wake-up times must be added to determine the total start-up time

3 The LCD can optionally be kept running while the device is in STANDBY mode.

4 All of the RAM contents is retained, but not accessible in STANDBY mode.

5 8 KB of the RAM contents is retained, but not accessible in STANDBY mode.

Additional notes on low power operation:

- Fast wake-up using the on-chip 16 MHz internal RC oscillator allows rapid execution from RAM on exit from low power modes
- The 16 MHz internal RC oscillator supports low speed code execution and clocking of peripherals when it is selected as the system clock and can also be used as the PLL input clock source to provide fast start-up without the external oscillator delay
- PXD10 devices include an internal voltage regulator that includes the following features:
  - Regulates input to generate all internal supplies
  - Manages power gating
  - Low power regulators support operation when in STOP and STANDBY modes to minimize power consumption
  - Startup on-chip regulators in <50 µs for rapid exit of STOP and STANDBY modes
  - Low voltage detection on main supply and 1.2 V regulated supplies

1.6.2 e200z0h core processor

The e200z0h processor is similar to other processors in the e200zx series but supports only the VLE instruction set and does not include the signal processing extension for DSP applications or a floating point unit.

The e200z0h has all the features of the e200z0 plus:

- Branch acceleration using Branch Target Buffer (BTB)
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and Flash memory via independent Instruction and Data BIUs

The e200z0h processor uses a four stage in-order pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), an 8 × 32 Hardware Multiplier array, result feed-forward hardware, and a hardware divider.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide and multiply instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated Branch Address adder to minimize delays during change of flow operations. Branch target prefetching from the BTB is performed to accelerate certain taken branches. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding four instructions.

Conditional branches not taken execute in a single clock. Branches with successful target prefetching have an effective execution time of one clock on e200z0h. All other taken branches have an execution time of two clocks.

Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the Power Architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

Vectored and autovectored interrupts are supported. Hardware vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements. This allows the classic PowerPC instruction set to be represented by a modified instruction set made up from a mixture of 16-bit and 32-bit instructions. This results in a significantly smaller code size footprint without affecting performance noticeably.

The CPU core is enhanced by an additional interrupt source—Non Maskable Interrupt. This interrupt source is routed directly from package pins, via edge detection logic in the SIU to the CPU, bypassing the Interrupt Controller completely. Once the edge detection logic is programmed, it can not be disabled, except by reset. The Non Maskable Interrupt is, as the name suggests, completely un-maskable and when asserted will always result in the immediate execution of the respective interrupt service routine. The Non maskable interrupt is not guaranteed to be recoverable.

The CPU core has an additional ‘Wait for Interrupt’ instruction that is used in conjunction with low power STOP mode. When Low Power Stop mode is selected, this instruction is executed to allow the system clock to be stopped. An external interrupt source or the system wake-up timer is used to restart the system clock and allow the CPU to service the interrupt.

Additional features include:

- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Reservation instructions for implementing read-modify-write constructs
- Multi-cycle divide (divw) and load multiple (lmw) store multiple (smw) multiple class instructions, can be interrupted to prevent increases in interrupt latency
- Extensive system development support through Nexus debug port

1.6.3 Display Control Unit (DCU)

The DCU is a display controller designed to drive TFT LCD displays capable of driving up to WQVGA resolution screens with 16 layers and 4 planes with real time alpha-blending.

The DCU generates all the necessary signals required to drive the display: up to 24-bit RGB data bus, Pixel Clock, Data Enable, Horizontal-Sync and Vertical-Sync.

Internal memory resource of the PXD10 allows to easily handle complex graphics contents (pictures, icons, languages, fonts) on a color TFT panel in up to Wide Quarter Video Graphics Array (WQVGA) sizes. All the data fetches from internal and/or external memory are performed by the internal four-channel DMA of the DCU providing a high speed/low latency access to the system backbone.

Control Descriptors (CDs) associated with each layer enable effective merging of different resolutions into one plane to optimize use of internal memory buffers. A layer may be constructed from graphic content of various resolutions including 1bpp, 2bpp, 4bpp, 8bpp, 16bpp, 24bpp and 24bpp+alpha. The ability of the DCU to handle input data in resolutions as low as 1bpp, 2bpp and 4bpp enables a highly efficient use of internal memory resources of the PXD10. A special tiled mode can be enabled on any of the 16 layers to repeat a pattern optimizing graphic memory usage.

A hardware cursor can be managed independently of the layers at blending level increasing the efficient use of the internal DCU resources.

To secure the content of all critical information to be displayed, a safety mode can be activated to check the integrity of critical data along the whole system data path from the memory to the TFT pads.

The DCU features the following:

- Display color depth: up to 24 bpp
- Generation of all RGB and control signals for TFT
- Four-plane blending
- Maximum number of Input Layers: 16 (fixed priority)
- Dynamic look-up table (color and gamma look-up)
- α–blending range: as many as 256 levels
- Transparency Mode
- Gamma Correction
- Tiled mode on all the layers
- Hardware cursor
- Critical display content integrity monitoring for functional safety support
- Internal Direct Memory Access (DMA) module to transfer data from internal and/or external memory.

1.6.4 Parallel Data Interface (PDI)

The PDI is a digital interface used to receive external digital video or graphic content into the DCU.

The PDI input is directly injected into the DCU background plane FIFO. When the PDI is activated, all the DCU synchronization is extracted from the external video stream to guarantee the synchronization of the two video sources.

The PDI can be used to:

- Connect a video camera output directly to the PDI
- Connect a secondary display driver as slave with a minimum of extra cost
- Connect a device gathering various Video sources
- Provide flexibility to allow the DCU to be used in slave mode (external synchronization)

The PDI features the following:

- Supported color modes:
  - 8-bit mono
  - 8-bit color multiplexed
  - RGB565
  - 16-bit/18-bit RAW color
- Supported synchronization modes:
  - Embedded ITU-R BT.656-4 (RGB565 mode 2)
  - HSYNC, VSYNC
  - Data Enable
- Direct interface with DCU background plane FIFO
- Synchronization generation for the DCU

1.6.5 Liquid Crystal Display (LCD) driver

The LCD driver module has two configurations allowing a maximum of 160 or 228 LCD segments:

- As many as 40 frontplane drivers and four backplane drivers
- As many as 38 frontplane drivers and six backplane drivers

Each segment is controlled and can be masked by a corresponding bit in the LCD RAM.

Four to six multiplex modes (1/1, 1/2, 1/3, 1/4, 1/5, 1/6 duty), and three bias (1/1, 1/2, 1/3) methods are available. All frontplane and backplane pins can be multiplexed with other port functions.

The LCD driver module features the following:

- Programmable frame clock generator from different clock sources:
  - System clock
  - Internal RC oscillator
- Programmable bias voltage level selector
- On-chip generation of all output voltage levels

  - LCD voltage reference taken from main 5V supply
- LCD RAM
  - Contains the data to be displayed on the LCD
  - Data can be read from or written to the display RAM at any time
- End of Frame interrupt
  - Optimizes the refresh of the data without visual artefact
  - Provides selectable number of frames between each interrupt
- Contrast adjustment using programmable internal voltage reference
- Remapping capability of four or six backplanes with frontplanes
  - Increase pin selection flexibility
- In low power modes, the LCD operation can be suspended under software control. The LCD can also operate in low power modes, clocked by the internal 128 kHz IRC or external 32 KHz crystal oscillator
- Selectable output current boost during transitions

1.6.6 Stepper Motor Controller (SMC)

The SMC module is a PWM motor controller suitable to drive loads requiring a PWM signal. The motor controller has twelve PWM channels associated with two pins each (24 pins in total).

The SMC module includes the following features:

- 10/11-bit PWM counter
- 11-bit resolution with selectable PWM dithering function
- Left, right, or center aligned PWM
- Output slew rate control
- Output Short Circuit Detection

This module is suited for, but not limited to, driving small stepper and air core motors used in instrumentation applications. This module can be used for other motor control or PWM applications that match the frequency, resolution, and output drive capabilities of the module.

1.6.7 Stepper Stall Detector (SSD)

The stepper stall detector (SSD) module provides a circuit to measure and integrate the induced voltage on the non-driven coil of a stepper motor using full steps when the gauge pointer is returning to zero (RTZ).

The SSD module features the following:

- Programmable full step state
- Programmable integration polarity
- Blanking (recirculation) state
- 16-bit integration accumulator register
- 16-bit modulus down counter with interrupt

1.6.8 Flash memory

The PXD10 microcontroller has the following flash memory features:

- As much as 1 MB of burst flash memory
  - — Typical flash memory access time: 0 wait-state for buffer hits, 2 wait-states for page buffer miss at 64 MHz
  - — Two 4 × 128-bit page buffers with programmable prefetch control
    - – One set of page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
    - – One set of page buffers allocated to Display Controller Unit and the eDMA
  - — 64-bit ECC with single-bit correction, double-bit detection for data integrity
  - — 64 KB data flash memory — separate 4 × 16 KB flash block for EEPROM emulation with prefetch buffer and 128-bit data access port
- Small block flash memory arrangement to support features such as boot block, operating system block
- Hardware managed flash memory writes, erase and verify sequence
- Censorship protection scheme to prevent flash memory content visibility
- Separate dedicated 64 KB data flash memory for EEPROM emulation
  - — Four erase sectors each containing 16 KB of memory
  - — Offers Read-While-Write functionality from main program space
  - — Same data retention and program erase specification as main program flash memory array

1.6.9 Static random-access memory (SRAM)

The PXD10 microcontrollers have as much as 48 KB general-purpose on-chip SRAM with the following features:

- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back to back with a read to same memory block
- 32-bit ECC with single-bit correction, double bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Separate internal power domain applied to full SRAM block, 8 KB SRAM block during STANDBY modes to retain contents during low power mode.

1.6.10 On-chip graphics SRAM

The PXD10 microcontroller has 160 KB on-chip graphics SRAM with the following features:

- Usable as general purpose SRAM
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory

1.6.11 QuadSPI serial flash controller

The QuadSPI module enables use of external serial flash memories supporting single, dual and quad modes of operation. It features the following:

- Memory mapping of external serial flash
- Automatic serial flash read command generation by CPU, DMA or DCU read access on AHB bus
- Supports single, dual and quad serial flash read commands
- Flexible buffering scheme to maximize read bandwidth of serial flash
- 'Legacy' mode allowing QuadSPI to be used as a standard SPI (no DSI or CSI mode)

1.6.12 Analog-to-digital converter (ADC)

The ADC features the following:

- 10-bit A/D resolution
- 0 to 5 V common mode conversion range
- Supports conversions speeds of as fast as 1 µs
- 16 internal and 8 external channels support
- As many as 16 single-ended inputs channels
  - All channels configured to have alternate function as general purpose input/output pins
    - 10-bit ±3 counts accuracy (TUE)
- External multiplexer support to increase as many as 23 channels
  - Automatic 1 × 8 multiplexer control
  - External multiplexer connected to a dedicated input channel
  - Shared register between the 8 external channels
- Result register available for every non-multiplexed channel
- Configurable left- or right-aligned result format
- Supports for one-shot, scan and injection conversion modes
- Injection mode status bit implemented on adjacent 16-bit register for each result
  - Supports access to result and injection status with single 32-bit read
- Independently enabling of function for channels:
  - Pre-sampling
  - Offset error cancellation
  - Offset refresh
- Conversion Triggering support
  - Internal conversion triggering from periodic interrupt timer (PIT)
- Four configurable analog comparator channels offering range comparison with triggered alarm
  - Greater than
  - Less than
  - Out of range

- All unused analog inputs can be used as general purpose input and output pins
- Power down mode
- Optional support for DMA transfer of results

1.6.13 Sound generation logic (SGL) module

The SGL module has two modes of operation:

- Amplitude modulated PWM mode for low cost buzzers using any two eMIOS channels
  - Monophonic signal with amplitude control
  - 8-bit amplitude resolution
  - Ability to mix any two eMIOS channels.
  - Requires simple external RC lowpass filter
- Digital sample mode for higher quality sound using one eMIOS channel and eDMA
  - Up to 10-bit audio amplitude resolution
  - Polyphonic sound synthesis
  - Playback of sample based waveforms
  - Text-to-speech possibility
  - Requires external lowpass filter

1.6.14 Serial communication interface module (UART)

The PXD10 devices include as many as two UART modules and support UART Master mode, UART Slave mode and UART mode. The modules are UART state machine compliant to the UART 1.3 and 2.0 and 2.1 Specifications and handle UART frame transmission and reception without CPU intervention.

The serial communication interface module offers the following:

- UART features:
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
    - Parity, noise and framing errors
  - Interrupt driven operation with four interrupts sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - Two receiver wake-up methods
- LIN features:
  - Autonomous LIN frame handling
  - Message buffer to store identifier and as many as 8 data bytes

— Supports message length of as long as 64 bytes
— Detection and flagging of LIN errors
— Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Timeout errors
— Classic or extended checksum calculation
— Configurable Break duration of up to 36-bit times
— Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
— Diagnostic features
  – Loop back
  – Self Test
  – LIN bus stuck dominant detection
— Interrupt driven operation with 16 interrupt sources
— LIN slave mode features
  – Autonomous LIN header handling
  – Autonomous LIN response handling
  – Discarding of irrelevant LIN responses using as many as 16 ID filters

1.6.15 Serial Peripheral Interface (SPI) module

The SPI modules provide a synchronous serial interface for communication between the PXD10 MCU and external devices.

The SPI features the following:

- As many as two SPI modules
- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from four to 16 bits
- As many as six chip select lines available, depending on package and pin multiplexing, enable 64 external devices to be selected using external muxing from a single SPI
- Eight clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering as many as four transfers on the transmit and receive side
- General purpose I/O functionality on pins when not used for SPI
- Queueing operation possible through use of eDMA

1.6.16 Controller Area Network (CAN) module

The PXD10 contains two CAN modules that offer the following features:

- Compliant with CAN protocol specification, Version 2.0B active
- 64 mailboxes, each configurable as transmit or receive
  - — Mailboxes configurable while module remains synchronized to CAN bus
- Transmit features
  - — Supports configuration of multiple mailboxes to form message queues of scalable depth
  - — Arbitration scheme according to message ID or message buffer number
  - — Internal arbitration to guarantee no inner or outer priority inversion
  - — Transmit abort procedure and notification
- Receive features
  - — Individual programmable filters for each mailbox
  - — 8 mailboxes configurable as a 6-entry receive FIFO
  - — 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - — System clock
  - — Direct oscillator clock to avoid PLL jitter
- Listen only mode capabilities
- CAN Sampler
  - — Can catch the first message sent on the CAN network while the PXD10 is stopped. This guarantees a clean startup of the system without missing messages on the CAN network.
  - — The CAN sampler is connected to one of the CAN RX pins.

1.6.17 Inter-IC Communications (I^2C) module

The I^2C module features the following:

- As many as four I^2C modules supported
- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multimaster operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

1.6.18 Real Time Counter (RTC)

The Real Timer Counter supports wake-up from Low Power modes or Real Time Clock generation

- Configurable resolution for different timeout periods
  - 1 s resolution for >1 hour period
  - 1 ms resolution for 2 second period
- Selectable clock sources from external 32 KHz crystal, external 4–16 MHz crystal, internal 128 kHz RC oscillator or divided internal 16 MHz RC oscillator

1.6.19 Enhanced Modular Input/Output System (Timers, PWM)

PXD10 microcontrollers have two eMIOS modules—one with 16 channels and one with 8—with input/output channels supporting a range of 16-bit input capture, output compare, and Pulse Width Modulation functions.

The modules are configurable and can implement 8-channel, 16-bit input capture/output compare or 16-channel, 16-bit output pulse width modulation/input compare/output compare. As many as five additional channels are configurable as modulus counters.

eMIOS features include:

- Selectable clock source from main FMPLL, auxiliary FMPLL, external 4–16 MHz oscillator or 16 MHz Internal RC oscillator
- Timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges
- Edge aligned output pulse width modulation
  - Programmable pulse period and duty cycle
  - Supports 0% and 100% duty cycle
  - Shared or independent time bases
- Programmable phase shift between channels
- Selectable combination of pairs of eMIOS outputs to support sound generation
- DMA transfer support
- Selectable clock source from the primary FMPLL, auxiliary FMPLL, external 4–16 MHz oscillator or the 16 MHz internal RC oscillator.

The channel configuration options for the 16-channel eMIOS module are summarized in Table 2.

Table 2. 16-channel eMIOS module channel configuration

Channel mode	Channel number				
	8 IC/OC Counter	9–15 IC/OC	16 PWM Counter	17–22 PWM	23 PWM Counter
General Purpose Input/Output	X	X	X	X	X
Single Action Input Capture	X	X	X	X	X
Single Action Output Compare	X	X	X	X	X
Modulus Counter Buffered[1]	X		X		X
Output Pulse Width and Frequency Modulation Buffered			X	X	X
Output Pulse Width Modulation Buffered			X	X	X

NOTES:
1 Modulus up and down counters to support driving local and global counter busses

The channel configuration options for the 8-channel eMIOS module are summarized in Table 3.

Table 3. 8-Channel eMIOS module channel configuration

Channel mode	Channel number		
	16 PWM Counter	17–22 PWM	23 PWM Counter
General Purpose Input/Output	X	X	X
Single Action Input Capture	X	X	X
Single Action Output Compare	X	X	X
Modulus Counter Buffered[1]	X		X
Output Pulse Width and Frequency Modulation Buffered	X	X	X
Output Pulse Width Modulation Buffered	X	X	X

NOTES:
1 Modulus up and down counters to support driving local and global counter busses

1.6.20 Periodic interrupt timer (PIT) module

The PIT features the following:

- Four general purpose interrupt timers
- As many as two dedicated interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for Real Time Interrupt, clocked from main external oscillator

1.6.21 System Timer Module (STM)

The STM is a 32-bit timer that supports commonly required system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel. The counter is driven by the system clock divided by an 8-bit prescale value (1 to 256).

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.6.22 Software Watchdog Timer (SWT)

The SWT features the following:

- Watchdog supporting software activation or enabled out of reset
- Supports normal or windowed mode
- Watchdog timer value writable once after reset
- Watchdog supports optional halting during low power modes
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Selectable clock source for main system clock or internal 16 MHz RC oscillator clock

1.6.23 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software settable interrupt requests. These same software settable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software settable interrupt request to finish the servicing in a lower priority ISR. Therefore these software settable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS. The INTC provides the following features:

- Unique 9-bit vector for each of the possible 128 separate interrupt sources
- Eight software-triggerable interrupt sources

- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority.
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- External non-maskable interrupt directly accessing the main core critical interrupt mechanism
- 32 external interrupts

1.6.24 System Integration Unit (SIU)

The SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.

The GPIO features the following:

- As many as four levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package
- Centralized general purpose input output (GPIO) control of as many as 132 input/output pins (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs
- Direct readback of the pin value supported on all digital output pins through the SIU
- Configurable digital input filter that can be applied to as many as 14 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset.

1.6.25 System Clocks and Clock Generation Modules

The system clock on the PXD10 can be derived from an external oscillator, an on-chip FMPLL, or the internal 16 MHz oscillator.

- The source system clock frequency can be changed via an on-chip programmable clock divider (÷1 to ÷32).
- Additional programmable peripheral bus clock divider ratio (÷1 to ÷16)
- The PXD10 has two on-chip FMPLLs—the primary module and an auxiliary module.
  - Each features the following:
    - Input clock frequency from 4 MHz to 16 MHz
    - Lock detect circuitry continuously monitors lock status
    - Loss Of Clock (LOC) detection for reference and feedback clocks
    - On-chip loop filter (for improved electromagnetic interference performance and reduction of number of external components required)

  - Support for frequency ramping from PLL
  - The primary FMPLL module is for use as a system clock source. The auxiliary FMPLL is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules and as alternate clock to the DCU for pixel clock generation.
- The main oscillator provides the following features:
  - Input frequency range 4–16 MHz
  - Square-wave input mode
  - Oscillator input mode 3.3 V (5.0 V)
  - Automatic level control
  - PLL reference
- PXD10 includes a 32 KHz low power external oscillator for slow execution, low power, and Real Time Clock
- Dedicated internal 128 kHz RC oscillator for low power mode operation and self wake-up
  - ±10% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support improved accuracy with in-application calibration
- Dedicated 16 MHz internal RC oscillator
  - Used as default clock source out of reset
  - Provides a clock for rapid start-up from low power modes
  - Provides a back-up clock in the event of PLL or External Oscillator clock failure
  - Offers an independent clock source for the Watchdog timer
  - ±5% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support frequency adjustment with in-application calibration

1.6.26 Crossbar Switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port but one of those transfers must be an instruction fetch from internal flash. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters having equal priority are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- Four master ports
  - e200z0h core instruction port
  - e200z0h core complex load/store data port
  - eDMA controller
  - Display control unit

- Four slave ports
  - — One flash port dedicated to the CPU
  - — Platform SRAM
  - — QuadSPI serial flash controller
  - — One slave port combining:
    - – Flash port dedicated to the Display Control Unit and eDMA module
    - – Graphics SRAM
    - – Peripheral bridge
- 32-bit internal address bus, 32-bit internal data bus

1.6.27 Enhanced Direct Memory Access (eDMA)

The eDMA module is a controller capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- 16 channels support independent 8-, 16- or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, periodic timer interrupt or eDMA channel request
- Each DMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, QuadSPI, SPIs, I^2C, ADC, eMIOS and General Purpose I/Os (GPIOs)
- Programmable DMA Channel Mux allows assignment of any DMA source to any available DMA channel with a total of as many as 64 potential request sources.

1.6.28 Memory Protection Unit (MPU)

The MPU features the following:

- 12 region descriptors for per-master protection
- Start and end address defined with 32-byte granularity
- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for 3 concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters