



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



FEATURES

64K x 16 MRAM Memory

- 3.3 Volt power supply
- Fast 35ns read/write cycle
- SRAM compatible timing
- Unlimited read & write endurance
- Commercial, Industrial, and Extended Temperatures
- Data non-volatile for >20 years at temperature
- RoHS-compliant TSOP2 and BGA packages available
- All products meet MSL-3 moisture sensitivity level
- Automotive AEC-Q100 Grade 1 option available



44-pin TSOP2



48-ball BGA

BENEFITS

- One memory replaces FLASH, SRAM, EEPROM and BBSRAM in system for simpler, more efficient designs
- Improves reliability by replacing battery-backed SRAM
- Automatic data protection on power loss



INTRODUCTION

The **MR0A16A** is a 1,048,576-bit magnetoresistive random access memory (MRAM) device organized as 65,536 words of 16 bits. The **MR0A16A** offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification.

MR0A16A is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The **MR0A16B** is available in a small footprint 48-pin ball grid array (BGA) package and a 44-pin thin small outline package (TSOP Type 2). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.

The **MR0A16A** provides highly reliable data storage over a wide range of temperatures. The product is available with commercial temperature (0 to +70 °C), industrial temperature (-40 to +85 °C), extended temperature (-40 to +105 °C), and Automotive AEC-Q100 Grade 1 (-40 to +125°) temperature range options.

TABLE OF CONTENTS

| | |
|---|-----------|
| FEATURES | 1 |
| BENEFITS..... | 1 |
| INTRODUCTION | 1 |
| BLOCK DIAGRAM AND PIN ASSIGNMENTS..... | 4 |
| Figure 1 – Block Diagram | 4 |
| Table 1 – Pin Functions..... | 4 |
| Figure 2 – MR0A16A Package Pinouts | 5 |
| OPERATING MODES..... | 5 |
| Table 2 – Operating Modes..... | 5 |
| ABSOLUTE MAXIMUM RATINGS..... | 6 |
| Table 3 – Absolute Maximum Ratings..... | 6 |
| OPERATING CONDITIONS | 7 |
| Table 4 – Operating Conditions..... | 7 |
| Power Up and Power Down Sequencing | 8 |
| Figure 3 – Power Up and Power Down Timing | 8 |
| DC CHARACTERISTICS..... | 9 |
| Table 5 – DC Characteristics..... | 9 |
| Table 6 – Power Supply Characteristics | 9 |
| TIMING SPECIFICATIONS | 10 |
| Table 7 – Capacitance | 10 |
| Table 8 – AC Measurement Conditions | 10 |
| Figure 4 – Output Load Test Low and High..... | 10 |
| Figure 5 – Output Load Test All Others..... | 10 |
| Table 9 – Read Cycle Timing | 11 |
| Figure 6 – Read Cycle 1 | 12 |

TABLE OF CONTENTS - continued

| | |
|---|-----------|
| Figure 7 – Read Cycle 2..... | 12 |
| Table 10 – Write Cycle Timing 1 (\overline{W} Controlled) | 13 |
| Figure 8 – Write Cycle Timing 1 (\overline{W} Controlled) | 14 |
| Table 11 – Write Cycle Timing 2 (\overline{E} Controlled)..... | 15 |
| Figure 9 – Write Cycle Timing 2 (\overline{E} Controlled) | 15 |
| Table 12 – Write Cycle Timing 3 ($\overline{LB}/\overline{UB}$ Controlled)..... | 16 |
| Figure 10 – Write Cycle Timing 3 ($\overline{UB}/\overline{LB}$ Controlled)..... | 16 |
| ORDERING INFORMATION | 17 |
| Table 13 – Part Numbering System..... | 17 |
| Table 14 – MR0A16A Ordering Part Numbers | 18 |
| PACKAGE OUTLINE DRAWINGS..... | 19 |
| Figure 11 – 44-pin TSOP2..... | 19 |
| Figure 12 – 48-ball FBGA..... | 20 |
| REVISION HISTORY | 21 |
| HOW TO CONTACT US..... | 22 |

BLOCK DIAGRAM AND PIN ASSIGNMENTS

Figure 1 – Block Diagram

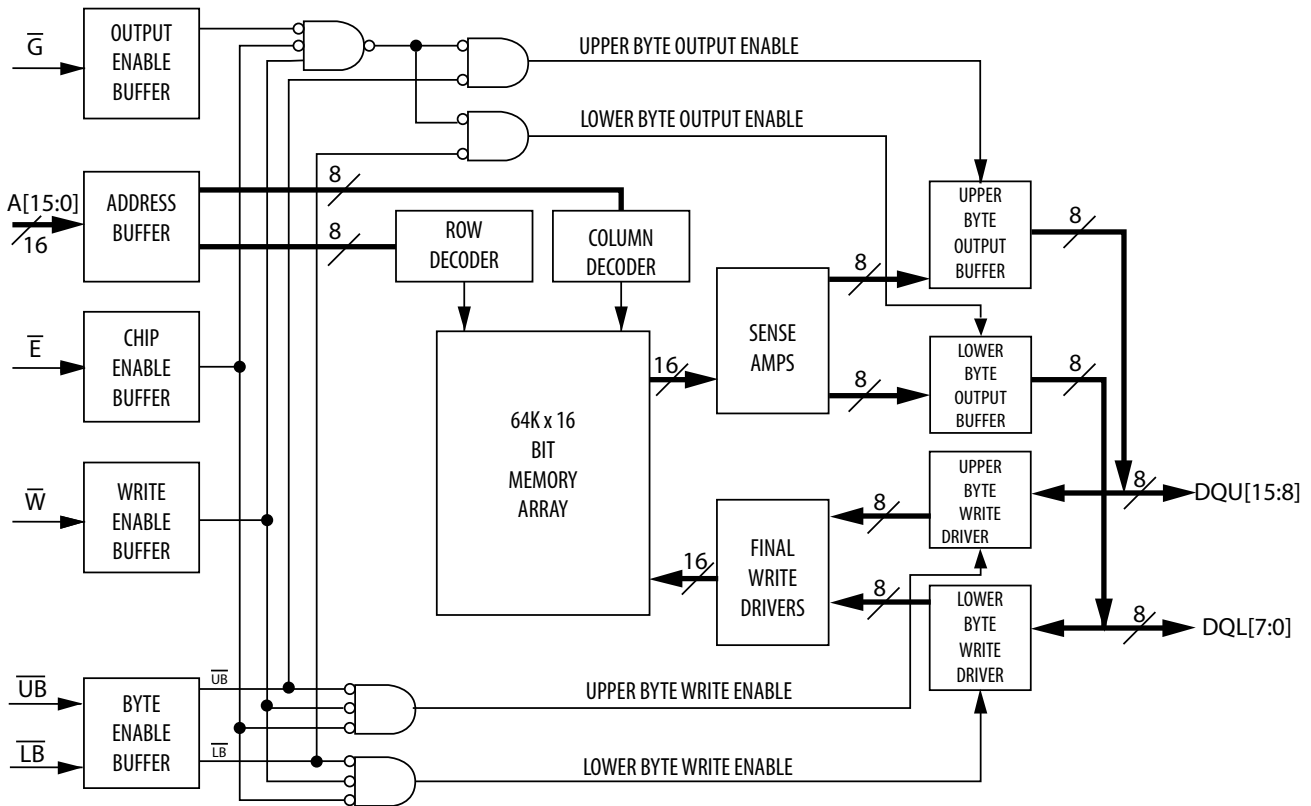
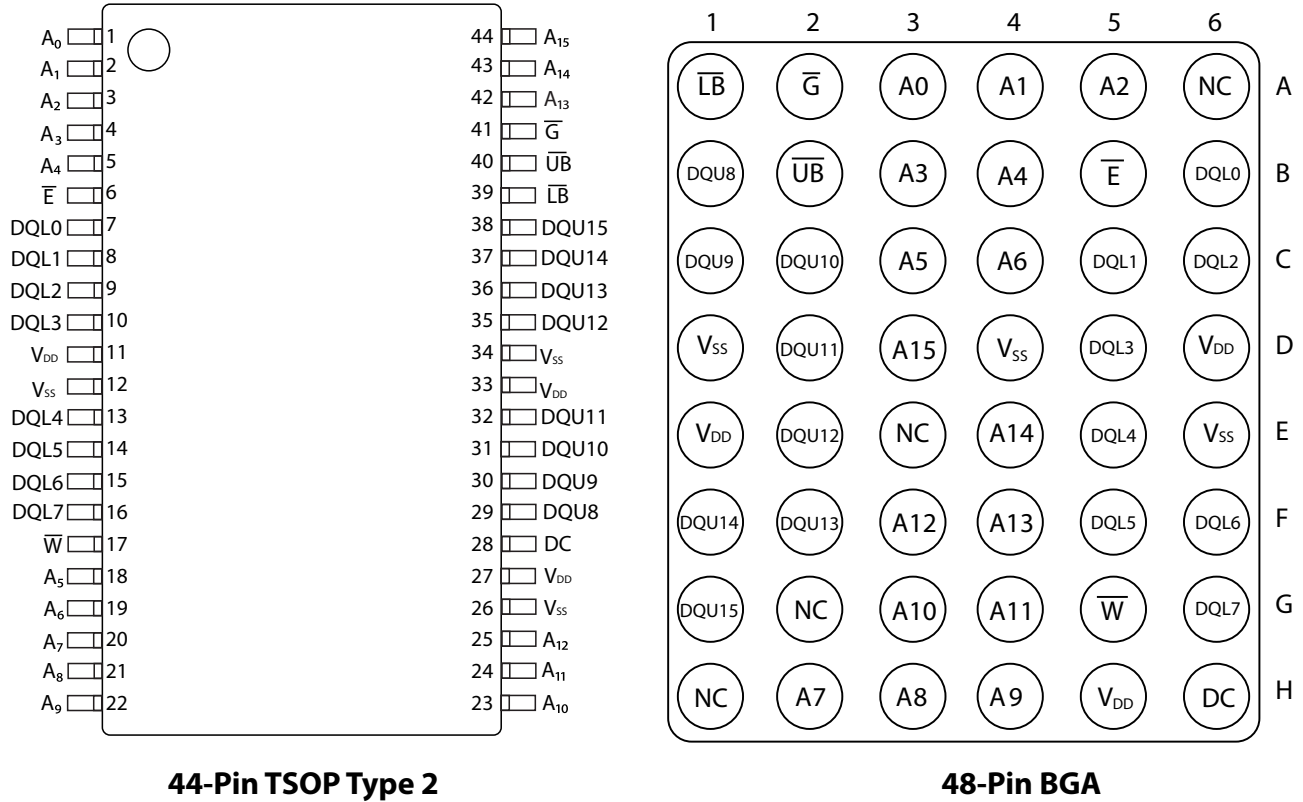


Table 1 – Pin Functions

| Signal Name | Function |
|-------------|-------------------|
| A | Address Input |
| \bar{E} | Chip Enable |
| \bar{W} | Write Enable |
| \bar{G} | Output Enable |
| \bar{UB} | Upper Byte Enable |
| \bar{LB} | Lower Byte Enable |
| DQ | Data I/O |
| V_{DD} | Power Supply |
| V_{SS} | Ground |
| DC | Do Not Connect |
| NC | No Connection |

Figure 2 – MR0A16A Package Pinouts



OPERATING MODES

Table 2 – Operating Modes

| \bar{E}^1 | \bar{G}^1 | \bar{W}^1 | \bar{LB}^1 | \bar{UB}^1 | Mode | V_{DD} Current | DQL[7:0] ² | DQU[15:8] ² |
|-------------|-------------|-------------|--------------|--------------|------------------|--------------------|-----------------------|------------------------|
| H | X | X | X | X | Not selected | I_{SB1}, I_{SB2} | Hi-Z | Hi-Z |
| L | H | H | X | X | Output disabled | I_{DDR} | Hi-Z | Hi-Z |
| L | X | X | H | H | Output disabled | I_{DDR} | Hi-Z | Hi-Z |
| L | L | H | L | H | Lower Byte Read | I_{DDR} | D _{Out} | Hi-Z |
| L | L | H | H | L | Upper Byte Read | I_{DDR} | Hi-Z | D _{Out} |
| L | L | H | L | L | Word Read | I_{DDR} | D _{Out} | D _{Out} |
| L | X | L | L | H | Lower Byte Write | I_{DDW} | D _{in} | Hi-Z |
| L | X | L | H | L | Upper Byte Write | I_{DDW} | Hi-Z | D _{in} |
| L | X | L | L | L | Word Write | I_{DDW} | D _{in} | D _{in} |

Notes:

1. H = high, L = low, X = don't care
2. Hi-Z = high impedance

ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, normal precautions should be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability. ¹

Table 3 – Absolute Maximum Ratings

| Symbol | Parameter | Temp Range | Package | Value | Unit |
|------------------------|---|----------------------|------------|-------------------------------|------|
| V _{DD} | Supply voltage ² | - | - | -0.5 to 4.0 | V |
| V _{IN} | Voltage on any pin ² | - | - | -0.5 to V _{DD} + 0.5 | V |
| I _{OUT} | Output current per pin | - | - | ±20 | mA |
| P _D | Package power dissipation ³ | - | Note 3 | 0.600 | W |
| T _{BIAS} | Temperature under bias | Commercial | - | -10 to 85 | °C |
| | | Industrial | - | -45 to 95 | |
| | | Extended | - | -45 to 110 | |
| | | AEC Q-100 Grade 1 | - | -45 to 130 | |
| T _{stg} | Storage Temperature | - | - | -55 to 150 | °C |
| T _{Lead} | Lead temperature during solder (3 minute max) | - | - | 260 | °C |
| H _{max_write} | Maximum magnetic field during write | Commercial | TSOP2, BGA | 2,000 | A/m |
| | | Industrial, Extended | BGA | 2,000 | |
| | | | TSOP2 | 10,000 | |
| | | AEC-Q100 Grade 1 | TSOP2 | 2,000 | |
| H _{max_read} | Maximum magnetic field during read or standby | Commercial | TSOP2, BGA | 8,000 | A/m |
| | | Industrial, Extended | BGA | 8,000 | |
| | | | TSOP2 | 10,000 | |
| | | AEC-Q100 Grade 1 | TSOP2 | 8,000 | |

Notes appear on the next page.

Notes: for MR0A16A Absolute Maximum Ratings:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS} .
3. Power dissipation capability depends on package characteristics and use environment.

OPERATING CONDITIONS

Table 4 – Operating Conditions

| Symbol | Parameter | Temp Range | Min | Typical | Max | Unit |
|----------|-----------------------------------|--------------------------------|-------------------|---------|-----------------------------|------|
| V_{DD} | Power supply voltage ¹ | All | 3.0 | 3.3 | 3.6 | V |
| V_{WI} | Write inhibit voltage | All | 2.5 | 2.7 | 3.0 ¹ | V |
| V_{IH} | Input high voltage | All | 2.2 | - | $V_{DD} + 0.3$ ² | V |
| V_{IL} | Input low voltage | All | -0.5 ³ | - | 0.8 | V |
| T_A | Ambient Temperature under bias | Commercial | 0 | | 70 | °C |
| | | Industrial | -40 | | 85 | |
| | | Extended | -40 | | 105 | |
| | | AEC Q-100 Grade 1 ⁴ | -40 | | 125 | |

Notes:

1. There is a 2 ms startup time once V_{DD} exceeds $V_{DD, (min)}$. See **Power Up and Power Down Sequencing** below.
2. $V_{IH(max)} = V_{DD} + 0.3 V_{DC}$; $V_{IH(max)} = V_{DD} + 2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.
3. $V_{IL(min)} = -0.5 V_{DC}$; $V_{IL(min)} = -2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.
4. AEC-Q100 Grade 1 temperature profile assumes 10% duty cycle at maximum temperature (2 years out of 20 years life.)

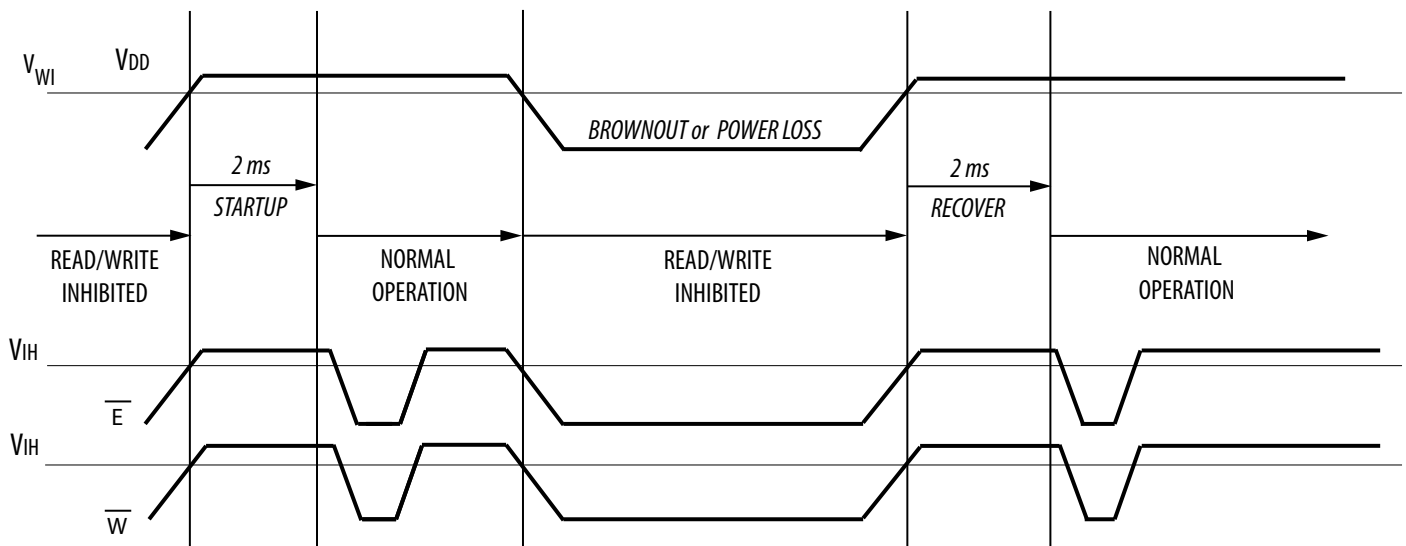
Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds $V_{DD(min)}$, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The \bar{E} and \bar{W} control signals should track V_{DD} on power up to $V_{DD} - 0.2\text{ V}$ or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives \bar{E} and \bar{W} should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above $V_{DD(min)}$.

Figure 3 – Power Up and Power Down Timing



DC CHARACTERISTICS

Table 5 – DC Characteristics

| Symbol | Parameter | Condition | Min | Max | Unit |
|--------------|------------------------|--------------------------|----------------|----------------|---------|
| $I_{lkg(I)}$ | Input leakage current | All | - | ± 1 | μA |
| $I_{lkg(O)}$ | Output leakage current | All | - | ± 1 | μA |
| V_{OL} | Output low voltage | $I_{OL} = +4 \text{ mA}$ | - | 0.4 | V |
| | | $I_{OL} = +100 \mu A$ | | $V_{SS} + 0.2$ | |
| V_{OH} | Output high voltage | $I_{OH} = -4 \text{ mA}$ | 2.4 | - | V |
| | | $I_{OH} = -100 \mu A$ | $V_{DD} - 0.2$ | | |

Table 6 – Power Supply Characteristics

| Symbol | Parameter | Condition | Temp Range | Typical | Max | Unit |
|-----------|--|---|---------------------|---------|-----|------|
| I_{DDR} | AC active supply current - read modes ¹ | $I_{OUT} = 0 \text{ mA}, V_{DD} = \text{max}$ | All | 55 | 80 | mA |
| I_{DDW} | AC active supply current - write modes ¹ | $V_{DD} = \text{max}$ | Commercial | 105 | 155 | mA |
| | | | Industrial | 105 | 165 | |
| | | | Extended | 105 | 165 | |
| | | | AEC-Q100 Grade 1 | 105 | 165 | |
| I_{SB1} | AC standby current | $V_{DD} = \text{max}, E = V_{IH}$ No other restrictions on other inputs | All | 18 | 28 | mA |
| I_{SB2} | CMOS standby current | $E \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$ $V_{DD} = \text{max}, f = 0 \text{ MHz}$ | | 9 | 12 | mA |

Notes:

- All active current measurements are measured with one address transition per cycle and at minimum cycle time.

TIMING SPECIFICATIONS

Table 7 – Capacitance

| Symbol | Parameter ¹ | Typical | Max | Unit |
|-----------|---------------------------|---------|-----|------|
| C_{In} | Address input capacitance | - | 6 | pF |
| C_{In} | Control input capacitance | - | 6 | pF |
| $C_{I/O}$ | Input/Output capacitance | - | 8 | pF |

Notes:

- $f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25 \text{ }^\circ\text{C}$, periodically sampled rather than 100% tested.

Table 8 – AC Measurement Conditions

| Parameter | Value | Unit |
|---|--------------|------|
| Logic input timing measurement reference level | 1.5 | V |
| Logic output timing measurement reference level | 1.5 | V |
| Logic input pulse levels | 0 or 3.0 | V |
| Input rise/fall time | 2 | ns |
| Output load for low and high impedance parameters | See Figure 4 | |
| Output load for all other timing parameters | See Figure 5 | |

Figure 4 – Output Load Test Low and High

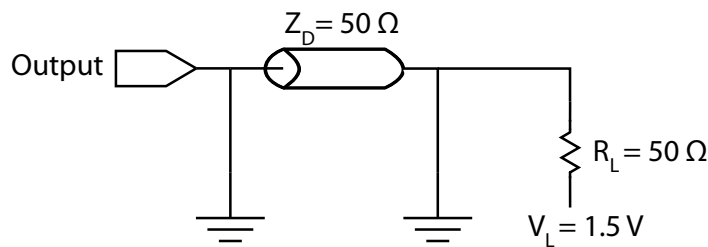


Figure 5 – Output Load Test All Others

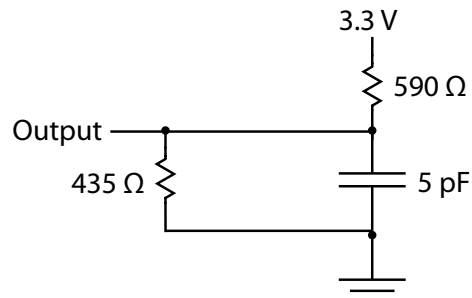


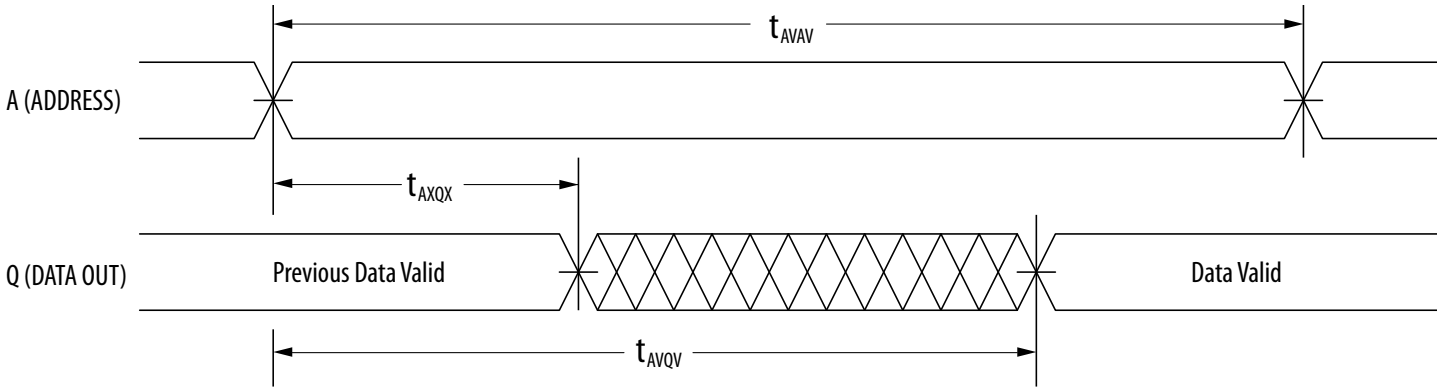
Table 9 – Read Cycle Timing

| Symbol | Parameter ¹ | Min | Max | Unit |
|-------------------|---|-----|-----|------|
| t _{AVAV} | Read cycle time | 35 | - | ns |
| t _{AVQV} | Address access time | - | 35 | ns |
| t _{ELQV} | Enable access time ² | - | 35 | ns |
| t _{GLQV} | Output enable access time | - | 15 | ns |
| t _{BLQV} | Byte enable access time | - | 15 | ns |
| t _{AXQX} | Output hold from address change | 3 | - | ns |
| t _{ELQX} | Enable low to output active ³ | 3 | - | ns |
| t _{GLQX} | Output enable low to output active ³ | 0 | - | ns |
| t _{BLQX} | Byte enable low to output active ³ | 0 | - | ns |
| t _{EHQZ} | Enable high to output Hi-Z ³ | 0 | 15 | ns |
| t _{GHQZ} | Output enable high to output Hi-Z ³ | 0 | 10 | ns |
| t _{BHQZ} | Byte high to output Hi-Z ³ | 0 | 10 | ns |

Notes:

1. W is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
2. Addresses valid before or at the same time E goes low.
3. This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage.

Figure 6 – Read Cycle 1



Note: Device is continuously selected ($\bar{E} \leq V_{IL}$, $\bar{G} \leq V_{IL}$).

Figure 7 – Read Cycle 2

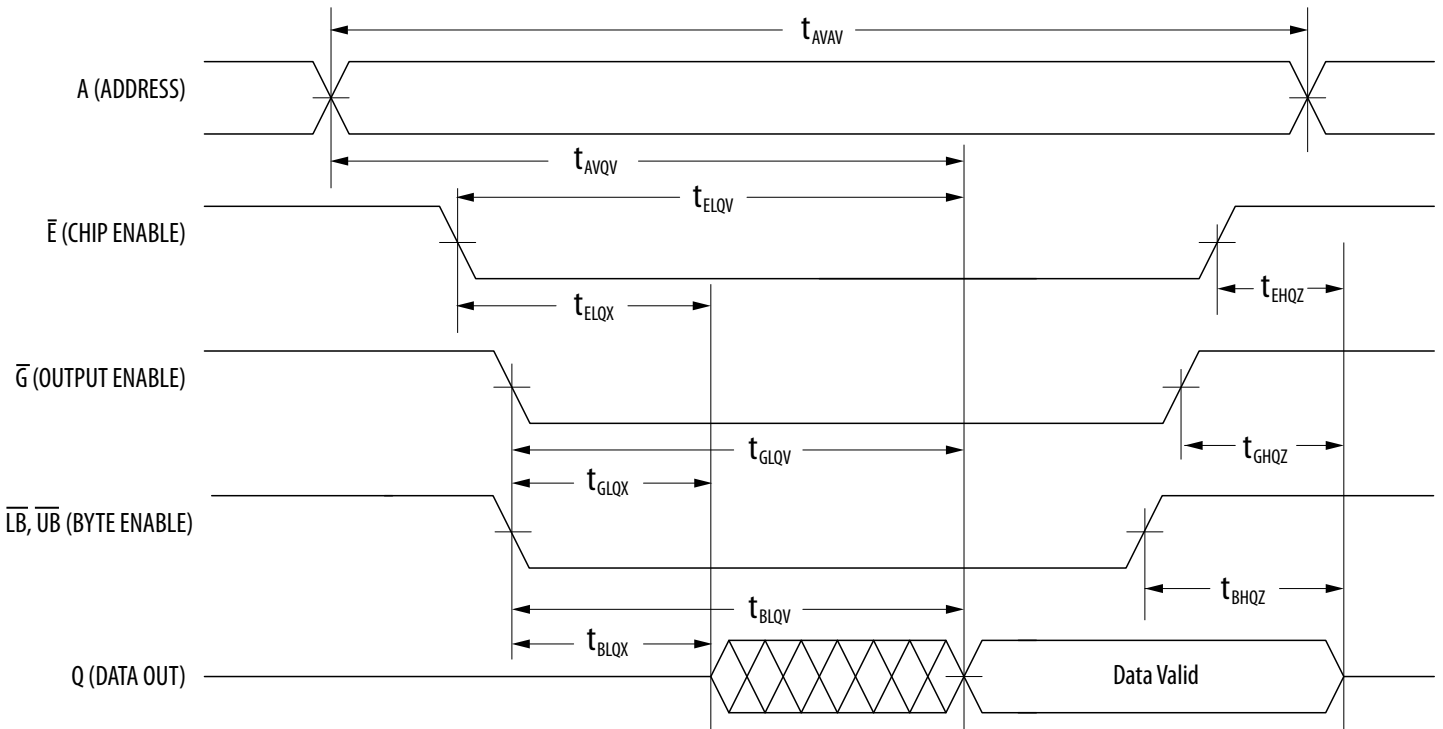


Table 10 – Write Cycle Timing 1 (\overline{W} Controlled)

| Symbol | Parameter ¹ | Min | Max | Unit |
|--------------------------|--|-----|-----|------|
| t_{AVAV} | Write cycle time ² | 35 | - | ns |
| t_{AVWL} | Address set-up time | 0 | - | ns |
| t_{AVWH} | Address valid to end of write (G high) | 18 | - | ns |
| t_{AVWL} | Address valid to end of write (G low) | 20 | - | ns |
| t_{WLWH} t_{WLEH} | Write pulse width (G high) | 15 | - | ns |
| t_{WLWH} t_{WLEH} | Write pulse width (G low) | 15 | - | ns |
| t_{DVWH} | Data valid to end of write | 10 | - | ns |
| t_{WHDX} | Data hold time | 0 | - | ns |
| t_{WLQZ} | Write low to data Hi-Z ³ | 0 | 12 | ns |
| t_{WHQX} | Write high to output active ³ | 3 | - | ns |
| t_{WHAX} | Write recovery time | 12 | - | ns |

Notes:

1. All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} or \overline{E} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage. At any given voltage or temperate, $t_{WLQZ}(\max) < t_{WHQX}(\min)$

Figure 8 – Write Cycle Timing 1 (\overline{W} Controlled)

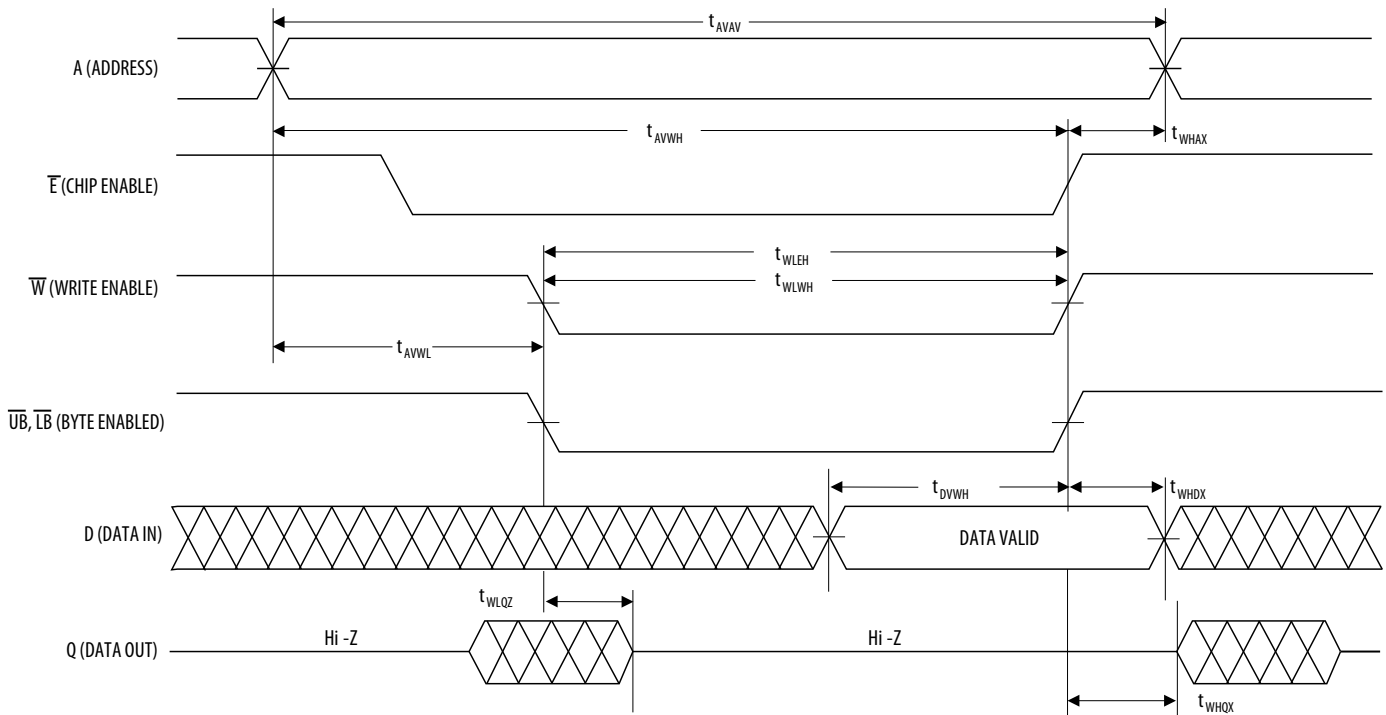


Table 11 – Write Cycle Timing 2 (E Controlled)

| Symbol | Parameter ¹ | Min | Max | Unit |
|--------------------------|---|-----|-----|------|
| t_{AVAV} | Write cycle time ² | 35 | - | ns |
| t_{AVEL} | Address set-up time | 0 | - | ns |
| t_{AVEH} | Address valid to end of write (G high) | 18 | - | ns |
| t_{AVEH} | Address valid to end of write (G low) | 20 | - | ns |
| t_{ELEH} t_{ELWH} | Enable to end of write (G high) | 15 | - | ns |
| t_{ELEH} t_{ELWH} | Enable to end of write (G low) ³ | 15 | - | ns |
| t_{DVEH} | Data valid to end of write | 10 | - | ns |
| t_{EHDX} | Data hold time | 0 | - | ns |
| t_{EHAX} | Write recovery time | 12 | - | ns |

Notes:

1. All write occurs during the overlap of \bar{E} low and \bar{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \bar{G} goes low at the same time or after \bar{W} goes low, the output will remain in a high impedance state. After \bar{W} or \bar{E} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \bar{E} being asserted low in one cycle to \bar{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If \bar{E} goes low at the same time or after \bar{W} goes low, the output will remain in a high-impedance state. If \bar{E} goes high at the same time or before \bar{W} goes high, the output will remain in a high-impedance state.

Figure 9 – Write Cycle Timing 2 (E Controlled)

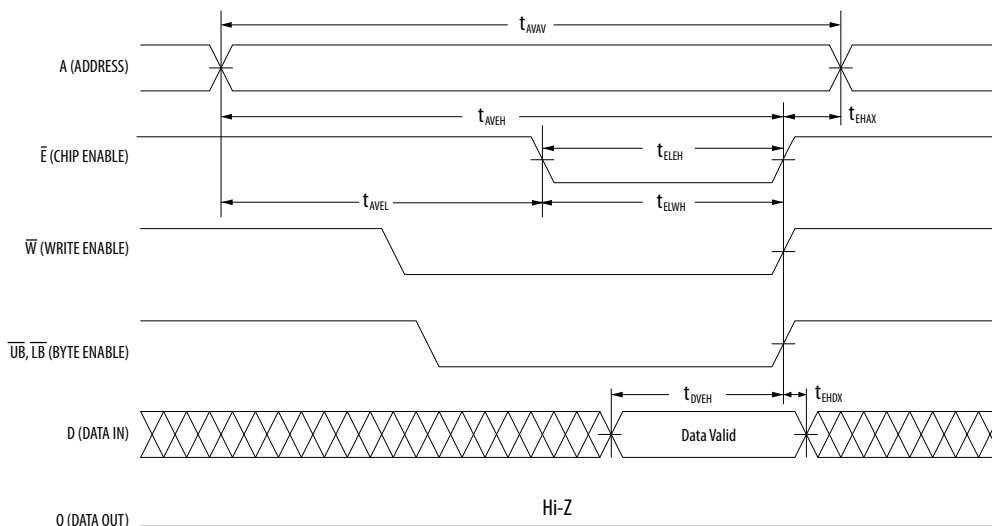


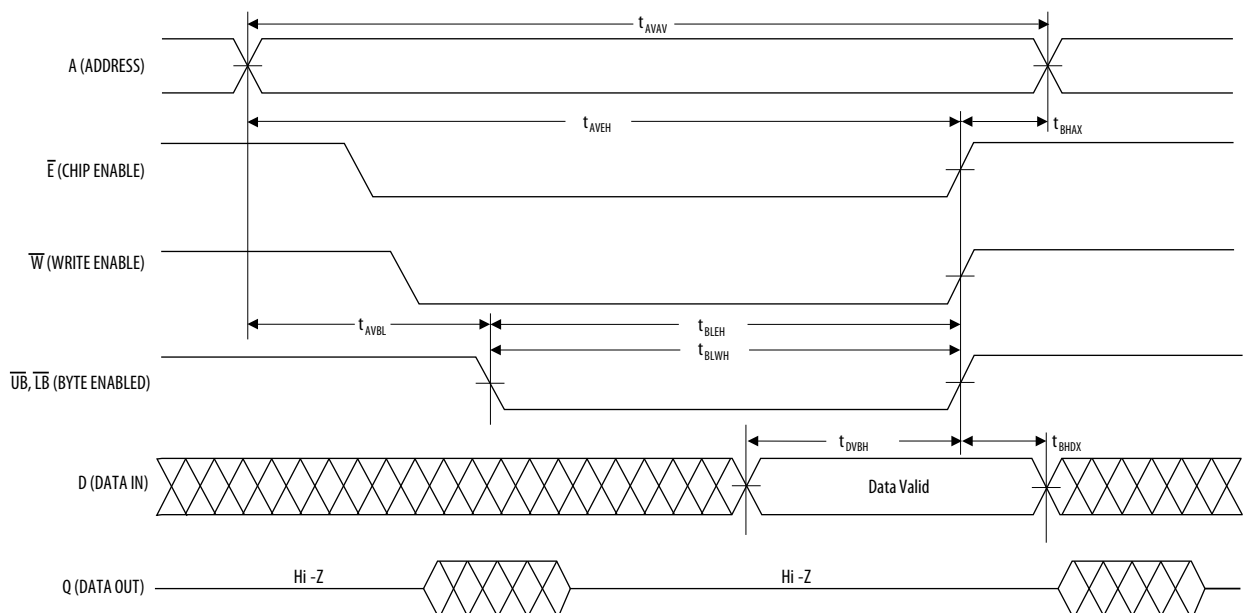
Table 12 – Write Cycle Timing 3 ($\overline{LB}/\overline{UB}$ Controlled)

| Symbol | Parameter ¹ | Min | Max | Unit |
|--------------------------|--|-----|-----|------|
| t_{AVAV} | Write cycle time ² | 35 | - | ns |
| t_{AVBL} | Address set-up time | 0 | - | ns |
| t_{AVBH} | Address valid to end of write (G high) | 18 | - | ns |
| | Address valid to end of write (G low) | 20 | - | ns |
| t_{BLEH} t_{BLWH} | Write pulse width (G high) | 15 | - | ns |
| t_{BLEH} t_{BLWH} | Write pulse width (G low) | 15 | - | ns |
| t_{DVBH} | Data valid to end of write | 10 | - | ns |
| t_{BHDX} | Data hold time | 0 | - | ns |
| t_{BHAX} | Write recovery time | 12 | - | ns |

Notes:

1. All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} , \overline{E} or $\overline{UB}/\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.

Figure 10 – Write Cycle Timing 3 ($\overline{UB}/\overline{LB}$ Controlled)



ORDERING INFORMATION

Table 13 – Part Numbering System

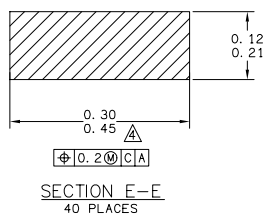
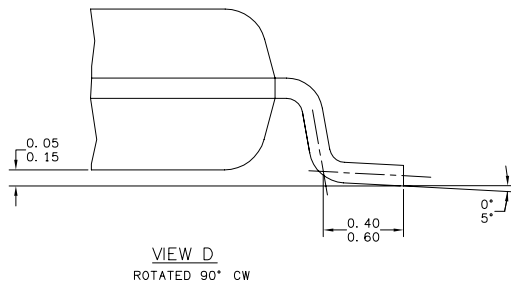
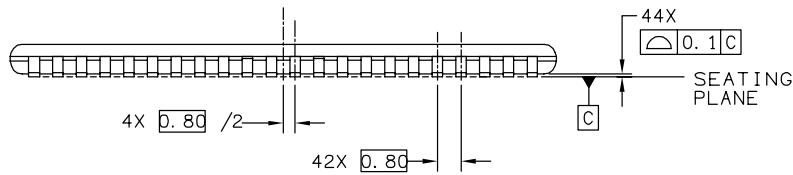
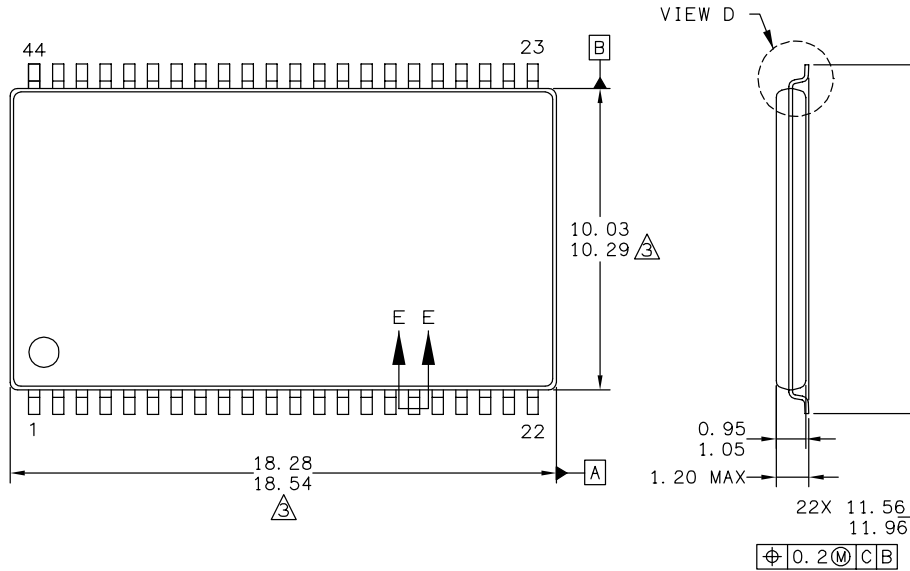
| | Memory | Density | Type | I/O Width | Rev. | Temp | Package | Speed | Packing | Grade |
|---|--------|--------------|-------|-----------|------|------|---------|-------|---------|-------|
| Example Ordering Part Number | MR | 0 | A | 16 | A | C | MA | 35 | R | |
| MRAM | MR | | | | | | | | | |
| 256 Kb | 256 | | | | | | | | | |
| 1 Mb | 0 | | | | | | | | | |
| 4 Mb | 2 | | | | | | | | | |
| 16 Mb | 4 | | | | | | | | | |
| Async 3.3v | A | | | | | | | | | |
| Async 3.3v Vdd and 1.8v Vddq | D | | | | | | | | | |
| Async 3.3v Vdd and 1.8v Vddq with 2.7v min. Vdd | DL | | | | | | | | | |
| 8-bit | 8 | | | | | | | | | |
| 16-bit | 16 | | | | | | | | | |
| Rev A | A | | | | | | | | | |
| Rev B | B | | | | | | | | | |
| Commercial | | 0 to 70°C | Blank | | | | | | | |
| Industrial | | -40 to 85°C | C | | | | | | | |
| Extended | | -40 to 105°C | V | | | | | | | |
| AEC Q-100 Grade 1 | | -40 to 125°C | M | | | | | | | |
| 44-TSOP-2 | YS | | | | | | | | | |
| 48-FBGA | MA | | | | | | | | | |
| 16-SOIC | SC | | | | | | | | | |
| 32-SOIC | SO | | | | | | | | | |
| 35 ns | 35 | | | | | | | | | |
| 45 ns | 45 | | | | | | | | | |
| Tray | Blank | | | | | | | | | |
| Tape and Reel | R | | | | | | | | | |
| Engineering Samples | ES | | | | | | | | | |
| Customer Samples | Blank | | | | | | | | | |
| Mass Production | Blank | | | | | | | | | |

Table 14 – MR0A16A Ordering Part Numbers

| Temp Grade | Temp | Package | Shipping | Ordering Part Number |
|------------------|----------------|----------|---------------|----------------------|
| Commercial | 0 to +70 °C | 44-TSOP2 | Tray | MR0A16AYS35 |
| | | | Tape and Reel | MR0A16AYS35R |
| | | 48-BGA | Tray | MR0A16AMA35 |
| | | | Tape and Reel | MR0A16AMA35R |
| Industrial | -40 to +85 °C | 44-TSOP2 | Tray | MR0A16ACYS35 |
| | | | Tape and Reel | MR0A16ACYS35R |
| | | 48-BGA | Tray | MR0A16ACMA35 |
| | | | Tape and Reel | MR0A16ACMA35R |
| Extended | -40 to +105 °C | 44-TSOP2 | Tray | MR0A16AVYS35 |
| | | | Tape and Reel | MR0A16AVYS35R |
| | | 48-BGA | Tray | MR0A16AVMA35 |
| | | | Tape and Reel | MR0A16AVMA35R |
| AEC-Q100 Grade 1 | -40 to 125 °C | 44-TSOP2 | Tray | MR0A16AMYS35 |
| | | | Tape and Reel | MR0A16AMYS35R |

PACKAGE OUTLINE DRAWINGS

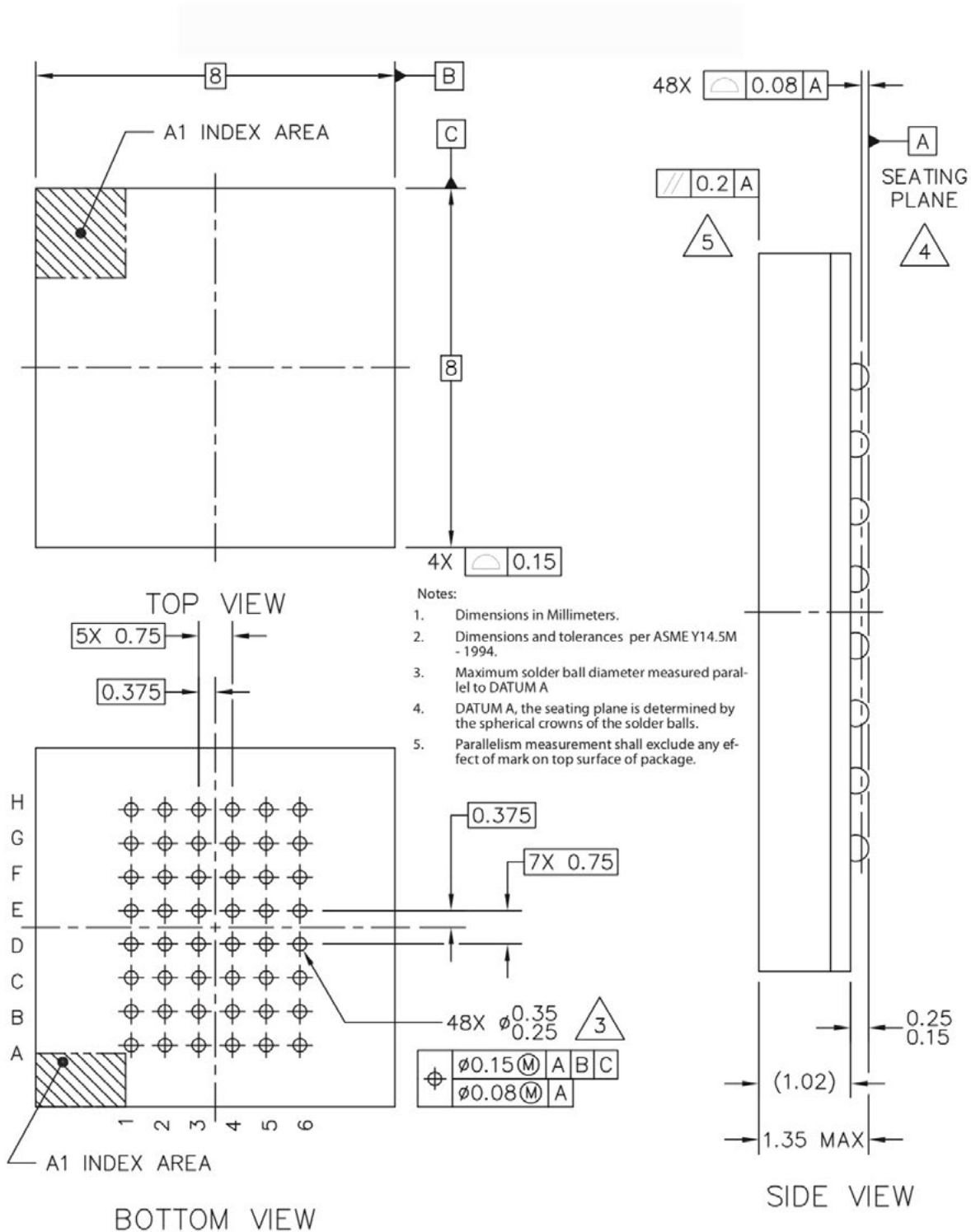
Figure 11 – 44-pin TSOP2



Notes:

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.
5. DAM Bar protrusion shall not cause the lead width to exceed 0.58.

Figure 12 – 48-ball BGA Package Outline



REVISION HISTORY

| Revision | Date | Description of Change |
|----------|-------------------|--|
| 0 | Jun 18, 2007 | Initial Advanced Information Release |
| 1 | Sept 21, 2007 | Table 6, Applied Values to TBD's in IDD Specifications |
| 2 | Nov 12, 2007 | Table 2, Changed IDDA to IDDR or IDDW |
| 3 | Sep 12, 2008 | Reformat Datasheet for EverSpin, Add BGA Packaging Information, Add Tape & Reel Part Numbers, Add Power Sequencing Info, Correct IOH spec of VOH to -100 uA, Correct ac Test Conditions. |
| 4 | Feb 28, 2011 | Add TSOPII Lead Cross-Section, Add Production Note. Converted to new document format. |
| 5 | Dec 9, 2011 | Figure 2.1 cosmetic update. Figure 5.2 BGA package outline drawing revised for ball size. Updated logo and contact information. |
| 6 | August 6, 2012 | Revised Table 1 and Figure 1 to be correct for x16 device. Revised magnetic immunity ratings for TSOP2 Industrial Grade. Revised figure 3. Complete document reformat and restructure. |
| 7 | October 14, 2013 | Added AEC-Q100 Grade 1 product option. |
| 8 | February 19, 2015 | Revised package outline for BGA. Ball size to 0.25 / 0.35 mm. |
| 8.1 | May 19, 2015 | Revised contact information on Contact Us page. |
| 8.2 | June 11, 2015 | Correction to Japan Sales Office telephone number. |
| 8.3 | March 23, 2018 | Revised contact information on Contact Us page. |

HOW TO CONTACT US

How to Reach Us:

Home Page:

www.everspin.com

World Wide Information Request

WW Headquarters - Chandler, AZ

5670 W. Chandler Blvd., Suite 100

Chandler, Arizona 85226

Tel: +1-877-480-MRAM (6726)

Local Tel: +1-480-347-1111

Fax: +1-480-347-1175

support@everspin.com

orders@everspin.com

sales@everspin.com

Europe, Middle East and Africa

Everspin Europe Support

support.europe@everspin.com

Japan

Everspin Japan Support

support.japan@everspin.com

Asia Pacific

Everspin Asia Support

support.asia@everspin.com

Filename:

EST00354_MR0A16A_Datasheet_Rev8.3032318

Everspin Technologies, Inc.

Information in this document is provided solely to enable system and software implementers to use Everspin Technologies products. There are no express or implied licenses granted hereunder to design or fabricate any integrated circuit or circuits based on the information in this document. Everspin Technologies reserves the right to make changes without further notice to any products herein. Everspin makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Everspin Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters, which may be provided in Everspin Technologies data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typicals" must be validated for each customer application by customer's technical experts. Everspin Technologies does not convey any license under its patent rights nor the rights of others. Everspin Technologies products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Everspin Technologies product could create a situation where personal injury or death may occur. Should Buyer purchase or use Everspin Technologies products for any such unintended or unauthorized application, Buyer shall indemnify and hold Everspin Technologies and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Everspin Technologies was negligent regarding the design or manufacture of the part. Everspin™ and the Everspin logo are trademarks of Everspin Technologies, Inc.

All other product or service names are the property of their respective owners.

Copyright © Everspin Technologies, Inc. 2018