Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MRF24J40
Data Sheet

IEEE 802.15.4™ 2.4 GHz
RF Transceiver

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

ISBN: 978-1-60932-459-9

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

MRF24J40

IEEE 802.15.4™ 2.4 GHz RF Transceiver

Features:

- IEEE 802.15.4™ Standard Compliant RF Transceiver
- Supports ZigBee®, MiWi™, MiWi P2P and Proprietary Wireless Networking Protocols
- Simple, 4-Wire Serial Peripheral Interface (SPI)
- Integrated 20 MHz and 32.768 kHz Crystal Oscillator Circuitry
- Low-Current Consumption:
  - RX mode: 19 mA (typical)
  - TX mode: 23 mA (typical)
  - Sleep: 2 μA (typical)
- Small, 40-Pin Leadless QFN 6x6 mm^2 Package

RF/Analog Features:

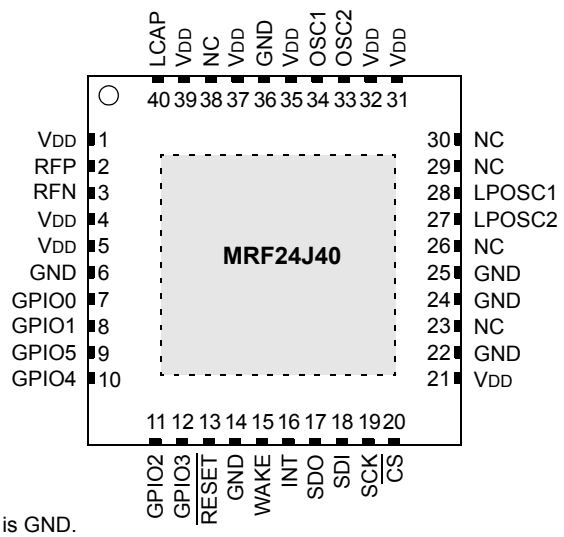
- ISM Band 2.405-2.48 GHz Operation
- Data Rate: 250 kbps (IEEE 802.15.4); 625 kbps (Turbo mode)
- -95 dBm Typical Sensitivity with +5 dBm Maximum Input Level
- +0 dBm Typical Output Power with 36 dB TX Power Control Range
- Differential RF Input/Output with Integrated TX/RX Switch
- Integrated Low Phase Noise VCO, Frequency Synthesizer and PLL Loop Filter
- Digital VCO and Filter Calibration
- Integrated RSSI ADC and I/Q DACs
- Integrated LDO
- High Receiver and RSSI Dynamic Range

MAC/Baseband Features:

- Hardware CSMA-CA Mechanism, Automatic Acknowledgement Response and FCS Check
- Independent Beacon, Transmit and GTS FIFO
- Supports all CCA modes and RSSI/ED
- Automatic Packet Retransmit Capability
- Hardware Security Engine (AES-128) with CTR, CCM and CBC-MAC modes
- Supports Encryption and Decryption for MAC Sublayer and Upper Layer

Pin Diagram:

40-Pin QFN



Note: Backside center pad is GND.

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com** or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

1.0 OVERVIEW

The MRF24J40 is an IEEE 802.15.4™ Standard compliant 2.4 GHz RF transceiver. It integrates the PHY and MAC functionality in a single chip solution. Figure 1-1 shows a simplified block diagram of a MRF24J40 wireless node. The MRF24J40 creates a low-cost, low-power, low data rate (250 or 625 kbps) Wireless Personal Area Network (WPAN) device. The MRF24J40 interfaces to many popular Microchip PIC® microcontrollers via a 4-wire serial SPI interface, interrupt, wake and Reset pins.

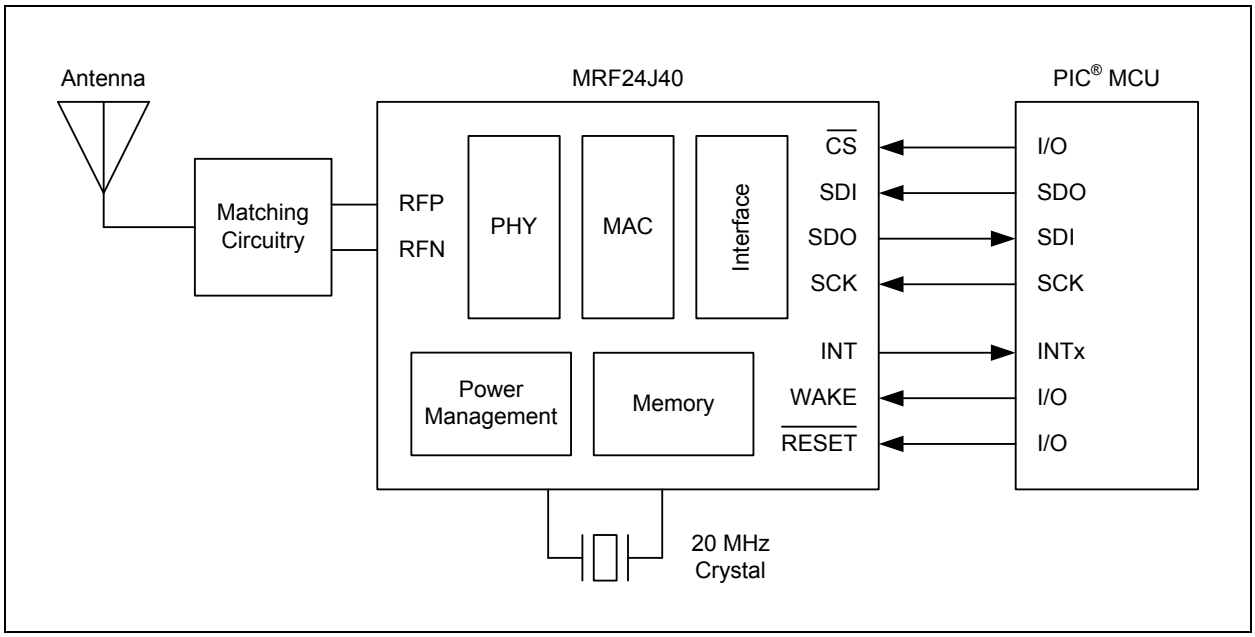
The MRF24J40 provides hardware support for:

- Energy Detection
- Carrier Sense
- Three CCA Modes
- CSMA-CA Algorithm
- Automatic Packet Retransmission
- Automatic Acknowledgment
- Independent Transmit, Beacon and GTS FIFO Buffers
- Security Engine supports Encryption and Decryption for MAC Sublayer and Upper Layer

These features reduce the processing load, allowing the use of low-cost 8-bit microcontrollers.

The MRF24J40 is compatible with Microchip's ZigBee®, MiWi™ and MiWi P2P software stacks. Each software stack is available as a free download, including source code, from the Microchip web site: http://www.microchip.com/wireless.

FIGURE 1-1: WIRELESS NODE BLOCK DIAGRAM

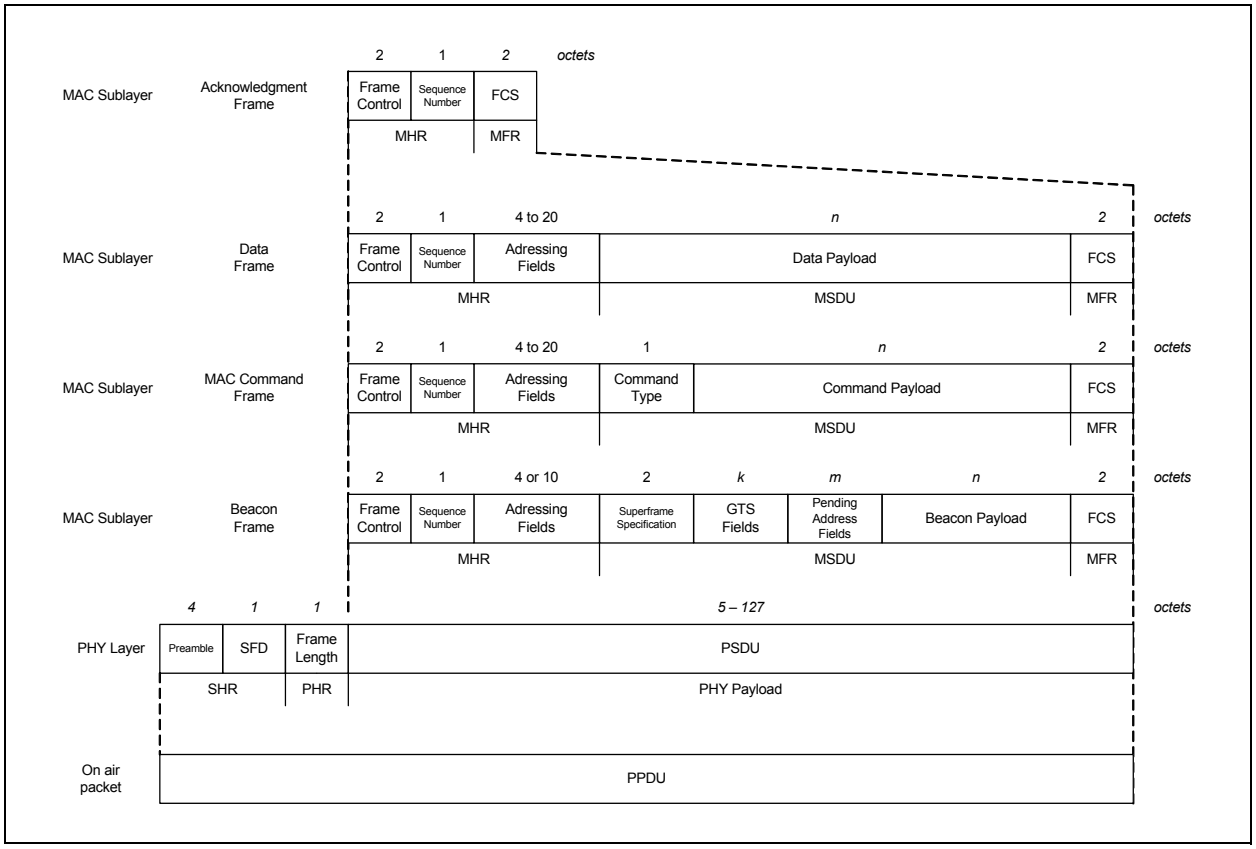


1.1 IEEE 802.15.4-2003 Standard

The MRF24J40 is compliant with the IEEE 802.15.4™-2003 Standard. The Standard specifies the physical (PHY) and Media Access Controller (MAC) functions that form the basis for a wireless network device. Figure 1-2 shows the structure of the PHY packet and MAC frame.

It is highly recommended that the design engineer be familiar with the IEEE 802.15.4-2003 Standard in order to best understand the configuration and operation of the MRF24J40. The Standard can be downloaded from the IEEE web site: http://www.ieee.org.

FIGURE 1-2: IEEE 802.15.4™ PHY PACKET AND MAC FRAME STRUCTURE



2.0 HARDWARE DESCRIPTION

2.1 2.1 Overview

The MRF24J40 is an IEEE 802.15.4 Standard compliant 2.4 GHz RF transceiver. It integrates the PHY and MAC functionality in a single chip solution. Figure 2-1 is a block diagram of the MRF24J40 circuitry.

A frequency synthesizer is clocked by an external 20 MHz crystal and generates a 2.4 GHz RF frequency.

The receiver is a low-IF architecture consisting of a Low Noise Amplifier (LNA), down conversion mixers, poly-phase channel filters and baseband limiting amplifiers with a Receiver Signal Strength Indicator (RSSI).

The transmitter is a direct conversion architecture with a 0 dBm maximum output (typical) and 36 dB power control range.

An internal Transmit/Receive (TR) switch combines the transmitter and receiver circuits into differential RFP and RFN pins. These pins are connected to impedance matching circuitry (balun) and antenna. An external Power Amplifier (PA) and/or LNA can be controlled via the GPIO pins.

Six General Purpose Input/Output (GPIO) pins can be configured for control or monitoring purposes. They can also be configured to control external PA/LNA RF switches.

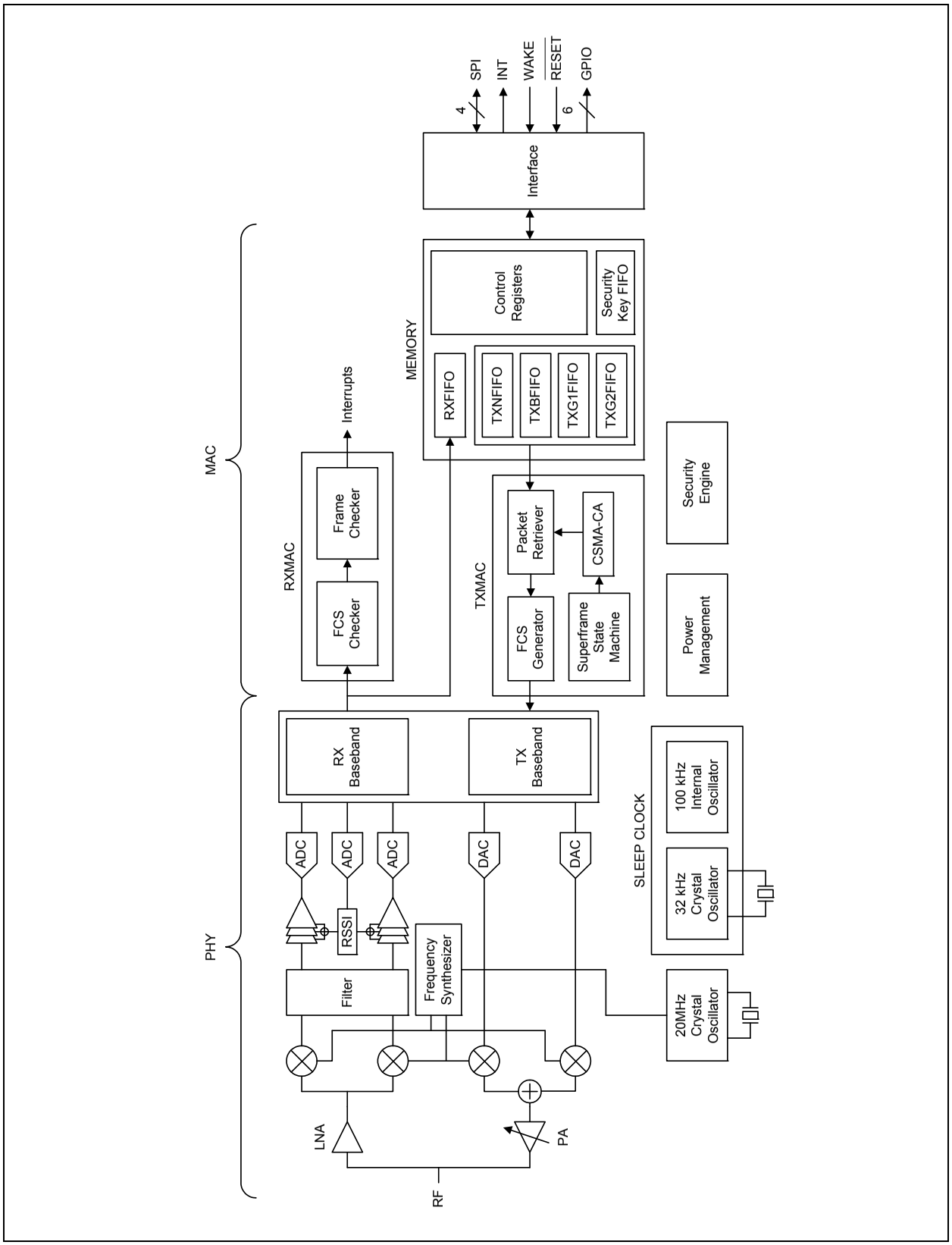
The power management circuitry consists of an integrated Low Dropout (LDO) voltage regulator. The MRF24J40 can be placed into a very low-current (2 μA typical) Sleep mode. An internal 100 kHz oscillator or 32 kHz external crystal oscillator can be used for Sleep mode timing.

The Media Access Controller (MAC) circuitry verifies reception and formats for transmission IEEE 802.15.4 Standard compliant packets. Data is buffered in Transmit and Receive FIFOs. Carrier Sense Multiple Access-Collision Avoidance (CSMA-CA), superframe constructor, receive frame filter and security engine functionality are implemented in hardware. The security engine provides hardware circuitry for AES-128 with CTR, CCM and CBC-MAC modes.

Control of the transceiver is via a 4-wire SPI, interrupt, wake and Reset pins.

2.2 Block Diagram

FIGURE 2-1: MRF24J40 ARCHITECTURE BLOCK DIAGRAM



2.3 Pin Descriptions

TABLE 2-1: MRF24J40 PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	VDD	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
2	RFP	AIO	Differential RF input/output (+).
3	RFN	AIO	Differential RF input/output (-).
4	VDD	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
5	VDD	Power	Guard ring power supply. Bypass with a capacitor as close to the pin as possible.
6	GND	Ground	Guard ring ground.
7	GPIO0	DIO	General purpose digital I/O, also used as external PA enable.
8	GPIO1	DIO	General purpose digital I/O, also used as external TX/RX switch control.
9	GPIO5	DIO	General purpose digital I/O.
10	GPIO4	DIO	General purpose digital I/O.
11	GPIO2	DIO	General purpose digital I/O, also used as external TX/RX switch control.
12	GPIO3	DIO	General purpose digital I/O.
13	$\overline{\text{RESET}}$	DI	Global hardware Reset pin active-low.
14	GND	Ground	Ground for digital circuit.
15	WAKE	DI	External wake-up trigger (must be enabled in software).
16	INT	DO	Interrupt pin to microcontroller.
17	SDO	DO	Serial interface data output from MRF24J40.
18	SDI	DI	Serial interface data input to MRF24J40.
19	SCK	DI	Serial interface clock.
20	$\overline{\text{CS}}$	DI	Serial interface enable.
21	VDD	Power	Digital circuit power supply. Bypass with a capacitor as close to the pin as possible.
22	GND	Ground	Ground for digital circuit.
23	NC	—	No Connection.
24	GND	Ground	Ground for digital circuit.
25	GND	Ground	Ground for digital circuit.
26	NC	—	No Connection. (Allow pin to float; do not connect signal.)
27	LPOSC2	AI	32 kHz crystal input.
28	LPOSC1	AI	32 kHz crystal input.
29	NC	—	No Connection. (Allow pin to float; do not connect signal.)
30	NC	—	No Connection. (Allow pin to float; do not connect signal.)
31	VDD	Power	Power supply for band gap reference circuit. Bypass with a capacitor as close to the pin as possible.
32	VDD	Power	Power supply for analog circuit. Bypass with a capacitor as close to the pin as possible.
33	OSC2	AI	20 MHz crystal input.
34	OSC1	AI	20 MHz crystal input.
35	VDD	Power	PLL power supply. Bypass with a capacitor as close to the pin as possible.
36	GND	Ground	Ground for PLL.
37	VDD	Power	Charge pump power supply. Bypass with a capacitor as close to the pin as possible.
38	NC	—	No Connection.
39	VDD	Power	VCO supply. Bypass with a capacitor as close to the pin as possible.
40	LCAP	—	PLL loop filter external capacitor. Connected to external 100 pF capacitor.

Legend: A = Analog, D = Digital, I = Input, O = Output

2.4 Power and Ground Pins

Recommended bypass capacitors are listed in Table 2-2. VDD pins 1 and 31 require two bypass capacitors to ensure sufficient bypass decoupling. Minimize trace length from the VDD pin to the bypass capacitors and make them as short as possible.

TABLE 2-2: RECOMMENDED BYPASS CAPACITOR VALUES

VDD Pin	Bypass Capacitor
1	47 pF and 0.01 µF
4	47 pF
5	0.1 µF
21	0.01 µF
31	47 pF and 0.01 µF
32	47 pF
35	47 pF
37	0.01 µF
39	1 µF

2.5 20 MHz Main Oscillator

The 20 MHz main oscillator provides the main frequency (MAINCLK) signal to internal RF, baseband and MAC circuitry. An external 20 MHz quartz crystal is connected to the OSC1 and OSC2 pins as shown in Figure 2-2. The crystal parameters are listed in Table 2-3.

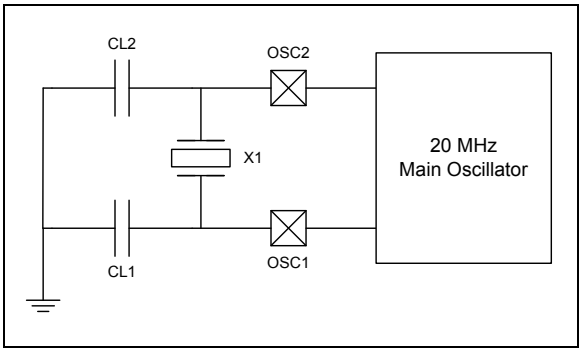
TABLE 2-3: 20 MHz CRYSTAL PARAMETERS(1)

Parameter	Value
Frequency	20 MHz
Frequency Tolerance at 25°C	±20 ppm(2)
Frequency Stability over Operating Temperature Range	±20 ppm(2)
Mode	Fundamental
Load Capacitance	10-15 pF
ESR	80Ω max.

Note 1: These values are for design guidance only.

2: IEEE 802.15.4™ Standard specifies transmitted center frequency tolerance shall be ±40 ppm maximum.

FIGURE 2-2: 20 MHz MAIN OSCILLATOR CRYSTAL CIRCUIT



2.6 Phase-Locked Loop

The Phase-Locked Loop (PLL) circuitry requires one external capacitor connected to pin 40 (LCAP). The recommended value is 100 pF. The PCB layout around the capacitor and pin 40 should be designed carefully such as to minimize interference to the PLL.

2.7 32 kHz External Crystal Oscillator

The 32 kHz external crystal oscillator provides one of two Sleep clock (SLPCLK) frequencies to Sleep mode counters. The Sleep mode counters time the Beacon Interval (BI) and inactive period for a beacon-enabled device and the Sleep interval for a nonbeacon-enabled device. Refer to **Section 3.15 "Sleep"** for more information.

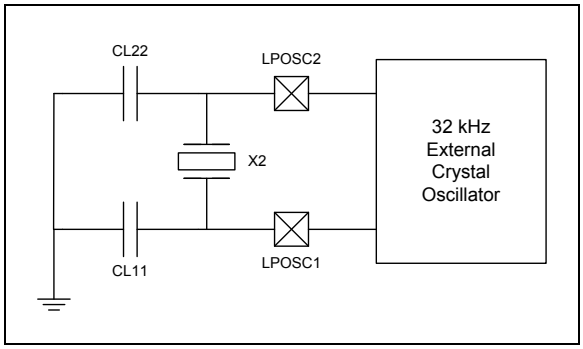
The SLPCLK frequency is selectable between the 32 kHz external crystal oscillator or 100 kHz internal oscillator. The 32 kHz external crystal oscillator provides better frequency accuracy and stability than the 100 kHz internal oscillator. An external 32 kHz tuning fork crystal is connected to the LPOSC1 and LPOSC2 pins, as shown in Figure 2-3. The crystal parameters are listed in Table 2-4.

TABLE 2-4: 32 kHz CRYSTAL PARAMETERS(1)

Parameter	Value
Frequency	32.768 kHz
Frequency Tolerance	±20 ppm
Load Capacitance	12.5 pF
ESR	70 kΩ max.

Note 1: These values are for design guidance only.

FIGURE 2-3: 32 kHz EXTERNAL OSCILLATOR CRYSTAL CIRCUIT



2.8 100 kHz Internal Oscillator

The 100 kHz internal oscillator requires no external components and provides one of two Sleep clock (SLPCLK) frequencies to Sleep mode counters. The Sleep mode counters time the Beacon Interval (BI) and inactive period for a beacon-enabled device and the Sleep interval for a nonbeacon-enabled device. Refer to **Section 3.15 "Sleep"** for more information.

The SLPCLK frequency is selectable between the 32 kHz external crystal oscillator or 100 kHz internal oscillator. The 32 kHz external crystal oscillator provides better frequency accuracy and stability than the 100 kHz internal oscillator. It is recommended that the 100 kHz internal oscillator be calibrated before use. The calibration procedure is given in **Section 3.15.1.2 "Sleep Clock Calibration"**.

2.9 Reset ($\overline{\text{RESET}}$) Pin

An external hardware Reset can be performed by asserting the $\overline{\text{RESET}}$ pin 13 low. The MRF24J40 will be released from Reset approximately 250 µs after the $\overline{\text{RESET}}$ pin is released. The $\overline{\text{RESET}}$ pin has an internal weak pull-up resistor.

2.10 Interrupt (INT) Pin

The Interrupt (INT) pin 16 provides an interrupt signal to the host microcontroller from the MRF24J40. The polarity is configured via the INTEDGE bit in the SLPCON0 (0x211<1>) register. Interrupts have to be enabled and unmasked before the INT pin is active. Refer to **Section 3.3 "Interrupts"** for a functional description of interrupts.

Note:	The INTEDGE polarity defaults to, 0 = Falling Edge. Ensure that the interrupt polarity matches the interrupt pin polarity on the host microcontroller.

Note:	The INT pin will remain high or low, depending on INTEDGE polarity setting, until INSTAT register is read.

2.11 Wake (WAKE) Pin

The Wake (WAKE) pin 15 provides an external wake-up signal to the MRF24J40 from the host microcontroller. It is used in conjunction with the Sleep modes of the MRF24J40. The WAKE pin is disabled by default. Refer to **Section 3.15.2 "Immediate Sleep and Wake-up Mode"** for a functional description of the Immediate Sleep and Wake-up modes.

2.12 General Purpose Input/Output (GPIO) Pins

Six GPIO pins can be configured individually for control or monitoring purposes. Input or output selection is configured by the TRISGPIO (0x34) register. GPIO data can be read/written to via the GPIO (0x33) register.

The GPIO pins have limited output drive capability. Table 2-5 lists the individual GPIO pin source current limits.

TABLE 2-5: GPIO SOURCE CURRENT LIMITS

Pin	Maximum Current Sourced
GPIO0	4 mA
GPIO1	1 mA
GPIO2	1 mA
GPIO3	1 mA
GPIO4	1 mA
GPIO5	1 mA

GPIO0, GPIO1 and GPIO2 can be configured to control external PA, LNA and RF switches by the internal RF state machine. This allows the external PA and LNA to be controlled by the MRF24J40 without any host microcontroller intervention. Refer to **Section 4.2 "External PA/LNA Control"** for control register configuration, timing diagrams and application information.

2.13 Serial Peripheral Interface (SPI) Port Pins

The MRF24J40 communicates with a host micro-controller via a 4-wire SPI port as a slave device. The MRF24J40 supports SPI (mode 0,0) which requires that SCK idles in a low state. The $\overline{CS}$ pin must be held low while communicating with the MRF24J40. Figure 2-4 shows timing for a write operation. Data is received by the MRF24J40 via the SDI pin and is clocked in on the rising edge of SCK. Figure 2-5 shows timing for a read operation. Data is sent by the MRF24J40 via the SDO pin and is clocked out on the falling edge of SCK.

Note: The $\overline{SDO}$ pin 17 defaults to a low state when $\overline{CS}$ is high (the MRF24J40 is not selected). If the MRF24J40 is to share a SPI bus, a tri-state buffer should be placed on the SDO signal to provide a high-impedance signal to the SPI bus. See **Section 4.4 "MRF24J40 Schematic and Bill of Materials"** for an example application circuit.

FIGURE 2-4: SPI PORT WRITE (INPUT) TIMING

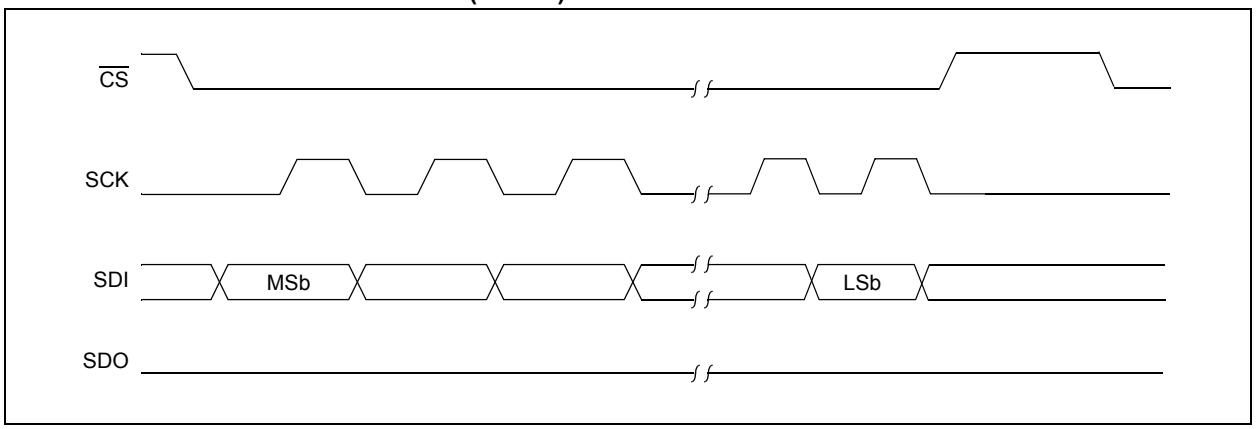
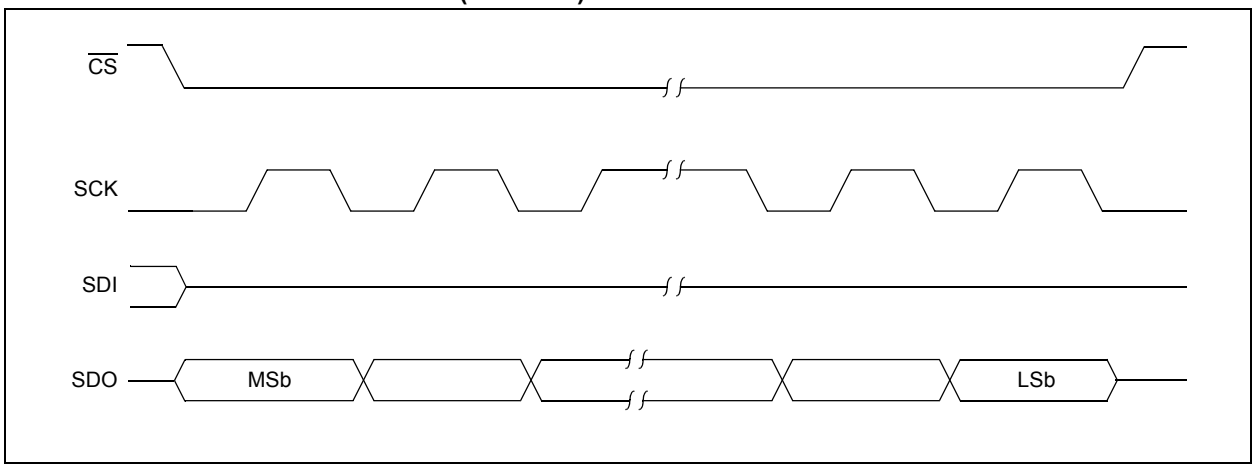


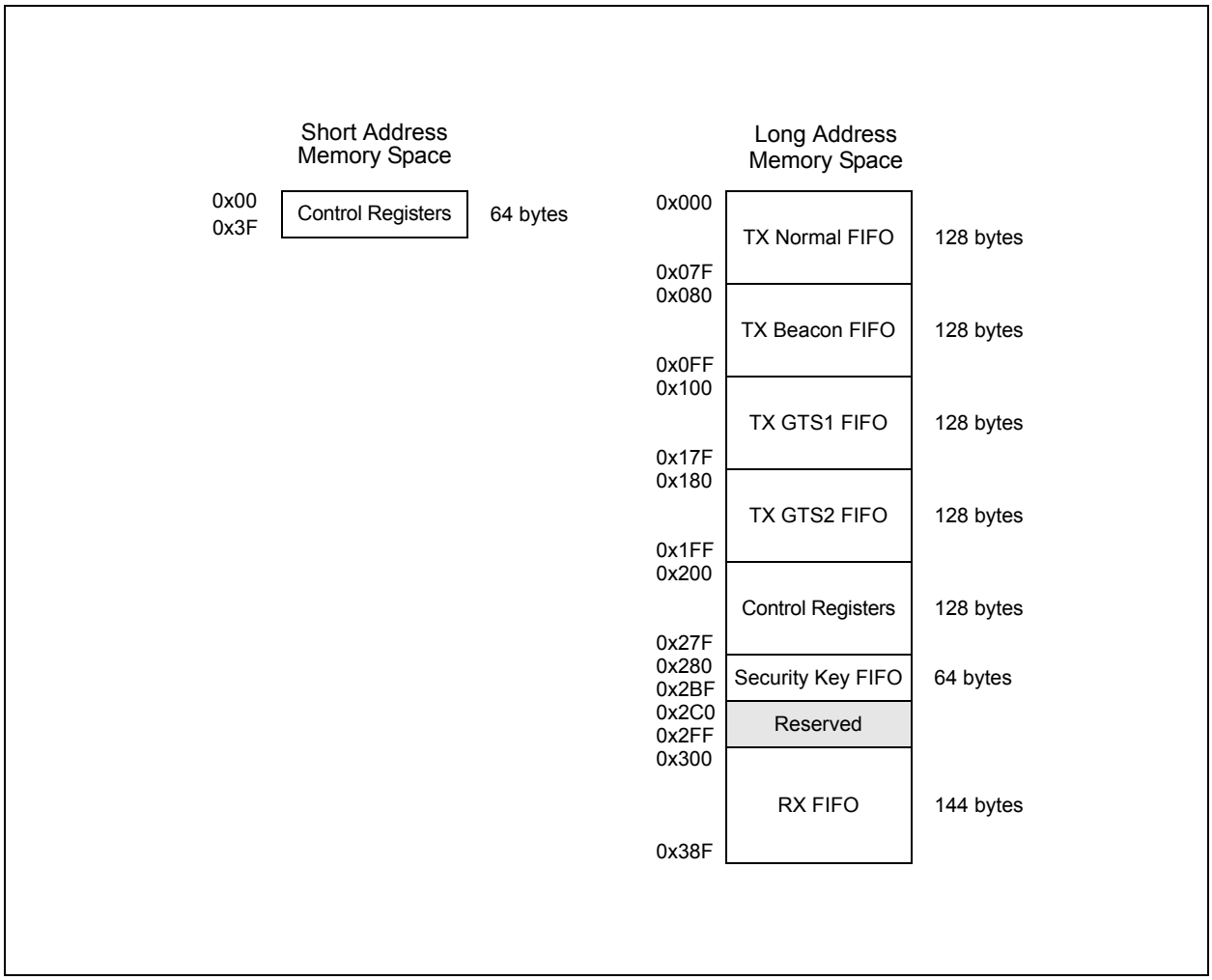
FIGURE 2-5: SPI PORT READ (OUTPUT) TIMING



2.14 Memory Organization

Memory in the MRF24J40 is implemented as static RAM and is accessible via the SPI port. Memory is functionally divided into control registers and data buffers (FIFOs), as shown in Figure 2-6. Control registers provide control, status and device addressing for MRF24J40 operations. FIFOs serve as temporary buffers for data transmission, reception and security keys. Memory is accessed via two addressing methods: Short and Long.

FIGURE 2-6: MEMORY MAP FOR MRF24J40



2.14.1 SHORT ADDRESS REGISTER INTERFACE

The short address memory space contains control registers with a 6-bit address range of 0x00 to 0x3F. Figure 2-7 shows a short address read and Figure 2-8 shows a short address write. The 8-bit SPI transfer begins with a '0' to indicate a short address transaction. It is followed by the 6-bit register address, Most Significant bit (MSb) first. The 8th bit indicates if it is a read ('0') or write ('1') transaction.

FIGURE 2-7: SHORT ADDRESS READ

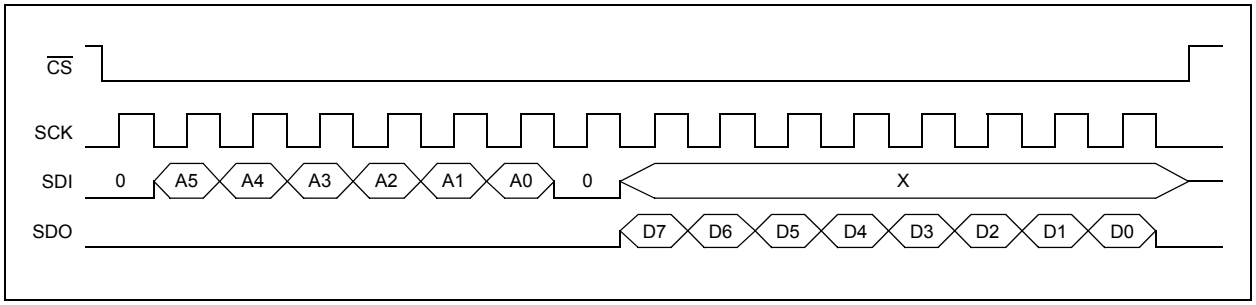
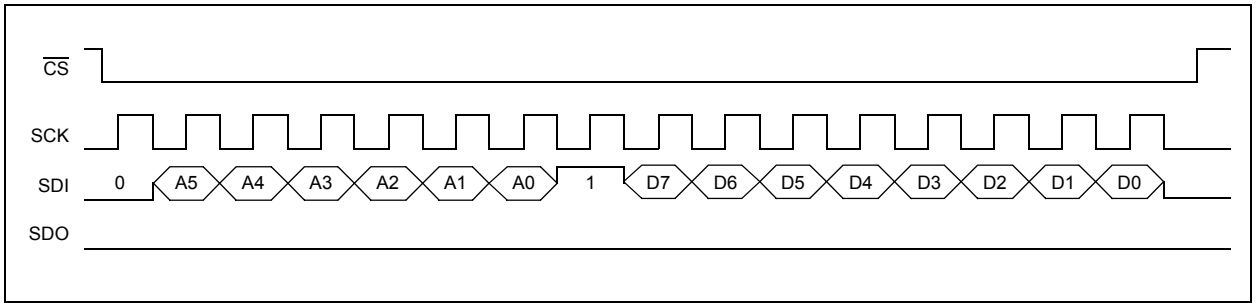


FIGURE 2-8: SHORT ADDRESS WRITE



2.14.2 LONG ADDRESS REGISTER INTERFACE

The long address memory space contains control registers and FIFOs with a 10-bit address range of 0x000 to 0x38F. Figure 2-9 shows a long address read and Figure 2-10 shows a long address write. The 12-bit SPI transfer begins with a '1' to indicate a long address transaction. It is followed by the 10-bit register address, Most Significant bit (MSb) first. The 12th bit indicates if it is a read ('0') or write ('1') transaction.

FIGURE 2-9: LONG ADDRESS READ

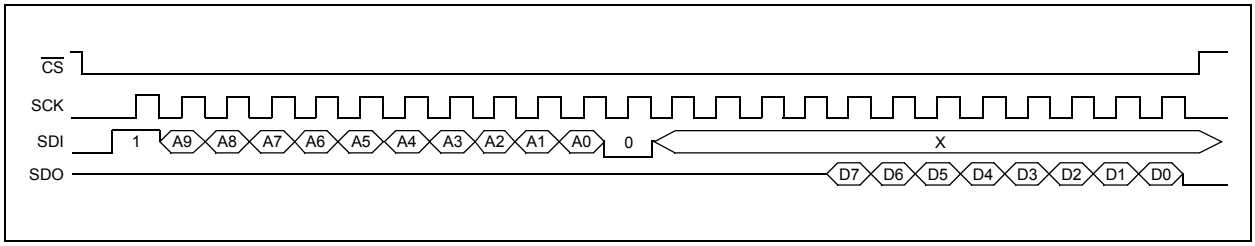
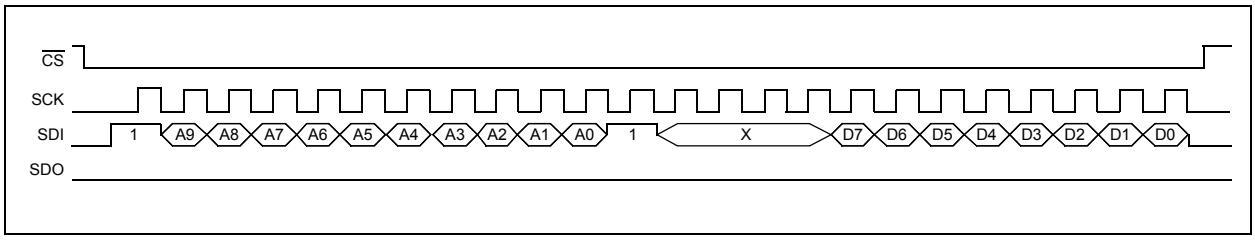


FIGURE 2-10: LONG ADDRESS WRITE



2.15 Control Register Description

Control registers provide control, status and device addressing for MRF24J40 operations. The following figures, tables and register definitions describe the control register operation.

2.15.1 CONTROL REGISTER MAP

FIGURE 2-11: SHORT ADDRESS CONTROL REGISTER MAP FOR MRF24J40

0x00	RXMCR	0x10	ORDER	0x20	ESLOTG67	0x30	RXSR
0x01	PANIDL	0x11	TXMCR	0x21	TXPEND	0x31	INTSTAT
0x02	PANIDH	0x12	ACKTMOUT	0x22	WAKECON	0x32	INTCON
0x03	SADRL	0x13	ESLOTG1	0x23	FRMOFFSET	0x33	GPIO
0x04	SADRH	0x14	SYMTICKL	0x24	TXSTAT	0x34	TRISGPIO
0x05	EADR0	0x15	SYMTICKH	0x25	TXBCON1	0x35	SLPACK
0x06	EADR1	0x16	PACON0	0x26	GATECLK	0x36	RFCTL
0x07	EADR2	0x17	PACON1	0x27	TXTIME	0x37	SECCR2
0x08	EADR3	0x18	PACON2	0x28	HSYMTMRL	0x38	BBREG0
0x09	EADR4	0x19	Reserved	0x29	HSYMTMRH	0x39	BBREG1
0x0A	EADR5	0x1A	TXBCON0	0x2A	SOFTRST	0x3A	BBREG2
0x0B	EADR6	0x1B	TXNCON	0x2B	Reserved	0x3B	BBREG3
0x0C	EADR7	0x1C	TXG1CON	0x2C	SECCON0	0x3C	BBREG4
0x0D	RXFLUSH	0x1D	TXG2CON	0x2D	SECCON1	0x3D	Reserved
0x0E	Reserved	0x1E	ESLOTG23	0x2E	TXSTBL	0x3E	BBREG6
0x0F	Reserved	0x1F	ESLOTG45	0x2F	Reserved	0x3F	CCAEDTH

FIGURE 2-12: LONG ADDRESS CONTROL REGISTER MAP FOR MRF24J40

0x200	RFCON0	0x210	RSSI	0x220	SLPCON1	0x230	ASSOEADR0	0x240	UPNONCE0
0x201	RFCON1	0x211	SLPCON0	0x221	Reserved	0x231	ASSOEADR1	0x241	UPNONCE1
0x202	RFCON2	0x212	Reserved	0x222	WAKETIMEL	0x232	ASSOEADR2	0x242	UPNONCE2
0x203	RFCON3	0x213	Reserved	0x223	WAKETIMEH	0x233	ASSOEADR3	0x243	UPNONCE3
0x204	Reserved	0x214	Reserved	0x224	REMCNTL	0x234	ASSOEADR4	0x244	UPNONCE4
0x205	RFCON5	0x215	Reserved	0x225	REMCNTH	0x235	ASSOEADR5	0x245	UPNONCE5
0x206	RFCON6	0x216	Reserved	0x226	MAINCNT0	0x236	ASSOEADR6	0x246	UPNONCE6
0x207	RFCON7	0x217	Reserved	0x227	MAINCNT1	0x237	ASSOEADR7	0x247	UPNONCE7
0x208	RFCON8	0x218	Reserved	0x228	MAINCNT2	0x238	ASSOSADR0	0x248	UPNONCE8
0x209	SLPCAL0	0x219	Reserved	0x229	MAINCNT3	0x239	ASSOSADR1	0x249	UPNONCE9
0x20A	SLPCAL1	0x21A	Reserved	0x22A	Reserved	0x23A	Reserved	0x24A	UPNONCE10
0x20B	SLPCAL2	0x21B	Reserved	0x22B	Reserved	0x23B	Reserved	0x24B	UPNONCE11
0x20C	Reserved	0x21C	Reserved	0x22C	Reserved	0x23C	Unimplemented	0x24C	UPNONCE12
0x20D	Reserved	0x21D	Reserved	0x22D	Reserved	0x23D	Unimplemented		
0x20E	Reserved	0x21E	Reserved	0x22E	Reserved	0x23E	Unimplemented		
0x20F	RFSTATE	0x21F	Reserved	0x22F	TESTMODE	0x23F	Unimplemented		

2.15.2 CONTROL REGISTER SUMMARY

TABLE 2-6: SHORT ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x00	RXMCR	r	r	NOACKRSP	r	PANCOORD	COORD	ERRPKT	PROMI	0000 0000	22
0x01	PANIDL	PAN ID Low Byte (PANIDL<7:0>)								0000 0000	23
0x02	PANIDH	PAN ID High Byte (PANIDH<15:8>)								0000 0000	23
0x03	SADRL	Short Address Low Byte (SADRL<7:0>)								0000 0000	24
0x04	SADRH	Short Address High Byte (SADRH<15:8>)								0000 0000	24
0x05	EADR0	64-Bit Extended Address bits (EADR0<7:0>)								0000 0000	25
0x06	EADR1	64-Bit Extended Address bits (EADR1<15:8>)								0000 0000	25
0x07	EADR2	64-Bit Extended Address bits (EADR2<23:16>)								0000 0000	25
0x08	EADR3	64-Bit Extended Address bits (EADR3<31:24>)								0000 0000	26
0x09	EADR4	64-Bit Extended Address bits (EADR4<39:32>)								0000 0000	26
0x0A	EADR5	64-Bit Extended Address bits (EADR5<47:40>)								0000 0000	26
0x0B	EADR6	64-Bit Extended Address bits (EADR6<55:48>)								0000 0000	27
0x0C	EADR7	64-Bit Extended Address bits (EADR7<63:56>)								0000 0000	27
0x0D	RXFLUSH	r	WAKEPOL	WAKEPAD	r	CMDONLY	DATAONLY	BCNONLY	RXFLUSH	0000 0000	28
0x0E	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x0F	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x10	ORDER	BO3	BO2	BO1	BO0	SO3	SO2	SO1	SO0	1111 1111	29
0x11	TXMCR	NOCSMA	BATLIFEXT	SLOTTED	MACMINBE1	MACMINBE0	CSMABF2	CSMABF1	CSMABF0	0001 1100	30
0x12	ACKTMOUT	DRPACK	MAWD6	MAWD5	MAWD4	MAWD3	MAWD2	MAWD1	MAWD0	0011 1001	31
0x13	ESLOTG1	GTS1-3	GTS1-2	GTS1-1	GTS1-0	CAP3	CAP2	CAP1	CAP0	0000 0000	32
0x14	SYMTICKL	TICKP7	TICKP6	TICKP5	TICKP4	TICKP3	TICKP2	TICKP1	TICKP0	0100 0000	33
0x15	SYMTICKH	TXONT6	TXONT5	TXONT4	TXONT3	TXONT2	TXONT1	TXONT0	TICKP8	0101 0001	33
0x16	PACON0	PAONT7	PAONT6	PAONT5	PAONT4	PAONT3	PAONT2	PAONT1	PAONT0	0010 1001	34
0x17	PACON1	r	r	r	PAONTS3	PAONTS2	PAONTS1	PAONTS0	PAONT8	0000 0010	34
0x18	PACON2	FIFOEN	r	TXONTS3	TXONTS2	TXONTS1	TXONTS0	TXONT8	TXONT7	1000 1000	35
0x19	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x1A	TXBCON0	r	r	r	r	r	r	TXBSECEN	TXBTRIG	0000 0000	36
0x1B	TXNCON	r	r	r	FPSTAT	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG	0000 0000	37
0x1C	TXG1CON	TXG1RETRY1	TXG1RETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG	0000 0000	38
0x1D	TXG2CON	TXG2RETRY1	TXG2RETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG	0000 0000	38

Legend: r = reserved

TABLE 2-6: SHORT ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40 (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x1E	ESLOTG23	GTS3-3	GTS3-2	GTS3-1	GTS3-0	GTS2-3	GTS2-2	GTS2-1	GTS2-0	0000 0000	39
0x1F	ESLOTG45	GTS5-3	GTS5-2	GTS5-1	GTS5-0	GTS4-3	GTS4-2	GTS4-1	GTS4-0	0000 0000	39
0x20	ESLOTG67	r	r	r	r	GTS6-3	GTS6-2	GTS6-1	GTS6-0	0000 0000	39
0x21	TXPEND	MLIFS5	MLIFS4	MLIFS3	MLIFS2	MLIFS1	MLIFS0	GTSSWITCH	FPACK	1000 0100	40
0x22	WAKECON	IMMWAKE	REGWAKE	INTL	INTL	INTL	INTL	INTL	INTL	0000 0000	41
0x23	FRMOFFSET	OFFSET7	OFFSET6	OFFSET5	OFFSET4	OFFSET3	OFFSET2	OFFSET1	OFFSET0	0000 0000	42
0x24	TXSTAT	TXNRETRY1	TXNRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2STAT	TXG1STAT	TXNSTAT	0000 0000	43
0x25	TXBCON1	TXBMSK	$\overline{\text{WU}}$/BCN	RSSINUM1	RSSINUM0	r	r	r	r	0011 0000	44
0x26	GATECLK	r	r	r	r	GTSON	r	r	r	0000 0000	45
0x27	TXTIME	TURNTIME3	TURNTIME2	TURNTIME1	TURNTIME0	r	r	r	r	0100 1000	46
0x28	HSYMTMRL	HSYMTMR7	HSYMTMR6	HSYMTMR5	HSYMTMR4	HSYMTMR3	HSYMTMR2	HSYMTMR1	HSYMTMR0	0000 0000	47
0x29	HSYMTMRH	HSYMTMR15	HSYMTMR14	HSYMTMR13	HSYMTMR12	HSYMTMR11	HSYMTMR10	HSYMTMR09	HSYMTMR08	0000 0000	47
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC	0000 0000	48
0x2B	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x2C	SECCON0	SECIGNORE	SECSTART	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPHER1	TXNCIPHER0	0000 0000	49
0x2D	SECCON1	r	TXBCIPHER2	TXBCIPHER1	TXBCIPHER0	r	r	DISDEC	DISENC	0000 0000	50
0x2E	TXSTBL	RFSTBL3	RFSTBL2	RFSTBL1	RFSTBL0	MSIFS3	MSIFS2	MSIFS1	MSIFS0	0111 0101	51
0x2F	Reserved	r	r	r	r	r	r	r	r	0000 0000	—

Legend: r = reserved

TABLE 2-6: SHORT ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40 (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x30	RXSR	r	UPSECERR	BATIND	r	r	SECDECERR	r	r	0000 0000	52
0x31	INTSTAT	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000	53
0x32	INTCON	SLPIE	WAKEIE	HSYMTMRIE	SECIE	RXIE	TXG2IE	TXG1IE	TXNIE	1111 1111	54
0x33	GPIO	r	r	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	0000 0000	55
0x34	TRISGPIO	r	r	TRISGP5	TRISGP4	TRISGP3	TRISGP2	TRISGP1	TRISGP0	0000 0000	55
0x35	SLPACK	SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0	0000 0000	56
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE	0000 0000	57
0x37	SECCR2	UPDEC	UPENC	TXG2CIPHER2	TXG2CIPHER1	TXG2CIPHER0	TXG1CIPHER2	TXG1CIPHER1	TXG1CIPHER0	0000 0000	58
0x38	BBREG0	r	r	r	r	r	r	r	TURBO	0000 0000	59
0x39	BBREG1	r	r	r	r	r	RXDECINV	r	r	0000 0000	59
0x3A	BBREG2	CCAMODE1	CCAMODE0	CCACSTH3	CCACSTH2	CCACSTH1	CCACSTH0	r	r	0100 1000	60
0x3B	BBREG3	PREVALIDTH3	PREVALIDTH2	PREVALIDTH1	PREVALIDTH0	PREDETTH2	PREDETTH1	PREDETTH0	r	1101 1000	60
0x3C	BBREG4	CSTH2	CSTH1	CSTH0	PRECNT2	PRECNT1	PRECNT0	r	r	1001 1100	61
0x3D	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x3E	BBREG6	RSSIMODE1	RSSIMODE2	r	r	r	r	r	RSSIRDY	0000 0001	61
0x3F	CCAEDTH	CCAEDTH7	CCAEDTH6	CCAEDTH5	CCAEDTH4	CCAEDTH3	CCAEDTH2	CCAEDTH1	CCAEDTH0	0000 0000	62

Legend: r = reserved

TABLE 2-7: LONG ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x200	RFCON0	CHANNEL3	CHANNEL2	CHANNEL1	CHANNEL0	RFOPT3	RFOPT2	RFOPT1	RFOPT0	0000 0000	63
0x201	RFCON1	VCOOPT7	VCOOPT6	VCOOPT5	VCOOPT4	VCOOPT3	VCOOPT2	VCOOPT1	VCOOPT0	0000 0000	63
0x202	RFCON2	PLLEN	r	r	r	r	r	r	r	0000 0000	64
0x203	RFCON3	TXPWRL1	TXPWRL0	TXPWRS2	TXPWRS1	TXPWRS0	r	r	r	0000 0000	64
0x204	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x205	RFCON5	BATTH3	BATTH2	BATTH1	BATTH0	r	r	r	r	0000 0000	65
0x206	RFCON6	TXFIL	r	r	20MRECVR	BATEN	r	r	r	0000 0000	65
0x207	RFCON7	SLPCLKSEL1	SLPCLKSEL0	r	r	r	r	CLKOUTMODE1	CLKOUTMODE0	0000 0000	66
0x208	RFCON8	r	r	r	RFVCO	r	r	r	r	0000 0000	66
0x209	SLPCAL0	SLPCAL7	SLPCAL6	SLPCAL5	SLPCAL4	SLPCAL3	SLPCAL2	SLPCAL1	SLPCAL0	0000 0000	67
0x20A	SLPCAL1	SLPCAL15	SLPCAL14	SLPCAL13	SLPCAL12	SLPCAL11	SLPCAL10	SLPCAL9	SLPCAL8	0000 0000	67
0x20B	SLPCAL2	SLPCALRDY	r	r	SLPCALEN	SLPCAL19	SLPCAL18	SLPCAL17	SLPCAL16	0000 0000	68
0x20C	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x20D	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x20E	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x20F	RFSTATE	RFSTATE2	RFSTATE1	RFSTATE0	r	r	r	r	r	0000 0000	69
0x210	RSSI	RSSI7	RSSI6	RSSI5	RSSI4	RSSI3	RSSI2	RSSI1	RSSI0	0000 0000	69
0x211	SLPCON0	r	r	r	r	r	r	INTEDGE	$\overline{\text{SLPCLKEN}}$	0000 0000	70
0x212	Reserved	r	r	r	r	r	r	r	r	0000 0000	—

Legend: r = reserved

TABLE 2-7: LONG ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40 (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x213	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x214	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x215	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x216	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x217	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x218	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x219	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21A	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21B	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21C	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21D	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21E	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x21F	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x220	SLPCON1	r	r	$\overline{\text{CLKOUTEN}}$	SLPCLKDIV4	SLPCLKDIV3	SLPCLKDIV2	SLPCLKDIV1	SLPCLKDIV0	0000 0000	70
0x221	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x222	WAKETIMEL	WAKETIME7	WAKETIME6	WAKETIME5	WAKETIME4	WAKETIME3	WAKETIME2	WAKETIME1	WAKETIME0	0000 1010	71
0x223	WAKETIMEH	r	r	r	r	r	WAKETIME10	WAKETIME9	WAKETIME8	0000 0000	71
0x224	REMCNTL	REMCNT7	REMCNT6	REMCNT5	REMCNT4	REMCNT3	REMCNT2	REMCNT1	REMCNT0	0000 0000	72
0x225	REMCNTH	REMCNT15	REMCNT14	REMCNT13	REMCNT12	REMCNT11	REMCNT10	REMCNT9	REMCNT8	0000 0000	72
0x226	MAINCNT0	MAINCNT7	MAINCNT6	MAINCNT5	MAINCNT4	MAINCNT3	MAINCNT2	MAINCNT1	MAINCNT0	0000 0000	73
0x227	MAINCNT1	MAINCNT15	MAINCNT14	MAINCNT13	MAINCNT12	MAINCNT11	MAINCNT10	MAINCNT9	MAINCNT8	0000 0000	73
0x228	MAINCNT2	MAINCNT23	MAINCNT22	MAINCNT21	MAINCNT20	MAINCNT19	MAINCNT18	MAINCNT17	MAINCNT16	0000 0000	74
0x229	MAINCNT3	STARTCNT	r	r	r	r	r	MAINCNT25	MAINCNT24	0000 0000	74
0x22A	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22B	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22C	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22D	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22E	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x22F	TESTMODE	r	r	r	RSSIWAIT1	RSSIWAIT0	TESTMODE2	TESTMODE1	TESTMODE0	0000 0000	75
0x230	ASSOEADR0	ASSOEADR0<7:0>								0000 0000	76
0x231	ASSOEADR1	ASSOEADR1<15:8>								0000 0000	76
0x232	ASSOEADR2	ASSOEADR2<23:16>								0000 0000	77
0x233	ASSOEADR3	ASSOEADR3<31:24>								0000 0000	77
0x234	ASSOEADR4	ASSOEADR4<39:32>								0000 0000	78
0x235	ASSOEADR5	ASSOEADR5<47:40>								0000 0000	78
0x236	ASSOEADR6	ASSOEADR6<55:48>								0000 0000	79
0x237	ASSOEADR7	ASSOEADR7<63:56>								0000 0000	79
0x238	ASSOSADR0	ASSOSADR0<7:0>								0000 0000	80
0x239	ASSOSADR1	ASSOSADR1<15:8>								0000 0000	80
0x23A	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x23B	Reserved	r	r	r	r	r	r	r	r	0000 0000	—
0x23C	Unimple-mented	—	—	—	—	—	—	—	—	---- ----	—
0x23D	Unimple-mented	—	—	—	—	—	—	—	—	---- ----	—
0x23E	Unimple-mented	—	—	—	—	—	—	—	—	---- ----	—
0x23F	Unimple-mented	—	—	—	—	—	—	—	—	---- ----	—
0x240	UPNONCE0	UPNONCE<7:0>								0000 0000	81
0x241	UPNONCE1	UPNONCE<15:8>								0000 0000	81
0x242	UPNONCE2	UPNONCE<23:16>								0000 0000	82
0x243	UPNONCE3	UPNONCE<31:24>								0000 0000	82
0x244	UPNONCE4	UPNONCE<39:32>								0000 0000	83
0x245	UPNONCE5	UPNONCE<47:40>								0000 0000	83

Legend: r = reserved

TABLE 2-7: LONG ADDRESS CONTROL REGISTER SUMMARY FOR MRF24J40 (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on Page:
0x246	UPNONCE6	UPNONCE<55:48>								0000 0000	84
0x247	UPNONCE7	UPNONCE<63:56>								0000 0000	84
0x248	UPNONCE8	UPNONCE<71:64>								0000 0000	85
0x249	UPNONCE9	UPNONCE<79:72>								0000 0000	85
0x24A	UPNONCE10	UPNONCE<87:80>								0000 0000	86
0x24B	UPNONCE11	UPNONCE<95:88>								0000 0000	86
0x24C	UPNONCE12	UPNONCE<103:96>								0000 0000	87

Legend: r = reserved

2.15.3 SHORT ADDRESS CONTROL REGISTERS DETAIL

REGISTER 2-1: RXMCR: RECEIVE MAC CONTROL REGISTER (ADDRESS: 0x00)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	NOACKRSP	r	PANCOORD	COORD	ERRPKT	PROMI
bit 7							bit 0

Legend:	r = reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Reserved:** Maintain as '0'

bit 5 **NOACKRSP:** Automatic Acknowledgement Response bit
- 1 = Disables automatic Acknowledgement response
- 0 = Enables automatic Acknowledgement response. Acknowledgements are returned when they are requested (default).

bit 4 **Reserved:** Maintain as '0'

bit 3 **PANCOORD:** PAN Coordinator bit
- 1 = Set device as PAN coordinator
- 0 = Device is not set as PAN coordinator (default)

bit 2 **COORD:** Coordinator bit
- 1 = Set device as coordinator
- 0 = Device is not set as coordinator (default)

bit 1 **ERRPKT:** Packet Error Mode bit
- 1 = Accept all packets including those with CRC error
- 0 = Accept only packets with good CRC (default)

bit 0 **PROMI:** Promiscuous Mode bit
- 1 = Receive all packet types with good CRC
- 0 = Discard packet when there is a MAC address mismatch, illegal frame type, dPAN/sPAN or MAC short address mismatch (default)

REGISTER 2-2: PANIDL: PAN ID LOW BYTE REGISTER (ADDRESS: 0x01)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAN ID Low Byte (PANIDL<7:0>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PANIDL<7:0>:** PAN ID Low Byte bits

REGISTER 2-3: PANIDH: PAN ID HIGH BYTE REGISTER (ADDRESS: 0x02)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAN ID High Byte (PANIDH<15:8>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PANIDH<15:8>:** PAN ID High Byte bits

REGISTER 2-4: SADRL: SHORT ADDRESS LOW BYTE REGISTER (ADDRESS: 0x03)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Short Address Low Byte (SADRL<7:0>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SADRL<7:0>:** Short Address Low Byte bits

REGISTER 2-5: SADRH: SHORT ADDRESS HIGH BYTE REGISTER (ADDRESS: 0x04)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Short Address High Byte (SADRH<15:8>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SADRH<15:8>:** Short Address High Byte bits

REGISTER 2-6: EADR0: EXTENDED ADDRESS 0 REGISTER (ADDRESS: 0x05)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR<7:0>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR<7:0>:** 64-Bit Extended Address bits

REGISTER 2-7: EADR1: EXTENDED ADDRESS 1 REGISTER (ADDRESS: 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR<15:8>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR<15:8>:** 64-Bit Extended Address bits

REGISTER 2-8: EADR2: EXTENDED ADDRESS 2 REGISTER (ADDRESS: 0x07)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
64-Bit Extended Address bits (EADR<23:16>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EADR<23:16>:** 64-Bit Extended Address bits