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# MRF24XA

# Low-Power, 2.4 GHz ISM-Band IEEE 802.15.4™ RF Transceiver with Extended Proprietary Features

## Features

- IEEE 802.15.4™-2003 and IEEE 802.15.4-2006 Standard Compliant RF transceiver
- Multiple air-data-rates:
  - 250 kbps (IEEE 802.15.4)
  - 125, 500, 1000, 2000 kbps, co-existence with standard networks
- Configurable TX output power: -19 to 1 dBm
- Frame header duration scales with the selected data rate
- On-the-fly, per frame air-data-rate detection (link-by-link independent air-data-rates)
- Inferred destination addressing (to further save on framing overheads; optional)

## Full-Featured MCU Support

- Hardware frame parser
- Hardware CSMA-CA controller, automatic Acknowledgment (ACK) and Frame Check Sequence (FCS)
- Supports all Clear Channel Assessment (CCA) modes
- Reports ED, RSSI, LQI, and CFO
- Channel Agility with acknowledgments
- Two independent 128 byte frame buffers
- Streaming mode to maximize throughput
- Automatic packet retransmit capability
- Hardware Security Engine (AES-128) and configurable Encryption/Decryption mode

## Low-Power

- Extreme minimization of radio ON time
  - Highest channel-admissible data rate used
  - 20%-70% overall reduction through framing
- 2 Mbps frames can reduce radio ON time by a factor of 4 to 8 with respect to 250 kbps frames
- 27.5 mA TX current (typical at 0 dBm)
- 13.5 mA RX current in RX Listen Power-Saving mode
- 15.5-16.5 mA RX current in RX Packet Demodulation mode (data rate and device Configuration dependent)
- Deep Sleep, Sleep, Crystal ON, and RX Listen Power-Saving modes
- Memory retention in Deep Sleep mode (<40 nA typical)
- Automated functions minimize MCU ON time

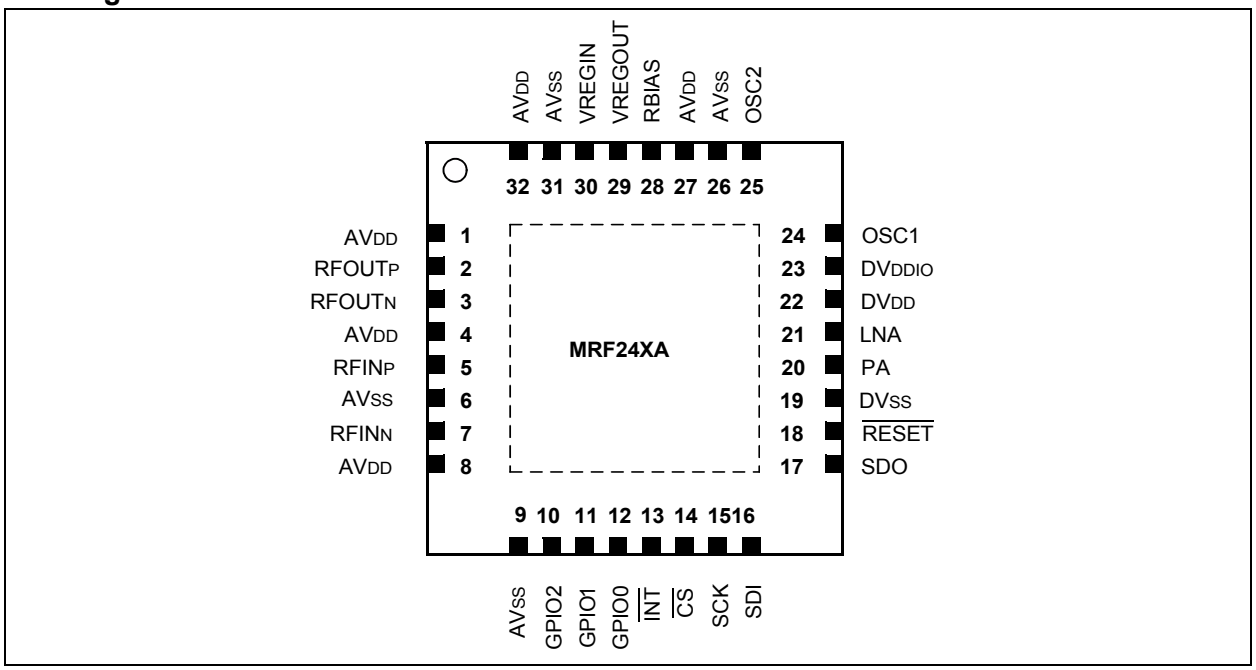
## General

- Low external component count
- Best-in-class battery life preservation
- Supply range: 1.5V to 3.6V
- Compact 32-pin 5x5 $mm^2$ QFN package
- Temperature range: -40°C to +85°C
- Certified turnkey-ready solutions available

## Applications

- IEEE 802.15.4/ZigBee® systems (RF4CE and MiWi™ network)
- Industrial monitoring and control
- IEEE 1588 precise timing protocol networks
- Automatic meter reading
- Home building automation
- Low-power wireless sensor networks
- Consumer electronics, voice and audio

**Pin Diagram**



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**NOTES:**

## 1.0 DEVICE OVERVIEW

MRF24XA is an IEEE 802.15.4™ Standard compliant 2.4 GHz RF transceiver with feature extensions. MRF24XA integrates the PHY and MAC functionality in a single-chip solution. MRF24XA implements a low-cost, low-power, high data rate (125 kbps to 2 Mbps) Wireless Personal Area Network (WPAN) device. All the data rates contains the same spectral shape requiring identical bandwidth. At 125 kbps data rate Direct Sequence Spread Spectrum (DSSS) is combined with error correction and coding for maximum range and robustness against interference. The 2 Mbps data rate is used to minimize radio ON time, therefore extending battery life. Figure 1-1 illustrates a simplified block diagram of a MRF24XA wireless node. MRF24XA interfaces to many popular Microchip PIC® microcontrollers through a 4-wire serial SPI interface, interrupt, GPIO, and $\overline{\text{RESET}}$ pins.

MRF24XA can also handle external Power Amplifier (PA) and Low Noise Amplifier (LNA).

MRF24XA provides hardware support for:

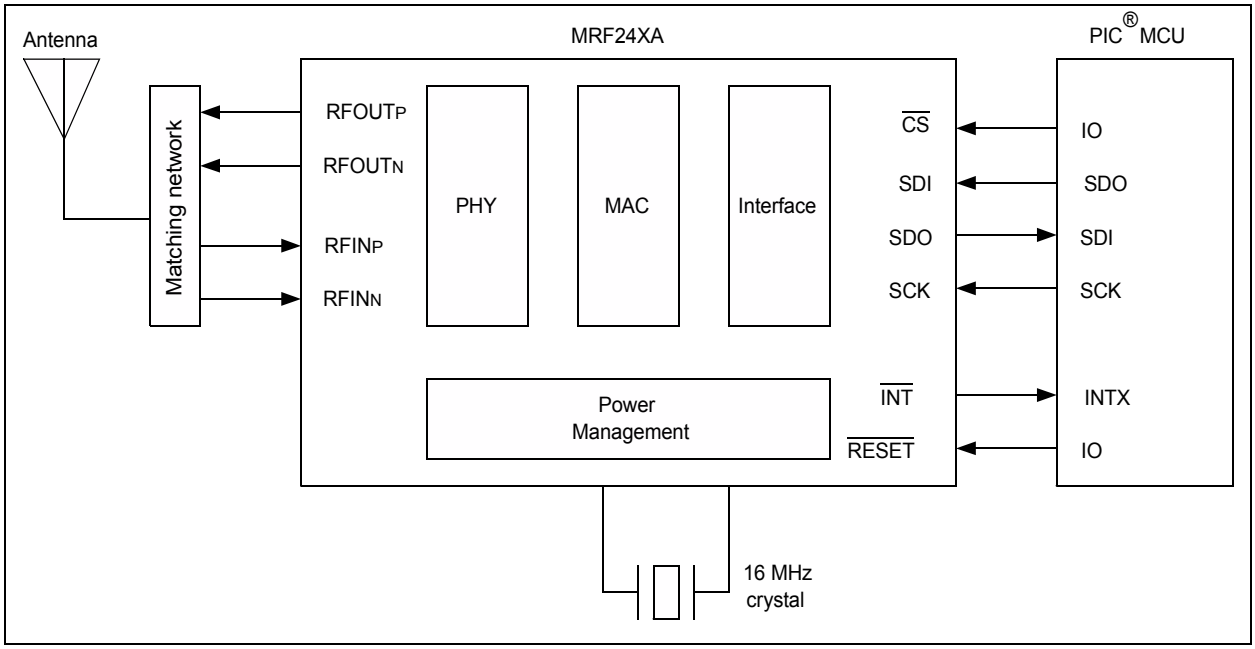
- Energy detection
- Carrier sense
- Four CCA modes
- CSMA-CA algorithm
- Automatic packet retransmission
- Automatic acknowledgement
- Independent transmit and receive buffers
- Security engine supports encryption and decryption for MAC sublayer and upper layer
- Inferred destination addressing
- Channel agility with ACKs
- Battery monitoring

These features reduce the processing load, allowing the use of low-cost 8-bit microcontrollers.

MRF24XA is compatible with Microchip's ZigBee®, MiWi™ and MiWi P2P software stacks. Each software stack is available as a free download, including source code, from the Microchip web site:

http://www.microchip.com/wireless.

**FIGURE 1-1: MRF24XA WIRELESS NODE BLOCK DIAGRAM**



**NOTES:**

# 2.0 HARDWARE DESCRIPTION

## 2.1 Overview

MRF24XA is an IEEE 802.15.4 Standard compliant 2.4 GHz RF transceiver with extended feature set for longer battery life, higher throughput and increased operating range.

MRF24XA integrates the PHY and MAC functionality in a single-chip solution. Figure 2-1 illustrates a block diagram of the MRF24XA circuitry.

An external 16 MHz crystal clocks the frequency synthesizer and generates a 2.4 GHz frequency RF carrier.

The receiver is a zero-IF architecture consisting of a Low-Noise Amplifier, down conversion mixers, channel filters and baseband amplifiers with a Received Signal Strength Indicator (RSSI).

The transmitter is a direct conversion architecture with a 1 dBm maximum output (typical) and 20 dB power control range.

The internal transmitter and receiver circuits contains separate RFP and RFN input/output pins that connects to impedance matching circuitry (balun) and antenna. An external Power Amplifier or Low Noise Amplifier, or both is controlled through the PA and LNA pins.

Three general purpose Input/Output (GPIO) pins are configurable for control or monitoring purposes.

The power management circuitry consists of an integrated Low Dropout (LDO) voltage regulator and a 5-bit resolution Battery Monitor Block. MRF24XA is placed into a low-current (<40 nA typical) Deep Sleep mode.

The Media Access Controller (MAC) circuitry can sequence the transmit, receive and automatically enable the security operations. The host MCU can control these mechanisms through register configurations and Frame Control (FCtrl) field embedded in the downloaded formatted frames. Three alternative frame formats are supported: IEEE 802.15.4 2003, 2006 compliant MAC frame formats and a flexible and power-efficient advanced MAC frame format, which is proprietary. Before launching transmission, the host must load the buffer with a formatted frame. The hardware can optionally perform encryption and message integrity code appending as configured, then sends the frame appending a Frame Check Sequence (FCS).

Hardware can autonomously sequence acknowledge reception and automatic retransmissions.

In reception, the format of the demodulated frame is verified. Depending on the Configuration, duplicate frames, frames with corrupted FCS or address mismatch are discarded. On reception of valid frames, automatic acknowledge sending, decryption and message integrity checking are supported.

As the default, separate buffers are reserved for transmission and reception. Alternatively, either the Transmit Streaming (TX-Streaming) or the Receive Streaming (RX-Streaming) modes are selected whereby buffers are used by alternating between the two for servicing a single direction of data flow. The AES-128 engine are governed to perform network-layer security processing and supports complete security suites such as CTR, CBC-MAC and CCM*.

Transceiver is controlled through a 4-wire SPI, interrupt and $\overline{\text{RESET}}$ pins.

## 2.2 Operating Modes

Table 2-1 summarizes the Operating modes of MRF24XA.

**TABLE 2-1: MRF24XA POWER MODES**

| Operating Mode | Internal Functional Blocks | | | | | |
|---|---|---|---|---|---|---|
| | 1.2V LDO | Crystal Oscillator | Synthesizer | RX Front End | RX Baseband | TX Chain |
| Deep Sleep | OFF | OFF | OFF | OFF | OFF | OFF |
| Sleep | ON | OFF | OFF | OFF | OFF | OFF |
| RFOFF Crystal ON | ON | ON | OFF | OFF | OFF | OFF |
| RFOFF Synthesizer ON | ON | ON | ON | OFF | OFF | OFF |
| RX Listen Power-Save | ON | ON | ON | ON | OFF | OFF |
| RX Listen | ON | ON | ON | ON | ON | OFF |
| TX | ON | ON | ON | OFF | OFF | ON |

## 2.3 Block Diagram

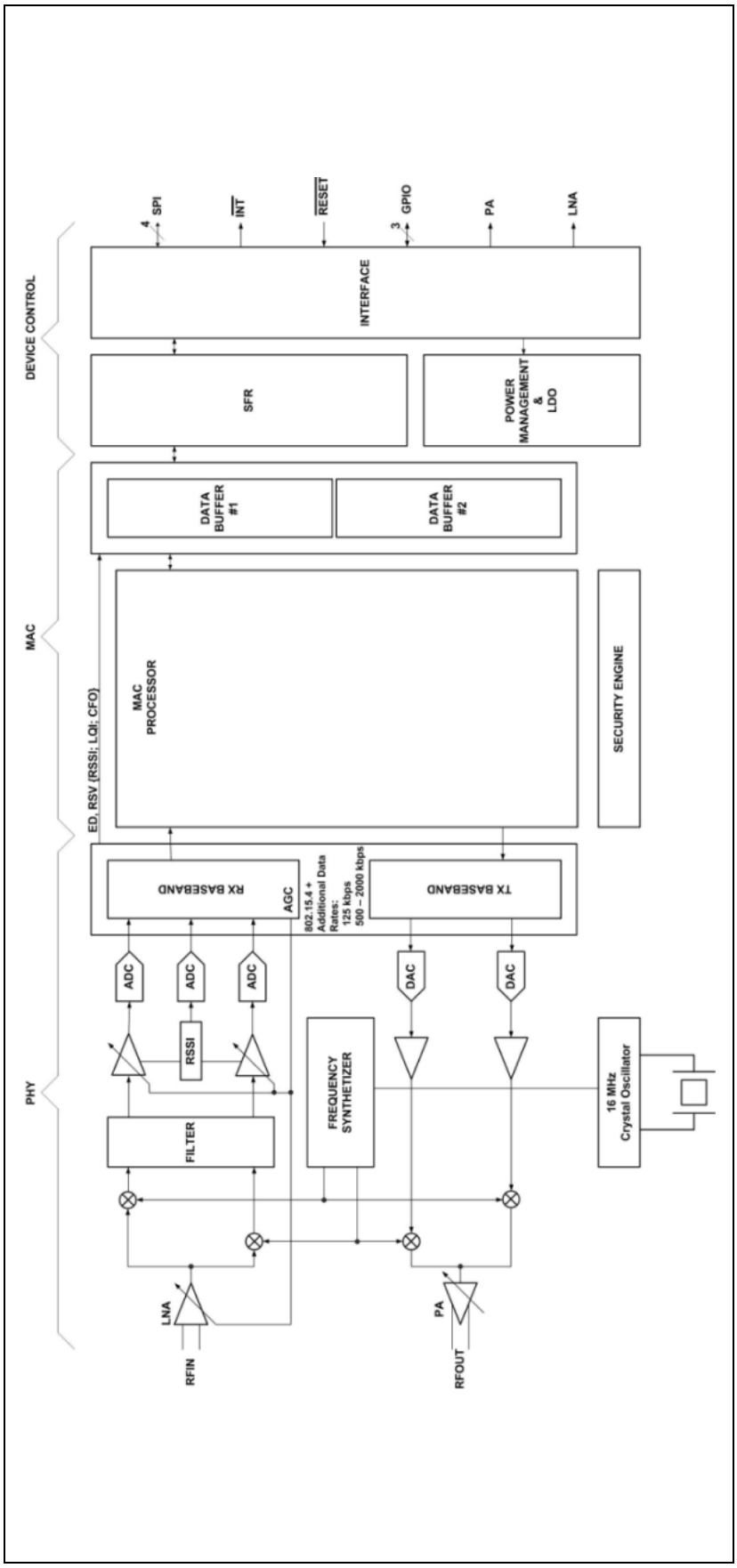



**FIGURE 2-1: MRF24XA ARCHITECTURE BLOCK DIAGRAM**

## 2.4 Pin Descriptions

**TABLE 2-2: MRF24XA PIN DESCRIPTIONS**

| Pin | Symbol | Type | Description |
|---|---|---|---|
| 1 | AVDD | Power | 1.2V supply, normally connected to VREGOUT (pin 29) |
| 2 | RFOUTP | AO | Differential RF Output (+) |
| 3 | RFOUTN | AO | Differential RF Output (–) |
| 4 | AVDD | Power | 1.2V supply, normally connected to VREGOUT (pin 29)(1) |
| 5 | RFINP | AI | Differential RF Input (+) |
| 6 | AVSS | Ground | Ground |
| 7 | RFINN | AI | Differential RF Input (–) |
| 8 | AVDD | Power | 1.2V supply, normally connected to VREGOUT (pin 29) |
| 9 | AVSS | Power | Ground(1) |
| 10 | GPIO2 | DIO | GPIO2 |
| 11 | GPIO1 | DIO | GPIO1 |
| 12 | GPIO0 | DIO | GPIO0 |
| 13 | $\overline{INT}$ | DO | Interrupt Output, active-low |
| 14 | $\overline{CS}$ | DI | SPI Chip Select Pin, active-low |
| 15 | SCK | DI | SPI serial clock |
| 16 | SDI | DI | SPI serial data Input |
| 17 | SDO | DO | SPI serial data Output |
| 18 | $\overline{RESET}$ | DI | Reset Input, active-low |
| 19 | DVSS | Ground | Digital ground |
| 20 | PA | DO | External PA enable Output |
| 21 | LNA | DO | External LNA enable Output |
| 22 | DVDD | Power | Digital 1.2V supply, normally connected to VREGOUT (pin 29) |
| 23 | DVDDIO | Power | Digital 1.5V–3.6V supply for the IO blocks, normally connected to VREGIN (pin 30) |
| 24 | OSC1 | AI | Crystal oscillator Pin 1, External Clock Input |
| 25 | OSC2 | AO | Crystal oscillator Pin 2 |
| 26 | AVSS | Ground | Ground |
| 27 | AVDD | Power | 1.2V supply, normally connected to VREGOUT (pin 29) |
| 28 | RBIAS | AO | External resistor reference pin |
| 29 | VREGOUT | Power | 1.2V regulated Output |
| 30 | VREGIN | Power | 1.5V–3.6V regulator Input |
| 31 | AVSS | Ground | Ground |
| 32 | AVDD | Power | 1.2V supply, normally connected to VREGOUT (pin 29) |

**Legend:** A = Analog, D = Digital, I = Input, O = Output

**Note 1:** In case PCB runs out of space, disconnect these pins.

### 2.4.1 POWER AND GROUND PINS

Table 2-3 lists the recommended bypass capacitors. VDD pins 29 and 30 are power pins, which require different bypass capacitors to ensure sufficient bypass decoupling and stability. Bypass capacitors must have low serial resistance. The 4.7 µF capacitors must be made of ceramic or high-performance tantalum.

On PCB layout minimize trace length from the VDD pin to the bypass capacitors and connect capacitors to the pads as short as possible. PCB tracks must be wide enough to minimize voltage drop and serial inductance of the power line.

Analog and digital power lines must follow a star topology, where the common point is the bypass capacitor on pin 30.

**TABLE 2-3: RECOMMENDED BYPASS CAPACITOR VALUES**

| VDD Pin | Symbol | Bypass Capacitor |
|---|---|---|
| 1 | AVDD | 3.3 pF |
| 29 | VREGOUT | 4.7 µF |
| 30 | VREGIN | 10 nF + 4.7 µF |

### 2.4.2 16 MHz MAIN OSCILLATOR PINS

The 16 MHz oscillator is connected to OSC1 and OSC2 pins as shown in Figure 2-2, which provides the reference frequency for the internal RF, MAC and BB circuitry. Table 2-4 lists the crystal parameters.

To minimize parasitic effects on pins, the crystal must be put as close as possible to MRF24XA. It keeps the tracks short. Crystal must be surrounded with ground pour to minimize cross coupling effects. Crystal load capacitors must be placed close to the crystal.

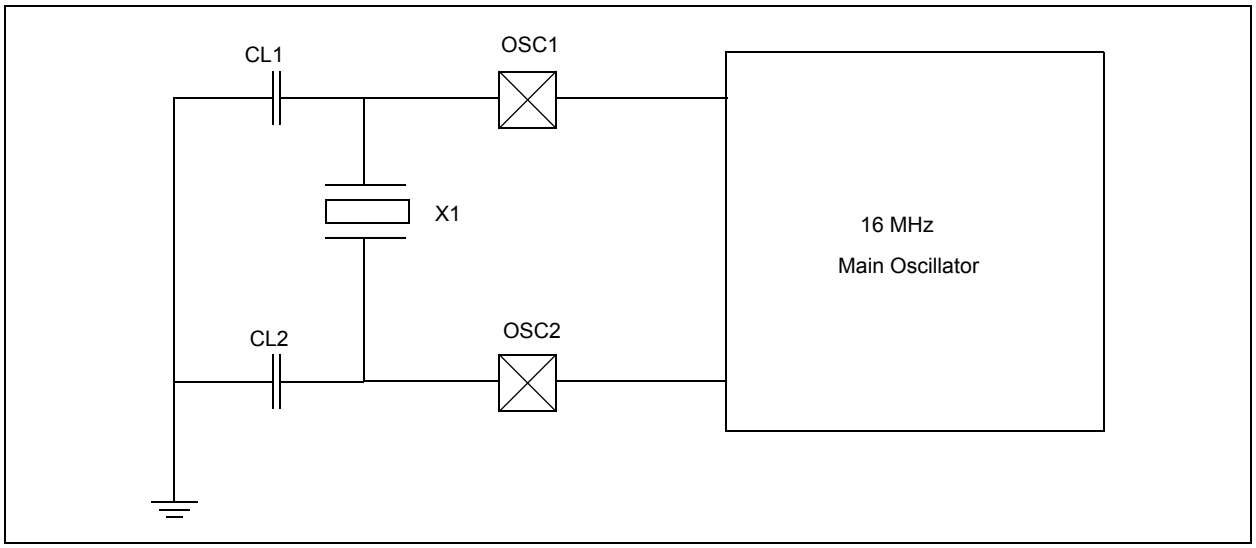
**TABLE 2-4: 16 MHz CRYSTAL PARAMETERS(1)**

| Parameters | Value |
|---|---|
| Frequency | 16 MHz |
| Frequency tolerance for 500, 250 and 125 kbps data rates (including manufacturing aging and temperature) | ±60 ppm(1) |
| Frequency tolerance for 2 and 1 Mbps data rates (including manufacturing aging and temperature) | ±40 ppm(2) |
| Mode | Fundamental |
| Load Capacitance | 18 pF |
| ESR | 80 Ohm max |

**Note 1:** IEEE 802.15.4 defines ±40 ppm.

**2:** These values are only used for design guidance .

**FIGURE 2-2: 16 MHz MAIN OSCILLATOR CRYSTAL CIRCUIT**



### 2.4.3 RESET ($\overline{\text{RESET}}$) PIN

An external Hardware Reset is performed by asserting the $\overline{\text{RESET}}$ pin 18 low. If the RESET pin is deasserted, MRF24XA starts the internal Calibration process. RDYIF interrupt is set when the device is ready to use. The $\overline{\text{RESET}}$ pin contains an internal weak pull-up resistor.

### 2.4.4 INTERRUPT ($\overline{\text{INT}}$) PIN

The Interrupt ($\overline{\text{INT}}$) pin 13 provides an interrupt signal to the host MCU from MRF24XA where the signal is active-low polarity. Interrupt sources must be enabled and unmasked before the $\overline{\text{INT}}$ pin becomes active.

Refer to **Section 3.2 "Interrupts"** for the functional description of interrupts.

### 2.4.5 GENERAL PURPOSE INPUT/ OUTPUT (GPIO) PINS

Three GPIO pins are configured individually for control or monitoring purposes. The TRISGPIOx bits in the GPIO register (0x0D) configures the input or output selection. GPIO data is read or written through the GPIO bits of GPIO register. The GPIO interrupt polarity is selected through GPIOxP bits in the STGPIO (0x0E) register.

GPIO lines in Input mode are used in Schmitt Trigger Input mode. STENGPIOx bits of STGPIO register enables Schmitt Triggers. GPIOs are also used to monitor the internal blocks. The GPIOMODE bits <3:0> of the PINCON (0x0C) register selects these monitoring functions.

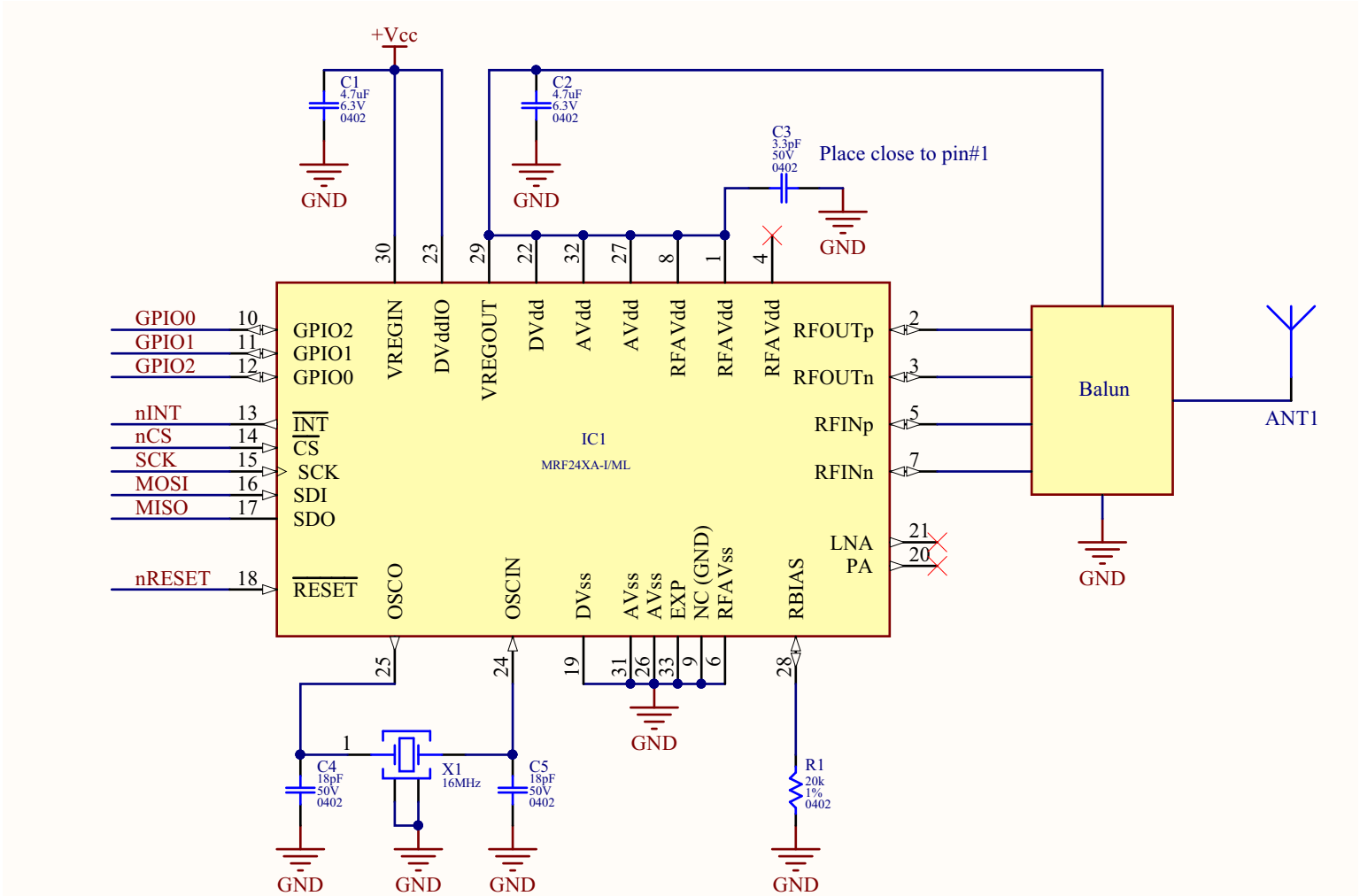
### 2.4.6 SERIAL PERIPHERAL INTERFACE (SPI) PORT PINS

MRF24XA communicates with a host MCU through a 4-wire SPI port as a slave device. MRF24XA supports SPI mode 0,0, which requires that SCK idles in a low state. The $\overline{\text{CS}}$ pin must be held low while communicating with MRF24XA. Figure 2-3 illustrates timing for a read and a write operation. MRF24XA receives the data through the SDI pin and clocks in on the rising edge of SCK. MRF24XA sends data through the SDO pin and clocks out on the falling edge of SCK. The SDO lines preserve its HiZ state in Deep Sleep mode.

## 2.5 Application Example

Figure 2-3 illustrates the schematic of a recommended application circuit for MRF24XA.

**FIGURE 2-3: MRF24XA APPLICATION CIRCUIT**



## 2.6 Memory Organization

Table 2-5 shows that memory is functionally divided into Special Function Registers (SFR) and data buffers.

The SFRs provide control, status and device Configuration addressing for MRF24XA operations. Data buffers serve as temporary buffers for data transmission and reception. Memory is accessed through two addressing methods: Short (1 byte) and Long (2 bytes).

### 2.6.1 ADDRESS OVERVIEW

MRF24XA contains two Addressing modes:

- Short Address Mode: Requires one byte for address, and may be used to access the first 64 on-chip control registers.
- Long Address Mode: Requires two bytes for address, and may be used to access all on-chip registers and data buffers. Figure 2-4 illustrates these modes.

**TABLE 2-5: MRF24XA MEMORY MAP**

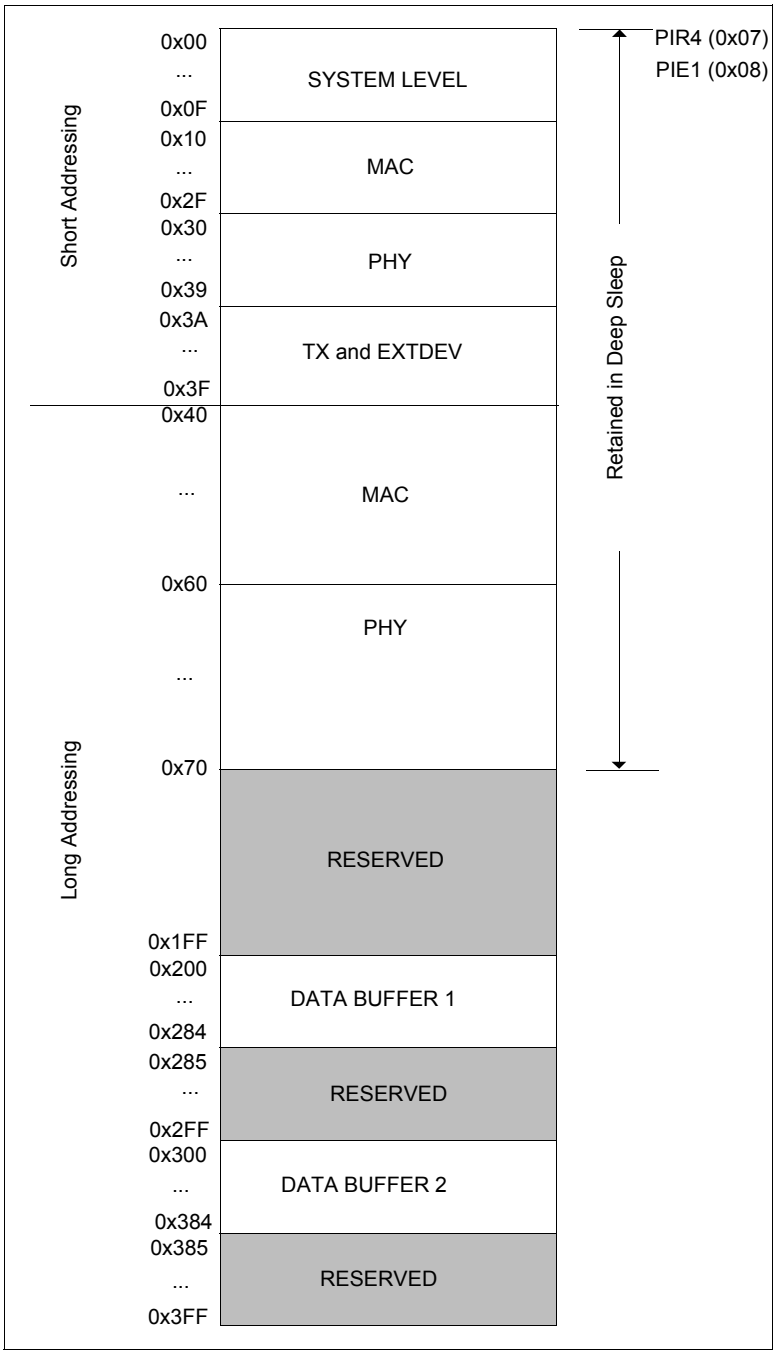


**TABLE 2-6: SHORT ADDRESS REGISTER SUMMARY FOR MRF24XA**

| Architecture | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SYSTEM LEVEL | 0x00 | REGRST | r | r | REGRST<5:0> | | | | | | 71 |
| | 0x01 | FSMRST | r | r | r | FSMRST<4:0> | | | | | 71 |
| | 0x02 | OPSTATUS | r | MACOP<3:0> | | | | RFOP<2:0> | | | 18 |
| | 0x03 | STATUS | INITDONESF | XTALSF | REGSF | CALST | XTALDIS | DSLEEP | IDLESF | POR | 19 |
| | 0x04 | PIR1 | VREGIF | r | RDYIF | IDLEIF | r | CALSOIF | CALHAIF | r | 20 |
| | 0x05 | PIR2 | TXIF | TXENCIF | TXMAIF | TXACKIF | TXCSMAIF | TXSZIF | TXOVFIF | FRMIF | 21 |
| | 0x06 | PIR3 | RXIF | RXDECIF | RXTAGIF | r | RXIDENTIF | RXFLTIF | RXOVFIF | STRMIF | 22 |
| | 0x07 | PIR4 | TXSFDIF | RXSFDIF | ERRORIF | WARNIF | EDCCAIF | GPIO2IF | GPIO1IF | GPIO0IF | 23 |
| | 0x08 | PIE1 | r | r | RDYIE | IDLEIE | r | CALSOIE | CALHAIE | r | 24 |
| | 0x09 | PIE2 | TXIE | TXENCIE | TXMAIE | TXACKIE | TXCSMAIE | TXSZIE | TXOVFIE | FRMIE | 25 |
| | 0x0A | PIE3 | RXIE | RXDECIE | RXTAGIE | r | RXIDENTIE | RXFLTIE | RXOVFIE | STRMIE | 26 |
| | 0x0B | PIE4 | TXSFDIE | RXSFDIE | ERRORIE | WARNIE | EDCCAIE | GPIO2IE | GPIO1IE | GPIO0IE | 27 |
| | 0x0C | PINCON | r | GIE | r | IRQIF | GPIOMODE<3:0> | | | | 28 |
| | 0x0D | GPIO | GPIOEN | TRISGPIO2 | TRISGPIO1 | TRISGPIO0 | r | GPIO2 | GPIO1 | GPIO0 | 29 |
| | 0x0E | STGPIO | r | GPIO2P | GPIO1P | GPIO0P | r | STENGPIO2 | STENGPIO1 | STENGPIO0 | 30 |
| | 0x0F | PULLGPIO | r | PULLDIRGPIO2 | PULLDIRGPIO1 | PULLDIRGPIO0 | r | PULLENGPIO2 | PULLENGPIO1 | PULLENGPIO0 | 31 |
| MAC | 0x10 | MACCON1 | TRXMODE<1:0> | | ADDRSZ<2:0> | | | CRCSZ | FRMFMT | SECFLAGOVR | 32 |
| | 0x11 | MACCON2 | CHANNEL<3:0> | | | | SECSUITE<3:0> | | | | 34 |
| | 0x12 | TXCON | TXST | DTSM | TXENC | TXBUFEMPTY | CSMAEN | DR<2:0> | | | 35 |
| | 0x13 | RXACKWAIT | RXACKWAIT<7:0> | | | | | | | | 37 |
| | 0x14 | RETXCOUNT | RETXMCNT<3:0> | | | | RETXCCNT<3:0> | | | | 37 |
| | 0x15 | RXCON1 | RXEN | NOPA | RXDEC | RXVLQIEN | RSVRSSIEN | RSVCHDREN | RSVCFOEN | r | 38 |
| | 0x16 | RXCON2 | RXBUFFUL | IDENTREJ | ACKRXFP | ACKTXFP | AUTORPTEN | AUTOACKEN | ADPTCHEN | ADPTDREN | 39 |
| | 0x17 | TXACKTO | TXACKTO<7:0> | | | | | | | | 41 |
| | 0x18 | RXFILTER | PANCRDN | CRCREJ | CMDREJ | DATAREJ | UNIREJ | NOTMEREJ | BCREJ | NSTDREJ | 42 |
| | 0x19 | TMRCON | BOMCNT<2:0> | | | BASETM<4:0> | | | | | 44 |
| | 0x1A | CSMABE | MAXBE<3:0> | | | | MINBE<3:0> | | | | 45 |
| | 0x1B | BOUNIT | BOUNIT<7:0> | | | | | | | | 46 |
| | 0x1C | STRMTOL | STRMTO<7:0> | | | | | | | | 46 |
| | 0x1D | STRMTOH | STRMTO<15:8> | | | | | | | | 46 |
| | 0x1E | OFFTM | OFFTM<7:0> | | | | | | | | 47 |

**Legend:** r = Reserved, read as '0'.

**TABLE 2-6: SHORT ADDRESS REGISTER SUMMARY FOR MRF24XA (CONTINUED)**

| Architecture | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0x1F | ADDR1 | ADDR<7:0> | | | | | | | | 48 |
| | 0x20 | ADDR2 | ADDR<15:8> | | | | | | | | 48 |
| | 0x21 | ADDR3 | ADDR<23:16> | | | | | | | | 48 |
| | 0x22 | ADDR4 | ADDR<31:24> | | | | | | | | 48 |
| | 0x23 | ADDR5 | ADDR<39:32> | | | | | | | | 48 |
| | 0x24 | ADDR6 | ADDR<47:40> | | | | | | | | 48 |
| | 0x25 | ADDR7 | ADDR<55:48> | | | | | | | | 48 |
| | 0x26 | ADDR8 | ADDR<63:56> | | | | | | | | 48 |
| | 0x27 | SHADDRL | SHADDR<7:0> | | | | | | | | 49 |
| | 0x28 | SHADDRH | SHADDR<15:8> | | | | | | | | 49 |
| | 0x29 | PANIDL | PANID<7:0> | | | | | | | | 49 |
| | 0x2A | PANIDH | PANID<15:8> | | | | | | | | 49 |
| | 0x2B | SECHDRINDX | r | SECHDRINDX<6:0> | | | | | | | 50 |
| | 0x2C | SECPAYINDX | r | SECPAYINDX<6:0> | | | | | | | 50 |
| | 0x2D | SECENDINDX | r | SECENDINDX<6:0> | | | | | | | 51 |
| | 0x2E | MACDEBUG | BUF1TXPP | BUF2TXPP | BUF1RXPP | BUF2RXPP | TXRDBUF | RXWRBUF | BUSRDBUF | BUSWRBUF | 52 |
| PHY | 0x2F | CCACON1 | CCABUSY | CCAST | RSSITHR<5:0> | | | | | | 53 |
| | 0x30 | CCACON2 | CSTHR<3:0> | | | | CCALEN<1:0> | | CCAMODE<1:0> | | 53 |
| | 0x31 | EDCON | r | r | EDMODE | EDST | EDLEN<3:0> | | | | 54 |
| | 0x32 | EDMEAN | EDMEAN<7:0> | | | | | | | | 54 |
| | 0x33 | EDPEAK | EDPEAK<7:0> | | | | | | | | 55 |
| | 0x34 | CFOCON | CFOTX<3:0> | | | | CFORX<3:0> | | | | 55 |
| | 0x35 | CFOMEAS | CFOMEAS<7:0> | | | | | | | | 56 |
| | 0x36 | RATECON | DIS2000 | DIS1000 | DIS500 | DIS250 | DISSTD | DIS125 | OPTIMAL | PSAV | 57 |
| | 0x37 | POWSAVE | DESENSTHR<3:0> | | | | PSAVTHR<3:0> | | | | 58 |
| | 0x38 | BBCON | RNDMOD | AFCOVR | RXGAIN<1:0> | | PRMBHOLD | PRMBSZ<2:0> | | | 59 |
| | 0x39 | IFGAP | r | r | r | IFGAP<4:0> | | | | | 60 |
| TX AND EXTDEV | 0x3A | TXPOW | CHIPBOOST<2:0> | | | TXPOW<4:0> | | | | | 60 |
| | 0x3B | TX2IDLE | r | r | r | TX2IDLE<4:0> | | | | | 61 |
| | 0x3C | TX2TXMA | r | r | r | TX2TXMA<4:0> | | | | | 61 |
| | 0x3D | EXTPA | r | EXTPA_P | PAEN | PA2TXMA<4:0> | | | | | 62 |
| | 0x3E | EXTLNA | r | EXTLNA_P | LNAEN | LNADLY<4:0> | | | | | 62 |
| | 0x3F | BATMON | r | r | BATMONPD | BATMON<4:0> | | | | | 63 |

**Legend:** r = Reserved, read as '0'.

**TABLE 2-7: LONG ADDRESS REGISTER SUMMARY FOR MRF24XA**

| | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MAC | 0x40 | SECKEY1 | SECKEY<7:0> | | | | | | | | 63 |
| | 0x41 | SECKEY2 | SECKEY<15:8> | | | | | | | | 63 |
| | 0x42 | SECKEY3 | SECKEY<23:16> | | | | | | | | 63 |
| | 0x43 | SECKEY4 | SECKEY<31:24> | | | | | | | | 63 |
| | 0x44 | SECKEY5 | SECKEY<39:32> | | | | | | | | 63 |
| | 0x45 | SECKEY6 | SECKEY<47:40> | | | | | | | | 63 |
| | 0x46 | SECKEY7 | SECKEY<55:48> | | | | | | | | 63 |
| | 0x47 | SECKEY8 | SECKEY<63:56> | | | | | | | | 63 |
| | 0x48 | SECKEY9 | SECKEY<71:64> | | | | | | | | 63 |
| | 0x49 | SECKEY10 | SECKEY<79:72> | | | | | | | | 63 |
| | 0x4A | SECKEY11 | SECKEY<87:80> | | | | | | | | 63 |
| | 0x4B | SECKEY12 | SECKEY<95:88> | | | | | | | | 63 |
| | 0x4C | SECKEY13 | SECKEY<103:96> | | | | | | | | 63 |
| | 0x4D | SECKEY14 | SECKEY111:104> | | | | | | | | 63 |
| | 0x4E | SECKEY15 | SECKEY<119:112> | | | | | | | | 63 |
| | 0x4F | SECKEY16 | SECKEY<127:120> | | | | | | | | 63 |
| | 0x50 | SECNONCE1 | SECNONCE<7:0> | | | | | | | | 65 |
| | 0x51 | SECNONCE2 | SECNONCE<15:8> | | | | | | | | 65 |
| | 0x52 | SECNONCE3 | SECNONCE<23:16> | | | | | | | | 65 |
| | 0x53 | SECNONCE4 | SECNONCE<31:24> | | | | | | | | 65 |
| | 0x54 | SECNONCE5 | SECNONCE<39:32> | | | | | | | | 65 |
| | 0x55 | SECNONCE6 | SECNONCE<47:40> | | | | | | | | 65 |
| | 0x56 | SECNONCE7 | SECNONCE<55:48> | | | | | | | | 65 |
| | 0x57 | SECNONCE8 | SECNONCE<63:56> | | | | | | | | 65 |
| | 0x58 | SECNONCE9 | SECNONCE<71:64> | | | | | | | | 65 |
| | 0x59 | SECNONCE10 | SECNONCE<79:72> | | | | | | | | 65 |
| | 0x5A | SECNONCE11 | SECNONCE<87:80> | | | | | | | | 65 |
| | 0x5B | SECNONCE12 | SECNONCE<95:88> | | | | | | | | 65 |
| | 0x5C | SECNONCE13 | SECNONCE<103:96> | | | | | | | | 65 |
| | 0x5D | SECENCFLAG | SECENCFLAG<7:0> | | | | | | | | |
| | 0x5E | SECAUTHFLAG | SECAUTHFLAG<7:0> | | | | | | | | |
| | 0x5F | r | | | | | | | | | |
| PHY | 0x60 | SFD1 | SFD1<7:0> | | | | | | | | 66 |
| | 0x61 | SFD2 | SFD2<7:0> | | | | | | | | 67 |
| | 0x62 | SFD3 | SFD3<7:0> | | | | | | | | 67 |
| | 0x63 | SFD4 | SFD4<7:0> | | | | | | | | 68 |
| | 0x64 | SFD5 | SFD5<7:0> | | | | | | | | 68 |
| | 0x65 | SFD6 | SFD6<7:0> | | | | | | | | 69 |
| | 0x66 | SFD7 | SFD7<7:0> | | | | | | | | 69 |
| | 0x67 | r | | | | | | | | | |
| | 0x68 | r | | | | | | | | | |
| | 0x69 | r | | | | | | | | | |
| | 0x6A | r | | | | | | | | | |
| | 0x6B | r | | | | | | | | | |
| | 0x6C | r | | | | | | | | | |
| | 0x6D | r | | | | | | | | | |
| | 0x6E | SFDTO | SFDTIMEOUT<7:0> | | | | | | | | |
| | 0x7F | r | | | | | | | | | |

### 2.6.2 ADDRESS

When using a Short Addressing mode, the Address field is 6 bits wide to reduce framing overhead while accessing the mostly active registers (0x00..0x3F). In Long Addressing mode, the Address field is 10 bits wide (0x00..0x3FF) thus all the address is available for SPI operation.

### 2.6.3 AUTOMATIC TX START FEATURE

When a write to TRXBUF is done using Long Addressing mode and the 3rd bit of Byte 2 is set, the TXST bit automatically sets after the $\overline{CS}$ pin is released, and then MRF24XA sends the packet.

### 2.6.4 AUTOMATIC BUFFER FLUSH FEATURE

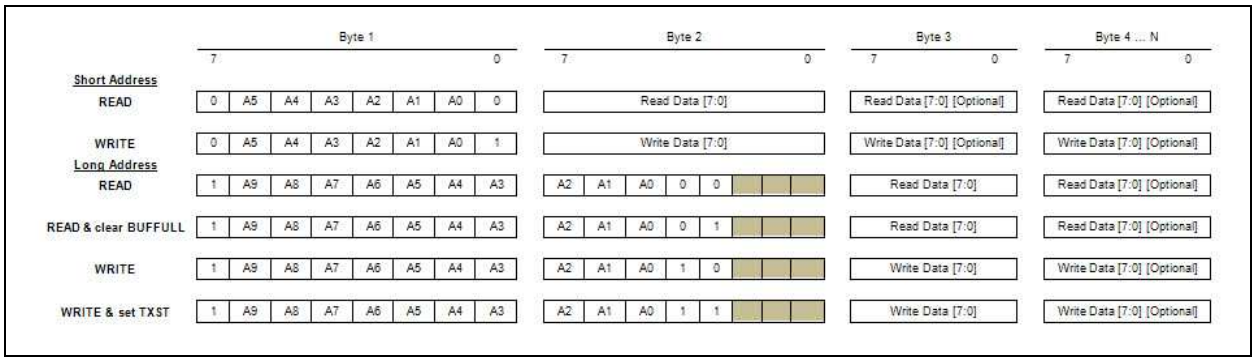
When a read from TRXBUF is done using Long Addressing mode and the 3rd bit of Byte 2 is set, the BUFFULL bit automatically becomes cleared after the $\overline{CS}$ pin is negated.

### 2.6.5 ADDRESS AUTO-INCREMENT FEATURE

After the starting address is loaded, the first byte of data is read from or written to this address. The second byte (assuming the $\overline{CS}$ pin is not negated between bytes) is read from or written to the starting address plus one, and so on.

If the memory map end is reached, the effective address rolls over to the beginning of the memory map. It is the sole responsibility of the software to handle this situation correctly. Figure 2-4 illustrates the available Address modes.

**FIGURE 2-4: SPI FRAMING TYPES**



## 2.7 Register Details

**REGISTER 2-1: OPSTATUS (OPERATION STATUS)[3]** **Address: 0x02**

| R-0 | R/HS/HC-0 | R/HS/HC-0 | R/HS/HC-0 | R/HS/HC-0 | R/HS/HC-0 | R/HS/HC-0 | R/HS/HC-0 |
|---|---|---|---|---|---|---|---|
| r | MACOP<3:0> | | | | RFOP<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|---|
| -n = Value at POR | | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| r = Reserved | | HC = Hardware Clear | HS = Hardware Set | |

bit 7 **Reserved:** Maintain as '0'

bit 6-3 **MACOP<3:0>:** MAC Operation Register bits[1, 2]

Provides status information on the current MAC state machine state. Encoding on MACOP<3:1>:
111 = Transmitting Acknowledge (TXACK)
110 = Receiving a packet (RXBUSY)
101 = Receiver listening to the channel waiting for packet (RX)
100 = Receiving (or waiting for) Acknowledge (RXACK)
011 = Transmitting a packet (TX)
010 = Performing Clear Channel Assessment (CCA)
001 = Back-off before repeated CCA (BO)
000 = MAC does not perform any o ation (IDLE)

bit 2-0 **RFOP<2:0>:** Radio Operation Register bits

Provides status information on the current radio state. Encoding on RFOP<2:0>:
111 = TX with external PA is turned on (TX+PA)
110 = RX with external LNA is turned on (RX+LNA)
101 = Synthesizer and external PA or LNA is turned on (SYNTH+PA/LNA)
100 = Radio calibrates if the host MCU sets the CALST, otherwise, device malfunction occurs (CAL/MAL)
011 = Analog transmit chain is activated (TX)
010 = Analog receiver chain is active (RX). Digital may be partially shut off
001 = Synthesizer is steady or ramping up or channel change is issued (SYNTH)
000 = Only the crystal oscillator is ON (OFF), (except when XTALSF = 1)

**Note 1:** GPIO<2:0> is dedicated to output MACOP<3:1> or RFOP<2:0>. Refer to the PINCON register, which specifies the pin Configuration.

**2:** MACOP<0> is connected to the RXBUFFUL register bit. It cannot be output over GPIO's.

**3:** The OPSTATUS register is sent on the SDO pin during the first byte of the SPI operation.

**REGISTER 2-2: STATUS (DEVICE STATUS)** **Address: 0x03**

| R/HS | R/HS | R/HS | R/W/HC-0 | R/W-0 | R/W-0 | R/HS | R/W/HC |
|---|---|---|---|---|---|---|---|
| INITDONESF | XTALSF | REGSF | CALST | XTALDIS | DSLEEP | IDLESF | POR |
| bit 7 | | | | | | | bit 0 |

| **Legend:** R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| r = Reserved | HC = Hardware Clear | HS = Hardware Set | |

bit 7 **INITDONESF:** Device Initialization Status Flag bit

Indicates that the ready state is reached since the LDO is on, (If VREGIF = 1). INITDONESF is asserted when RDYIF is set for the first time after VREGIF. This bit is only cleared on reset (POR, DEVFRST and PINRST).

bit 6 **XTALSF:** Crystal Status Flag bit

XTALSF = 1, indicates that 16 MHz system clock (from the crystal oscillator) is active. This bit is cleared either when XTALDIS is set or reset (POR, DEVFRST, PINRST).

XTALSF = 0, indicates that the crystal oscillator is either powered off (XTALDIS = 1) or is ramping up or is not stabilized yet, and the system clock is inactive.

bit 5 **REGSF:** Configuration Registers Status Flag bit

REGSF = 1 indicates that all the 1.2V register content is valid. Either it holds the default value after reset and the retention memory does not hold any data to restore, or the register configurations are restored from the retention memory.

REGSF = 0 indicates that registers from 0x08-0x6E are invalid. This occurs when the wake-up procedure from Deep Sleep mode did not complete the register restore operation yet. This bit is only cleared on Reset (POR, DEVFRST, and PINRST).

bit 4 **CALST:** Calibration Start bit

MCU sets this bit to start Calibration procedure after a CALSOIF or CALHAIF interrupt occurred. MCU may *not* clear it to abort Calibration. The device clears CALST when the Calibration is completed (CALHAIF = 0 indicates success, CALHAIF = 1 indicates failure). Issuing CALST operation without CALHAIF/CALSOIF terminates without any effect on the device.

bit 3 **XTALDIS:** Crystal Disable bit

MCU sets this bit to send the device into XTAL OFF state (reachable from ready state). XTALSF automatically gets cleared. The SPI register access is performed when crystal is not working.

bit 2 **DSLEEP:** Deep-Sleep bit

MCU sets this bit to send the device into Deep Sleep state. Following DSLEEP = 1 , the SPI access to the SFR is shut off, and the SPI pins must be quite, unless the host MCU wants to wake-up the device. When DSLEEP is set, the device transitions through register backup (taking cca. 16 ìs) before LDO is powered off.

bit 1 **IDLESF:** Idle Status Flag bit

Indicates Idle state of the device when all of the following bits are deasserted:

- TXBUFEMPTY = 0 since it is transmitted (TXST)
- Network layer security finished (TXENC)
- Crypto engine finished (RXDEC)
- Energy detect operation finished (EDST)
- Clear Channel Assessment finished (CCAST)

bit 0 **POR:** Power-on-Reset Flag bit

The 3.3V POR flag status. The device sets this only on 3.3V power-up (e.g., when battery is changed). Cleared by host MCU to be able to sense a Brown-out Reset (BOR). Settable for software testing.

**REGISTER 2-3: PIR1 (PERIPHERAL INTERRUPT REGISTER 1)** **Address: 0x04**

| R/HS-1 | R-0 | R/HS-0 | R/W/HC-0 | R-0 | R/W/HS-0 | R/W/HS-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VREGIF | r | RDYIF | IDLEIF | r | CALSOIF | CALHAIF | r |
| bit 7 | | | | | | | bit 0 |

| **Legend:** R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| r = Reserved | HC = Hardware Clear | HS = Hardware Set | |

bit 7 **VREGIF:** Voltage Regulator On Interrupt Flag bit

This is a nonpersistent bit. The register bit initializes to one on 1.2V reset except for PINRESET and only clears when reading PIR1. Note that the corresponding IE bit is not implemented(1).

bit 6 **Reserved:** Maintain as '0'

bit 5 **RDYIF:** Ready State Interrupt Flag bit

Set each time when ready state is reached:

- when Calibration ended (CALST = 0)
- when initialization ended (INITDONESF = 1)
- when crystal is ramped up (XTALSF = 1)

This bit is cleared when PIR1 is read.

bit 4 **IDLEIF:** Idle State Interrupt Flag bit

Set each time the IDLESF is set and if MCU did not trigger this change. This is unchanged when MCU aborts an action by clearing either of TXST, TXENC, RXDEC or EDST bits. This bit is cleared when PIR1 is read.

bit 3 **Reserved:** Maintain as '0'

bit 2 **CALSOIF:** Calibration Soft Interrupt Flag bit

CALSOIF = 1 indicates that Calibration is needed (CALST) although the radio is still functional. It also warns of a possible degradation in signal quality and consumption, and a risk of CALHAIF interrupt. This bit is cleared when PIR1 is read.

bit 1 **CALHAIF:** Calibration Hard Interrupt Flag bit

CALHAIF = 1 indicates that immediate Calibration (CALST) is mandatory, otherwise the radio is not functional. The device enters into malfunction state. This bit is cleared when PIR1 is read.

bit 0 **Reserved:** Maintain as '0'

**Note 1:** Generated non-maskable interrupt is gated off until the 1.2V reset is released.

**REGISTER 2-4: PIR2 (PERIPHERAL INTERRUPT REGISTER 2)** **ADDRESS: 0x05**

| R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 |
|---|---|---|---|---|---|---|---|
| TXIF | TXENCIF | TXMAIF | TXACKIF | TXCSMAIF | TXSZIF | TXOVFIF | FRMIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|---|
| -n = Value at POR | | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| r = Reserved | | HC = Hardware Clear | HS = Hardware Set | |

bit 7 **TXIF:** Transmission Done Interrupt Flag bit

The current TX operation (TXST) is successfully completed. This event is unchanged when a hardware generated ACK packet completed the transmission or when a packet is repeated. Nonpersistent, cleared by SPI read.

bit 6 **TXENCIF:** Transmit Encryption Interrupt Flag bit

The TX packet is successfully encrypted or complemented, or both with a Message Integrity Code (MIC). Set by the device after TXENC = 1, when TXENC is cleared. Nonpersistent, cleared by SPI read.

bit 5 **TXMAIF:** Transmitter Medium Access Interrupt Flag bit

Set by the device when the medium is accessed specifically when the first sample in the preamble is transmitted into the air. Nonpersistent, cleared by SPI read.

bit 4 **TXACKIF:** Transmission Unacknowledged Failure Interrupt Flag bit

Set by the device when Acknowledge is not received after the configured maximum number of transmission retries RETXMCNT<3:0>, provided that the Frame Control field of the transmitted frame indicates AckReq = 1. Nonpersistent, cleared by SPI read.

bit 3 **TXCSMAIF:** Transmitter CSMA Failure Interrupt Flag bit

Set by the device when CSMA-CA finds the channel busy for BOMCNT<2:0> number of times, provided that CSMAEN = 1 is configured. Nonpersistent, cleared by SPI read.

bit 2 **TXSZIF:** Transmit Packet Size Error Interrupt Flag bit

Set by the device if TX packet size (first byte of the TX buffer) is found to be zero or greater than the maximum size that the buffer can support. Automatic size check is performed after TXST is set by the user. Please note that the device may modify the packet length after CRC or MIC calculation. Nonpersistent, cleared by SPI read.

bit 1 **TXOVFIF:** Transmitter Overflow Interrupt Flag bit

The Host Controller attempted to write a TX buffer that was not empty (TXBUFEMPTY = 0).

Nonpersistent, cleared by SPI read.

bit 0 **FRMIF:** Frame Format Error Interrupt Flag bit

Set if the transmitter/receiver fails to parse the frame in the buffer (it is not as it must be or it is corrupted in demodulation).

**REGISTER 2-5: PIR3 (PERIPHERAL INTERRUPT REGISTER 3) ADDRESS: 0x06**

| R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 |
|---|---|---|---|---|---|---|---|
| RXIF | RXDECIF | RXTAGIF | r | RXIDENTIF | RXFLTIF | RXOVFIF | STRMIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|---|
| -n = Value at POR | | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| r = Reserved | | HC = Hardware Clear | HS = Hardware Set | |

bit 7 **RXIF:** Received Successful Interrupt Flag bit

Set by the device when a frame passed packet filtering and accepted, refer to Register 2-23. This interrupt flag is only set once for a packet and is not set when the packet is the duplicate of a repeated transmission (sequence number matches with the previously received frame).

Nonpersistent, cleared by SPI read.

bit 6 **RXDECIF:** Receiver Decryption/Authentication Passed Interrupt Flag bit

Set by the device when decryption/authentication finished without error.

Nonpersistent, cleared by SPI read.

bit 5 **RXTAGIF:** Receiver Decryption/Authentication Failure Interrupt Flag bit

Set by the device when decryption/authentication finished with error.

Nonpersistent, cleared by SPI read.

bit 4 **Reserved:** Maintain as '0'

bit 3 **RXIDENTIF:** Received Packet Identical Interrupt Flag bit

Set by the device when the packet is the duplicate of a repeated transmission (sequence number and source address matches with the previously received frame). Nonpersistent, cleared by SPI read.

bit 2 **RXFLTIF:** Received Packet Filtered Interrupt Flag bit

Set by the device when a packet is received, but rejected by one or more RX Filters, refer to Register 2-23.

Nonpersistent, cleared by SPI read.

bit 1 **RXOVFIF:** Receiver Overflow Error Interrupt Flag bit

Set by the device to indicate that a packet was received, but all RX buffers were full. Consequently the packet was not received, but was discarded instead(1).

Nonpersistent, cleared by SPI read.

bit 0 **STRMIF:** Receive Stream Time-Out Error Interrupt Flag bit

Set by the device to indicate that the duration specified in STRMTO elapsed since the last received packet while in RX-Streaming mode, and the MAC clears the stored sequence number.

Nonpersistent, cleared by SPI read.

**Note 1:** In Packet mode, use a single buffer for received frames. In RX-Streaming mode, use both buffers for reception.

**REGISTER 2-6: PIR4 (PERIPHERAL INTERRUPT REGISTER 4)(1)** **ADDRESS: 0x07**

| R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 | R/W/HS/HC-0 |
|---|---|---|---|---|---|---|---|
| TXSFDIF | RXSFDIF | ERRORIF | WARNIF | EDCCAIF | GPIO2IF | GPIO1IF | GPIO0IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|---|
| -n = Value at POR | | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| r = Reserved | | HC = Hardware Clear | HS = Hardware Set | |

bit 7 **TXSFDIF:** Transmit SFD Sent Interrupt Flag bit

Set by the device when the last sample of the SFD field is sent into the air.

Nonpersistent, cleared by SPI read

bit 6 **RXSFDIF:** Receive SFD Detected Interrupt Flag bit

Set by the device when the SFD field of the received frame is detected.

Nonpersistent, cleared by SPI read.

bit 5 **ERRORIF:** General Error Interrupt Flag bit

Set by the device, when malfunction state is reached.

bit 4 **WARNIF:** Warning Interrupt Flag bit

Set by the device when one of the following occurred:

- Battery voltage drops below the threshold by BATMON<4:0> at 0x3F
- Indicates that resistor is missing or improperly connected.

bit 3 **EDCCAIF:** Energy Detect/CCA Done Interrupt Flag bit

Set by the device when Energy-detect or CCA measurement is complete (following that the host MCU sets the EDST/CCAST bit to start the measurement and the device is clearing it for completion).

Nonpersistent. Cleared by SPI read.

bit 2 **GPIO2IF:** GPIO2 Interrupt Flag bit

Set by the device if the GPIOMODE register is set to normal operation, the GPIO is enabled and configured to input and the level matches with the polarity.

bit 1 **GPIO1IF:** GPIO1 Interrupt Flag bit

Set by the device if the GPIOMODE register is set to normal operation, the GPIO is enabled and configured to input and the level matches with the polarity.

bit 0 **GPIO0IF:** GPIO0 Interrupt Flag bit

Set by the device if the GPIOMODE register is set to normal operation, the GPIO is enabled and configured to input and the level matches with the polarity.

**Note 1:** CFOMEAS<7:0> indication becomes valid on SFD found.

**REGISTER 2-7: PIE1 (PERIPHERAL INTERRUPT ENABLE 1)** **ADDRESS: 0x08**

| R-0 | R/W-1 | R/W-1 | R-0 | R/W-1 | R/W-1 | R-0 |
|---|---|---|---|---|---|---|
| r | RDYIE | IDLEIE | r | CALSOIE | CALHAIE | r |
| bit 7 | | | | | | bit 0 |

| **Legend:** R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| r = Reserved | | | |

bit 7-6 **Reserved:** Maintain as '0'

bit 5 **RDYIE:** Ready Interrupt Enable bit
This bit masks the RDYIF interrupt bit.

bit 4 **IDLEIE:** Idle Interrupt Enable bit
This bit masks the IDLEIF interrupt bit.

bit 3 **Reserved:** Maintain as '0'

bit 2 **CALSOIE:** Calibration Soft Interrupt Enable bit
This bit masks the CALSOIF interrupt bit.

bit 1 **CALHAIE:** Calibration Hard Interrupt Enable bit
This bit masks the CALHAIF interrupt bit.

bit 0 **Reserved:** Maintain as '0'

**REGISTER 2-8: PIE2 (PERIPHERAL INTERRUPT ENABLE 2)** **ADDRESS: 0x09**

| R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| TXIE | TXENCIE | TXMAIE | TXACKIE | TXCSMAIE | TXSZIE | TXOVFIE | FRMIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|---|
| -n = Value at POR | | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| r = Reserved | | | | |

bit 7 **TXIE:** Transmit Interrupt Enable bit
This bit masks the TXIF interrupt bit.

bit 6 **TXENCIE:** Transmit Encryption and Authentication Interrupt Enable bit
This bit masks the TXENCIF interrupt bit.

bit 5 **TXMAIE:** Transmitter Medium Access Interrupt Enable bit
This bit masks the TXMAIF interrupt bit.

bit 4 **TXACKIE:** Transmission Unacknowledged Failure Interrupt Enable bit
This bit masks the TXACKIF interrupt bit.

bit 3 **TXCSMAIE:** Transmitter CSMA Failure Interrupt Enable bit
This bit masks the TXCSMAIF interrupt bit.

bit 2 **TXSZIE:** Transmit Packet Size Error Interrupt Enable bit
This bit masks the TXSZIF interrupt bit.

bit 1 **TXOVFIE:** Transmitter Overflow Interrupt Enable bit
This bit masks the TXOVFIF interrupt bit.

bit 0 **FRMIE:** Frame Format Error Interrupt Enable bit
This bit masks the FRMIF interrupt bit.