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Document Number: MRF373A
Rev. 7, 9/2008

RoHS

RF Power Field Effect Transistors

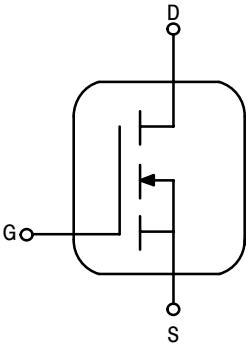
N-Channel Enhancement-Mode Lateral MOSFETs

MRF373ALR1
MRF373ALSR1

470-860 MHz, 75 W, 32 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs

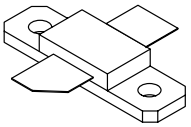
Designed for broadband commercial and industrial applications with frequencies from 470 to 860 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 28/32 volt transmitter equipment.

- Typical CW Performance at 860 MHz, 32 Volts, Narrowband Fixture
  Output Power — 75 Watts
  Power Gain — 18.2 dB
  Efficiency — 60%
- Capable of Handling 10:1 VSWR @ 32 Vdc, 860 MHz, 75 Watts CW Output Power

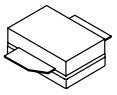


Features

- Integrated ESD Protection
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads.
  L Suffix Indicates 40μ″ Nominal.
- RoHS Compliant
- In Tape and Reel. R1 = 500 units per 32 mm, 13 inch Reel.



CASE 360B-05, STYLE 1
NI-360
MRF373ALR1



CASE 360C-05, STYLE 1
NI-360S
MRF373ALSR1

Table 1. Maximum Ratings

Rating		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-0.5, +70	Vdc
Gate-Source Voltage		V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	MRF373ALR1 MRF373ALSR1	P_D	197 1.12 278 1.59	W W/°C W W/°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Case Operating Temperature		T_C	150	°C
Operating Junction Temperature		T_J	200	°C

Table 2. Thermal Characteristics

Characteristic		Symbol	Value	Unit
Thermal Resistance, Junction to Case	MRF373ALR1 MRF373ALSR1	$R_{\theta JC}$	0.89 0.63	°C/W

Table 3. ESD Protection Characteristics

Test Conditions		Class
Human Body Model		1 (Minimum)
Machine Model	MRF373ALR1 MRF373ALSR1	M2 (Minimum) M1 (Minimum)

freescale semiconductor

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D =1 μA)	$V_{(BR)DSS}$	70	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 200 μA)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage (V_{DS} = 32 V, I_D = 100 mA)	$V_{GS(Q)}$	2.5	3.3	4.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	—	0.41	0.45	Vdc
Dynamic Characteristics					
Input Capacitance (V_{DS} = 32 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	98.5	—	pF
Output Capacitance (V_{DS} = 32 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	49	—	pF
Reverse Transfer Capacitance (V_{DS} = 32 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2	—	pF
Functional Characteristics (50 ohm system)					
Common Source Power Gain (V_{DD} = 32 V, P_{out} = 75 W CW, I_{DQ} = 200 mA, f = 860 MHz)	G_{ps}	16.5	18.2	—	dB
Drain Efficiency (V_{DD} = 32 V, P_{out} = 75 W CW, I_{DQ} = 200 mA, f = 860 MHz)	η	56	60	—	%

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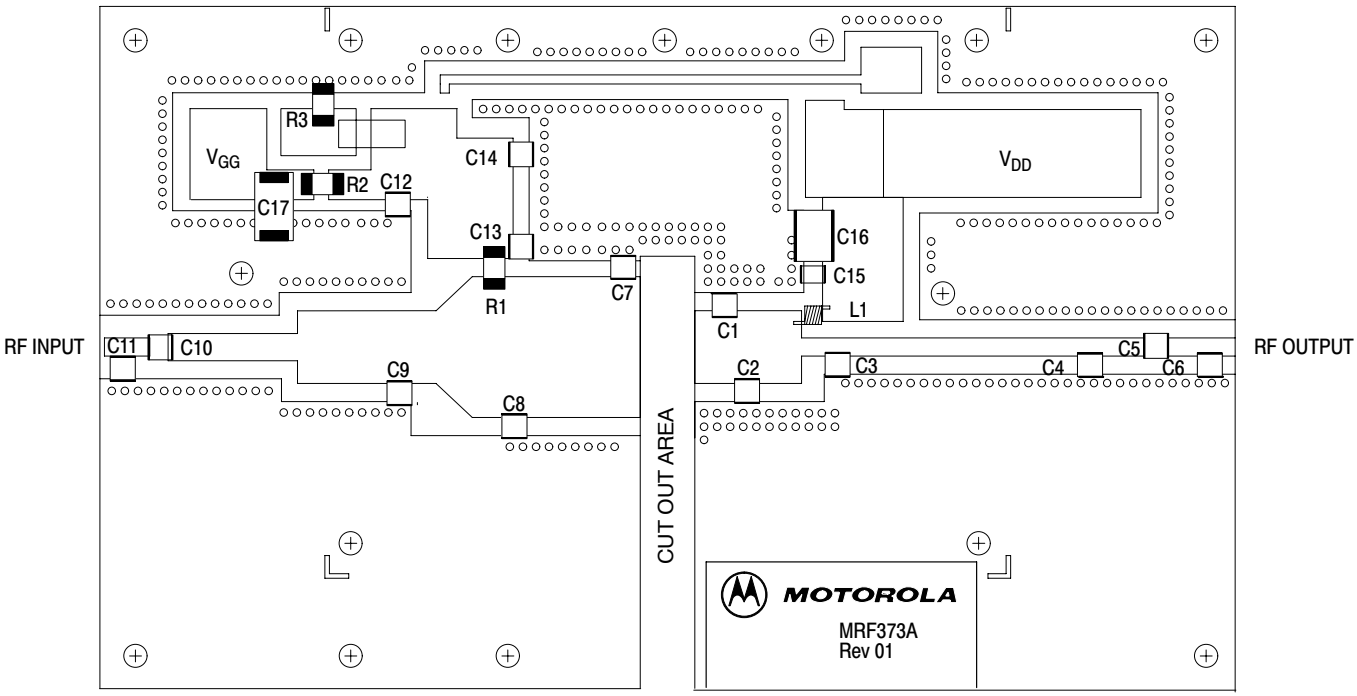


Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 1. MRF373ALR1/ALSR1 Narrowband Test Circuit Component Layout

Table 5. MRF373ALR1/ALSR1 Narrowband Test Circuit Component Layout Designations and Values

Designation	Description
C1, C2	18 pF Chip Capacitors
C3	12 pF Chip Capacitor
C4	1.8 pF Chip Capacitor
C5, C10	51 pF Chip Capacitors
C6	0.3 pF Chip Capacitor (Used only on the MRF373AS)
C7	15 pF Chip Capacitor
C8	10 pF Chip Capacitor
C9	2.7 pF Chip Capacitor
C11	0.5 pF Chip Capacitor
C12	1000 pF Chip Capacitor
C13	39 pF Chip Capacitor
C14, C15	470 pF Chip Capacitors
C16	2.2 μF, 100 V Chip Capacitor
C17	10 μF, 35 V Tantalum Capacitor
L1A	12 nH, Coilcraft
R1, R2	390 Ω, 1/2 W Chip Resistors (2010)
R3	1 kΩ, 1/2 W Chip Resistor (2010)
PCB	Arlon GX-0300-55, 30 mils, ε_r = 2.55

TYPICAL CHARACTERISTICS

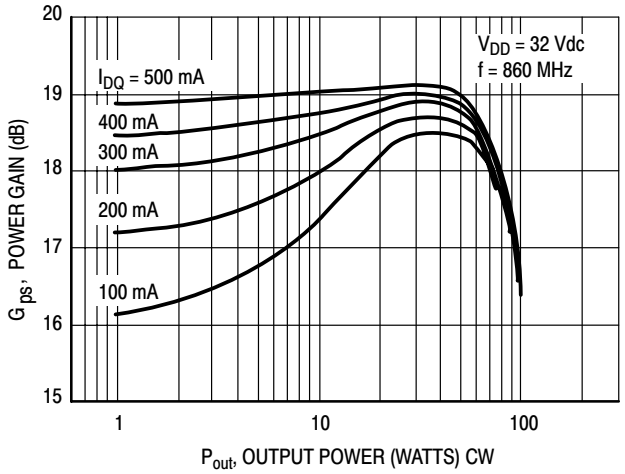


Figure 2. Power Gain versus Output Power

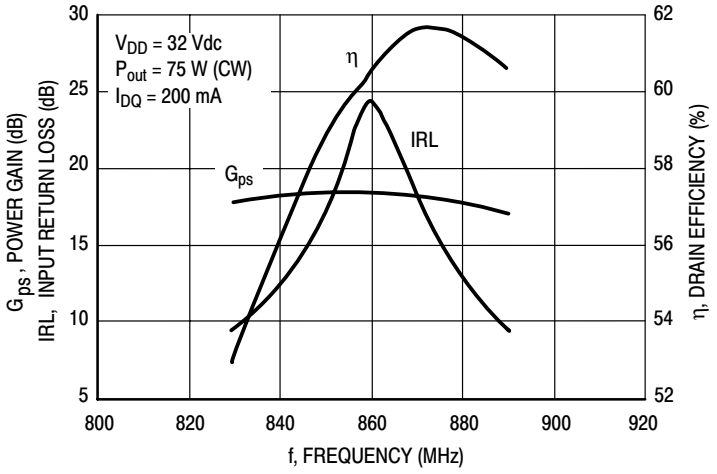


Figure 3. Performance in Narrowband Circuit

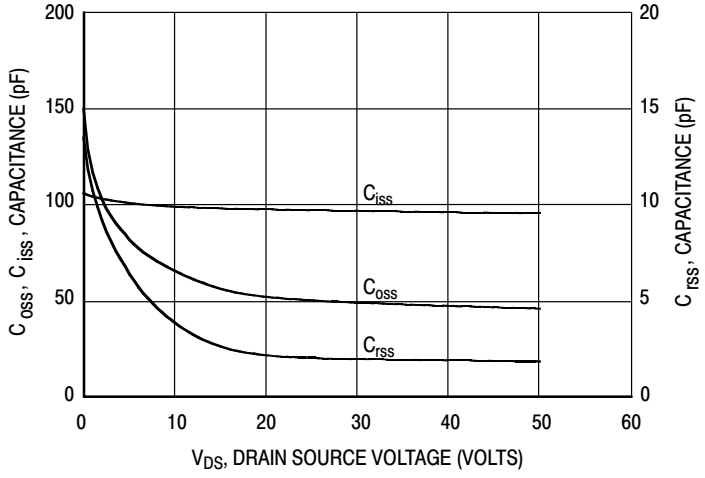
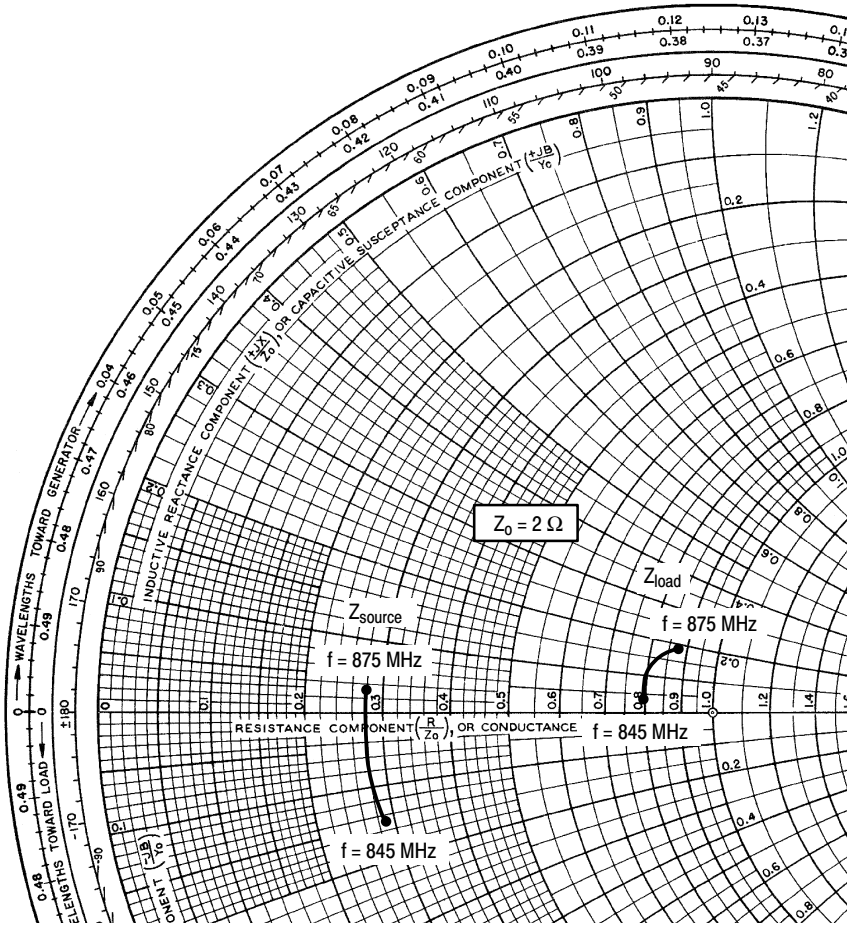


Figure 4. Capacitance versus Voltage



V_{DD} = 32 V, I_{DQ} = 200 mA, P_{out} = 75 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
845	0.58 - j0.29	1.60 + j0.07
860	0.56 - j0.11	1.65 + j0.22
875	0.56 + j0.06	1.79 + j0.38

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

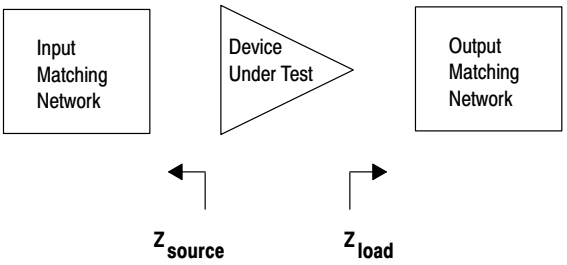
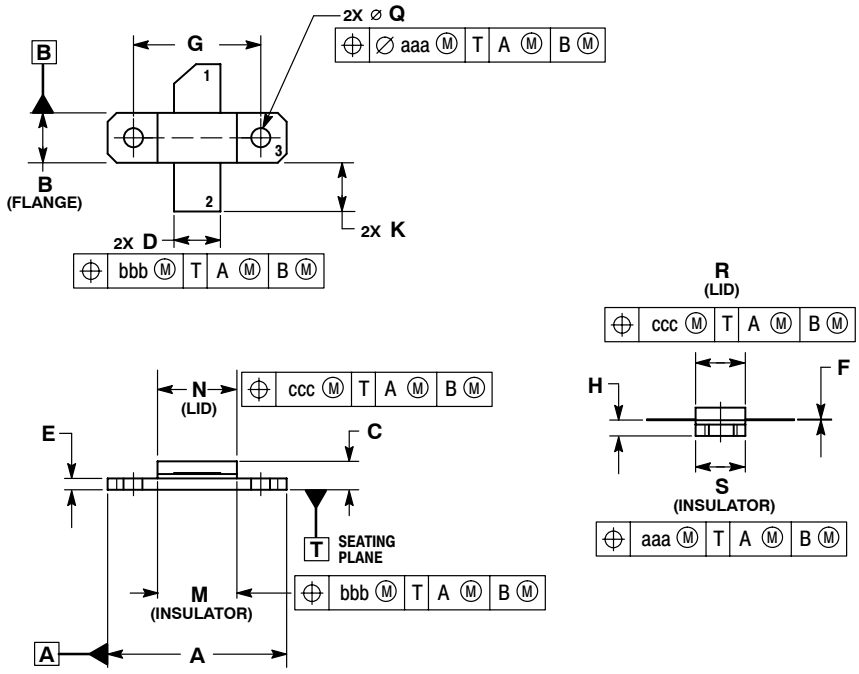


Figure 5. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS

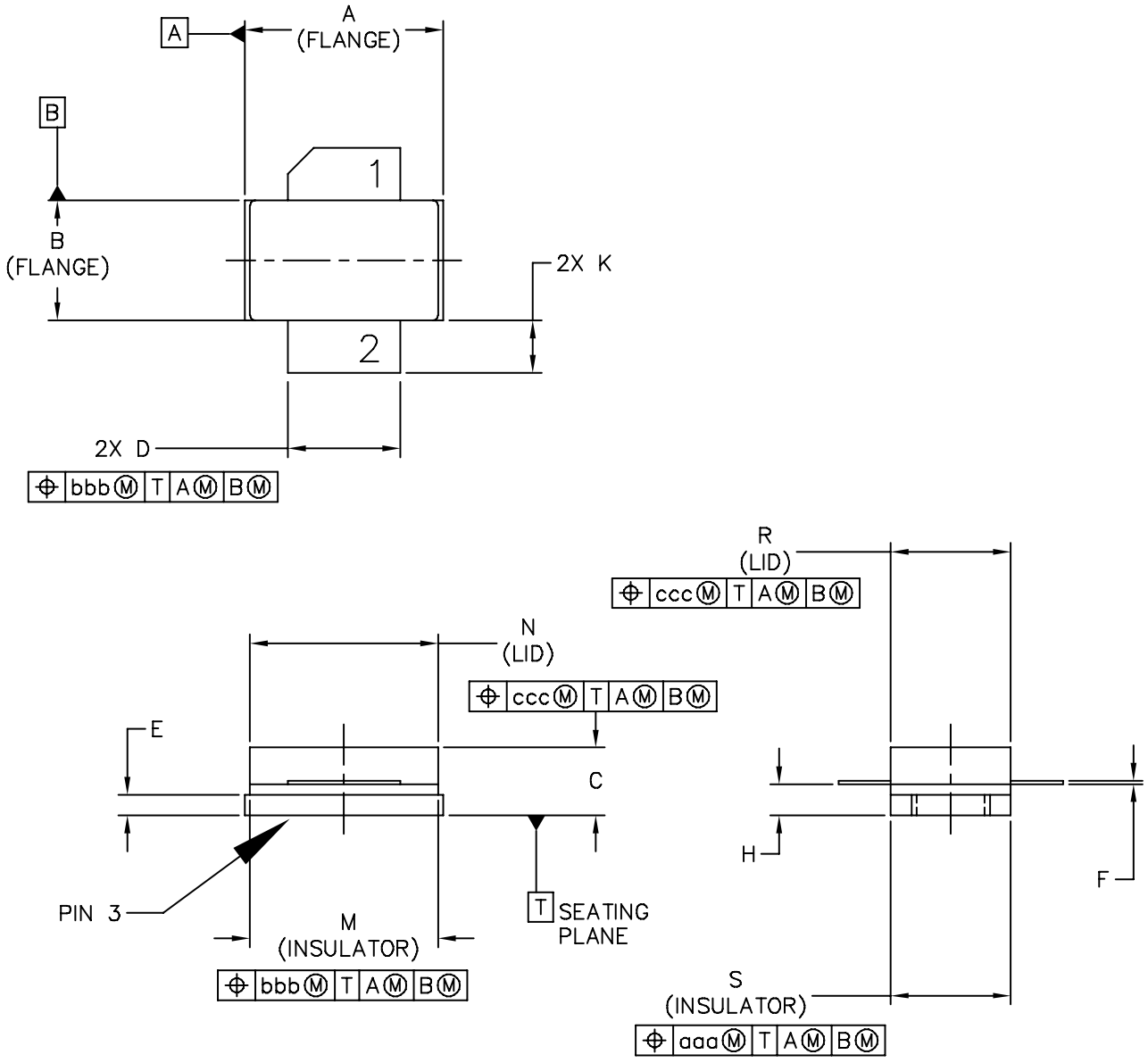


NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.795	0.805	20.19	20.45
B	0.225	0.235	5.72	5.97
C	0.125	0.175	3.18	4.45
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.10	0.15
G	0.562 BSC		14.28 BSC	
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
Q	0.125	0.135	3.18	3.43
R	0.227	0.233	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 360B-05
ISSUE G
NI-360
MRF373ALR1



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	CASE NUMBER: 360C-05	10 MAR 2006
	STANDARD: NON-JEDEC	

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY

STYLE 1:
PIN 1 – DRAIN
2 – GATE
3 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.375	.385	9.53	9.78	N	.357	.363	9.07	9.22
B	.225	.235	5.72	5.97	R	.227	.233	5.77	5.92
C	.105	.155	2.67	3.94	S	.225	.235	5.72	5.97
D	.210	.220	5.33	5.59					
E	.035	.045	0.89	1.14	aaa	.005		0.13	
F	.004	.006	0.1	0.15	bbb	.010		0.25	
H	.057	.067	1.45	1.7	ccc	.015		0.38	
K	.085	.115	2.16	2.92					
M	.355	.365	9.02	9.27					

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NI–360S SURFACE MOUNT	CASE NUMBER: 360C–05	10 MAR 2006
	STANDARD: NON–JEDEC	

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PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
7	Sept. 2008	• Replaced Case Outline 360C-05, Issue E with Issue F, p. 7-8. • Added Product Documentation and Revision History, p. 9

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Document Number: MRF373A
Rev. 7, 9/2008