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MRF39RA

Low-Power, Integrated UHF Receiver

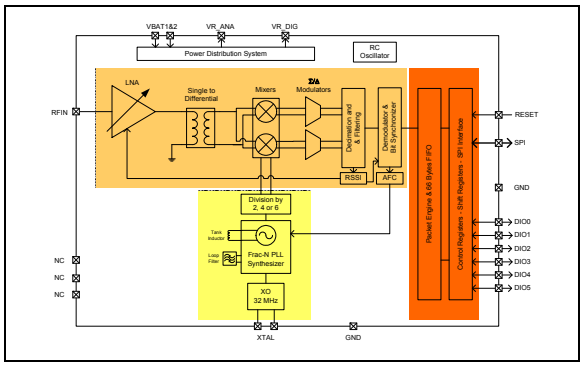
Features

- High Sensitivity:
  - down to -120 dBm at 1.2 kbps
- High Selectivity:
  - 16-Tap FIR channel filter
- Bullet-Proof Front End:
  - IIP3 = -18 dBm, IIP2 = +35 dBm, 80 dB blocking immunity, no image frequency response
- Low Current:
  - Rx = 16 mA, 100 nA register retention
- Constant RF Performance over Voltage Range of Chip
- FSK Bit Rates up to 300 kbps
- Fully Integrated Synthesizer with a Resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK Demodulation
- Built-in Bit Synchronizer Performing Clock Recovery
- Incoming Sync Word Recognition
- 115 dB+ Dynamic Range Received Signal Strength Indicator (RSSI)
- Automatic RF Sense with Ultra-Fast Automatic Frequency Control (AFC)
- Packet Engine with CRC, AES-128 Encryption and 66-Byte First In First Out (FIFO)
- Built-in Temperature Sensor and Low-Battery Indicator

General Description

The MRF39RA device is a highly integrated RF receiver capable of operation over a wide frequency range, including the 433, 868 and 915 MHz license-free Industry Scientific and Medical (ISM) frequency bands. Its highly integrated architecture enables for a minimum of external components while maintaining maximum design flexibility. All major RF communication parameters are programmable and most of these can be dynamically set. The MRF39RA offers the unique advantage of programmable narrow-band and wide-band communication modes without the need of modifying external components. The MRF39RA is optimized for low-power consumption while offering high sensitivity and channelized operation. TrueRF™ technology enables a low-cost external component count (elimination of the SAW filter) while still satisfying the European Telecommunications Standards Institute (ETSI) and Federal Communications Commission (FCC) regulations.

FIGURE 1: MRF39RA RECEIVER: LOW-POWER INTEGRATED UHF RECEIVER

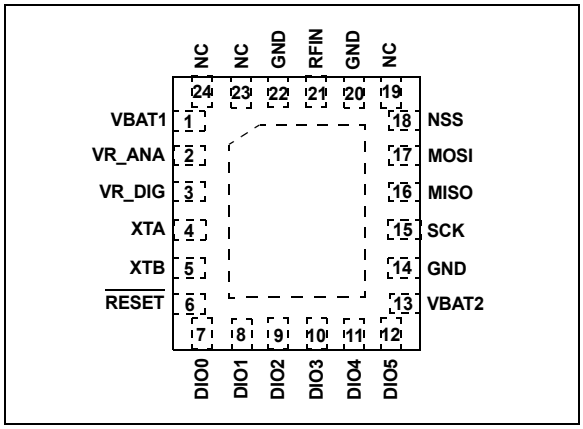


Typical Applications

- Automated Meter Reading
- Wireless Sensor Networks
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Wireless M-Bus

Pin Diagram

FIGURE 2: 24-PIN QFN



Markets

- Europe: EN 300-220-1
- North America: FCC Part 15.247, 15.249, 15.231
- Narrow Korean and Japanese Bands

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1.0 OVERVIEW

The MRF39RA is a single-chip integrated circuit ideally suited for today's high-performance ISM band RF applications. The MRF39RA's advanced features set, including state-of-the-art packet engine, greatly simplifies system design while the high level of integration reduces the external bill of materials (BOM) to a handful of passive decoupling and matching components. It is intended for use as a high-performance, low-cost FSK and OOK RF receiver for robust frequency agile RF links, and where stable and constant RF performance is required over the full operating range of the device down to 1.8V.

The MRF39RA is intended for applications over a wide frequency range, including the 433 MHz and 868 MHz European and 902-928 MHz North American ISM bands. Coupled with a very aggressive sensitivity, the advanced system features of the MRF39RA include a 66-byte RX FIFO, configurable automatic packet handler, Listen mode, temperature sensor and configurable DIOs, which greatly enhance system flexibility while significantly reducing MCU requirements at the same time.

The MRF39RA complies with both ETSI and FCC regulatory requirements and is available in a 5 x 5 mm 24-lead QFN package.

FIGURE 1-1: SIMPLIFIED BLOCK DIAGRAM

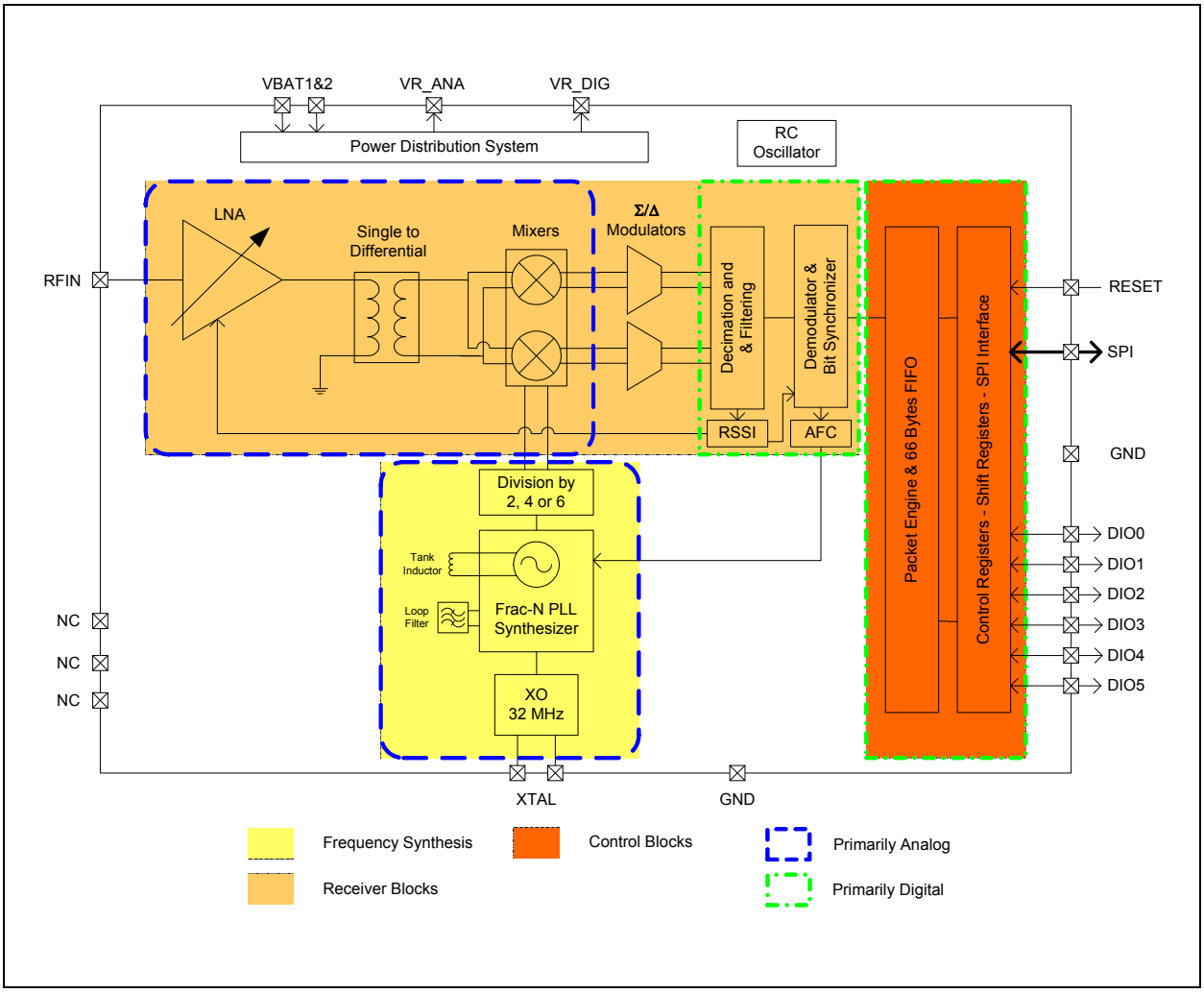


Table 1-1 lists the MRF39RA pinouts.

TABLE 1-1: MRF39RA PINOUTS

Number	Name	Type	Description
0	GROUND	—	Exposed Ground Pad
1	VBAT1	—	Supply Voltage
2	VR_ANA	—	Regulated Supply Voltage for Analogue Circuitry
3	VR_DIG	—	Regulated Supply Voltage for Digital Blocks
4	XTA	I/O	XTAL Connection
5	XTB	I/O	XTAL Connection
6	$\overline{\text{RESET}}$	I/O	Reset Trigger Input
7	DIO0	I/O	Digital I/O; Software Configured
8	DIO1/DCLK	O	Digital Output; Software Configured
9	DIO2/DATA	O	Digital Output; Software Configured
10	DIO3	I/O	Digital I/O; Software Configured
11	DIO4	I/O	Digital I/O; Software Configured
12	DIO5	I/O	Digital I/O; Software Configured
13	VBAT2	—	Supply Voltage
14	GND	—	Ground
15	SCK	I	SPI Clock Input
16	MISO	O	SPI Data Output
17	MOSI	I	SPI Data Input
18	NSS	I	SPI Chip Select Input
19	NC	—	Do not connect
20	GND	—	Ground
21	RFIN	I	RF Input
22	GND	—	Ground
23	NC	—	Do not connect
24	NC	—	Do not connect

2.0 DEVICE DESCRIPTION

This section describes in detail the architecture of the MRF39RA low-power, highly integrated receiver.

2.1 Power Supply Strategy

The MRF39RA employs an advanced power supply scheme, which provides stable operating characteristics over the full temperature and voltage range of operation.

The MRF39RA can be powered from any low-noise voltage source via pins VBAT1 and VBAT2. As suggested in the reference design, decoupling capacitors must be connected on VR_DIG and VR_ANA pins to ensure a correct operation of the built-in voltage regulators.

2.2 Low Battery Detector

A low battery detector is also included enabling the generation of an interrupt signal in response to passing a programmable threshold adjustable through the RegLowBat register. The interrupt signal can be mapped to any of the DIO pins through the programming of RegDioMapping.

2.3 Frequency Synthesis

The LO generation on the MRF39RA is based on a state-of-the-art fractional-N PLL. The PLL is fully integrated with automatic calibration.

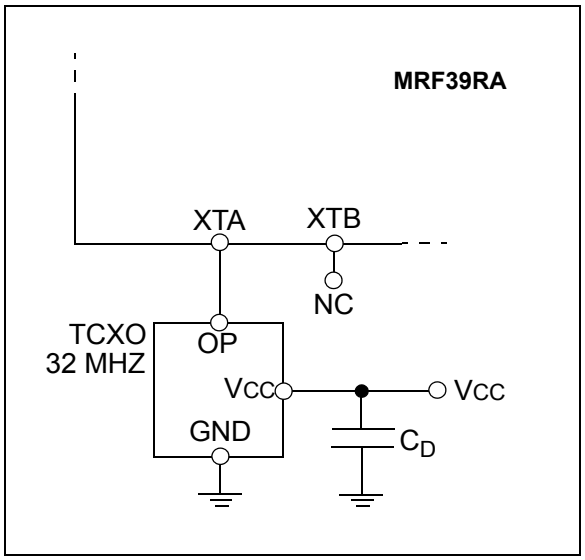
2.3.1 REFERENCE OSCILLATOR

The crystal oscillator is the main timing reference of the MRF39RA. It is used as a reference for the frequency synthesizer and as a clock for the digital processing.

The XO start-up time, TS_OSC, depends on the actual XTAL being connected on pins XTA and XTB. When using the built-in sequencer, the MRF39RA optimizes the start-up time and automatically triggers the PLL when the XO signal is stable. To manually control the start-up time, the user must either wait for TS_OSC max, or monitor the signal CLKOUT, which is only made available on the output buffer when a stable XO oscillation is achieved.

An external clock can be used to replace the crystal oscillator, for instance a tight tolerance TCXO. To do this, bit 4 at address 0x59 must be set to '1', and the external clock has to be provided on XTA (pin 4). XTB (pin 5) must be left open. The peak-peak amplitude of the input signal must never exceed 1.8V. Consult the TCXO supplier for an appropriate value of decoupling capacitor, CD. Figure 2-1 shows the TCXO connection.

FIGURE 2-1: TCXO CONNECTION



2.3.2 CLKOUT OUTPUT

The reference frequency, or a fraction of it, can be provided on DIO5 (pin 12) by modifying bits ClkOut in RegDioMapping2. Two typical applications of the CLKOUT output include:

- Providing a clock output for a companion processor, thus saving the cost of an additional oscillator; CLKOUT can be made available in any operation mode except Sleep mode and is automatically enabled at Power-on Reset
- Providing an oscillator reference output; measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note: To minimize the current consumption of the MRF39RA, ensure that the CLKOUT signal is disabled when not required.

2.3.3 PLL ARCHITECTURE

The frequency synthesizer generating the LO frequency for the receiver is a fractional-N sigma-delta PLL. The PLL incorporates a third-order loop capable of fast auto-calibration, and it has a fast switching time. The VCO and the loop filter are both fully integrated, removing the need for an external tight-tolerance, high-Q inductor in the VCO tank circuit.

2.3.3.1 VCO

The VCO runs at two, four or six times the RF frequency (respectively in the 915, 434 and 315 MHz bands) to reduce any LO leakage in Receiver mode, to improve the quadrature precision of the receiver.

The VCO calibration is fully automated. A coarse adjustment is carried out at Power-on Reset, and a fine tuning is performed each time the MRF39RA PLL is activated. Automatic calibration times are fully transparent to the end user as their processing time is included in the TS_RE specifications.

2.3.3.2 PLL Bandwidth

The bandwidth of the MRF39RA Fractional-N PLL is wide enough to enable for very fast PLL lock times, enabling both short start-up and fast hop times required for frequency-agile applications.

2.3.3.3 Carrier Frequency and Resolution

The MRF39RA PLL embeds a 19-bit sigma-delta modulator and its frequency resolution, constant over the whole frequency range, see Equation 2-1.

EQUATION 2-1: CARRIER FREQUENCY STEP

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

The carrier frequency is programmed through RegFrf, split across addresses 0x07 to 0x09:

EQUATION 2-2: CARRIER FREQUENCY

$$F_{RF} = F_{STEP} \times Frf(23,0)$$

Note: The Frf setting is split across three bytes. A change in the center frequency is only taken into account when the Least Significant Byte FrfLsb in RegFrfLsb is written.

2.3.4 LOCK TIME

PLL lock time TS_FS is a function of a number of technical factors, such as synthesized frequency, frequency step, and so on. When using the built-in sequencer, the MRF39RA optimizes the start-up time and automatically starts the receiver when the PLL is locked. To manually control the start-up time, the user must either wait for TS_FS max as given in the specification, or monitor the signal PLL lock detect indicator, which is set when the PLL is within its locking range.

When performing an AFC, which usually corrects very small frequency errors, the PLL response time is shown in Equation 2-3.

EQUATION 2-3: PLL RESPONSE TIME

$$T_{PLLAFC} = \frac{5}{PLLBW}$$

In a frequency hopping scheme, the TS_HOP timings in Table 7-4 give an order of magnitude for the expected lock times.

2.3.5 LOCK DETECT INDICATOR

A lock indication signal can be made available on some of the DIO pins, which is toggled high when the PLL reaches its locking range. Refer to Table 4-2 and Table 4-3 to map this interrupt to the desired pins.

2.4 Receiver Description

The MRF39RA features a digital receiver with the Analog-to-Digital conversion process being performed directly following the LNA-mixers block. The zero-IF receiver is able to handle (G)FSK and (G)MSK modulation. ASK and OOK modulation is, however, demodulated by a low-IF architecture. All the filtering, demodulation, gain control, synchronization and packet handling is performed digitally, which enables a very wide range of bit rates and frequency deviations to be selected. The receiver is also capable of automatic gain calibration to improve precision on RSSI measurements.

FIGURE 2-2: RECEIVER BLOCK DIAGRAM

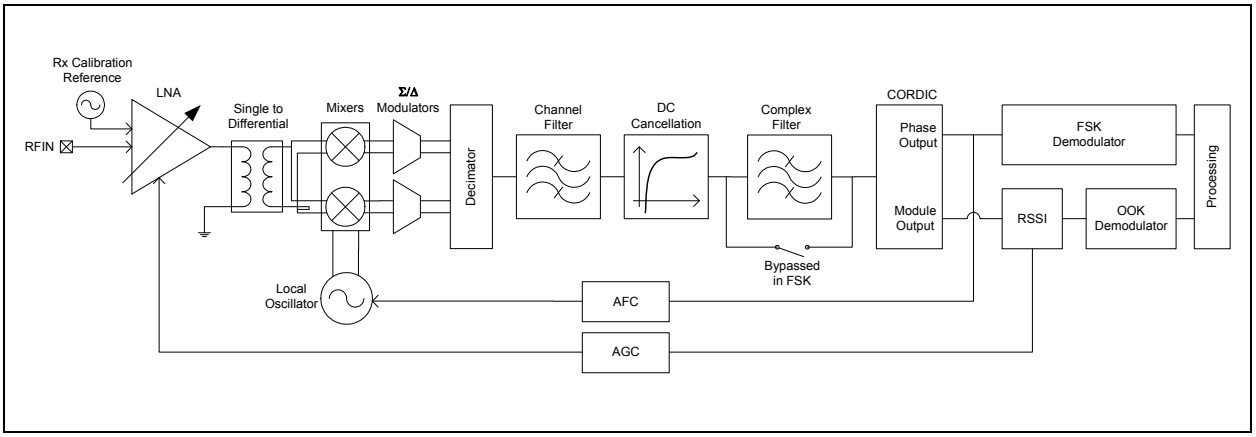


Figure 2-2 shows the receiver block diagram, and the following sections provides a brief description of each of the receiver blocks.

2.4.1 LNA – SINGLE-TO-DIFFERENTIAL BUFFER

The LNA uses a common-gate topology, which enables for a flat characteristic over the whole frequency range. It is designed to have an input impedance of 50 Ohms or 200 Ohms (as selected with bit LnaZin in RegLna), and the parasitic capacitance at the LNA input port is canceled with the external RF choke. A single-to-differential buffer is implemented to improve the second order linearity of the receiver.

The LNA gain, including the single-to-differential buffer, is programmable over a 48 dB dynamic range, and control is either manual or automatic with the embedded AGC function.

Note: In the specific case where the LNA gain is manually set by the user, the receiver is unable to properly handle FSK signals with a modulation index smaller than 2 at an input power greater than the 1 dB compression point, tabulated in **Section 2.4.2 "Automatic Gain Control"**.

Table 2-1 shows the LNA Gain settings.

TABLE 2-1: LNA GAIN SETTINGS

LnaGainSelect	LNA Gain	Gain Setting
000	Any of the below, set by the AGC loop	—
001	Max gain	G1
010	Max gain – 6 dB	G2
011	Max gain – 12 dB	G3
100	Max gain – 24 dB	G4
101	Max gain – 36 dB	G5
110	Max gain – 48 dB	G6
111	Reserved	—

2.4.2 AUTOMATIC GAIN CONTROL

By default (LnaGainSelect = 000) the LNA gain is controlled by a digital AGC loop to obtain the optimal sensitivity/linearity trade-off.

Regardless of the Data Transfer mode (Packet or Continuous), the following series of events takes place when the receiver is enabled:

- The receiver stays in Wait mode, until RssiValue exceeds RssiThreshold for two consecutive samples. Its power consumption is the receiver power consumption.
- When this condition is satisfied, the receiver automatically selects the most suitable LNA gain, optimizing the sensitivity/linearity trade-off.
- The programmed LNA gain, read-accessible with LnaCurrentGain in RegLna, is carried on for the whole duration of the packet, until one of the following conditions is fulfilled:
- **Packet mode**: if AutoRxRestartOn = 0, the LNA gain remains the same for the reception of the following packet. If AutoRxRestartOn = 1, after the controller has emptied the FIFO the receiver re-enters the Wait mode, after a delay of InterPacketRxDelay, enabling for the distant transmitter to ramp down, hence avoiding a false RSSI detection. In both cases (AutoRxRestartOn = 0 or AutoRxRestartOn = 1), the receiver can also re-enter the Wait mode by setting RestartRx bit to '1'. The user can decide to do this to manually launch a new AGC procedure.
- **Continuous mode**: upon reception of valid data, the user can decide to either leave the receiver enabled with the same LNA gain, or to restart the procedure, by setting RestartRx bit to '1', resuming the Wait mode of the receiver, described above.

Figure 2-3 illustrates the AGC behavior.

Note 1: The AGC procedure must be performed while receiving preamble in FSK mode.

2: In OOK mode, the AGC gives better results if performed while receiving a constant '1' sequence.

FIGURE 2-3: AGC THRESHOLDS SETTINGS

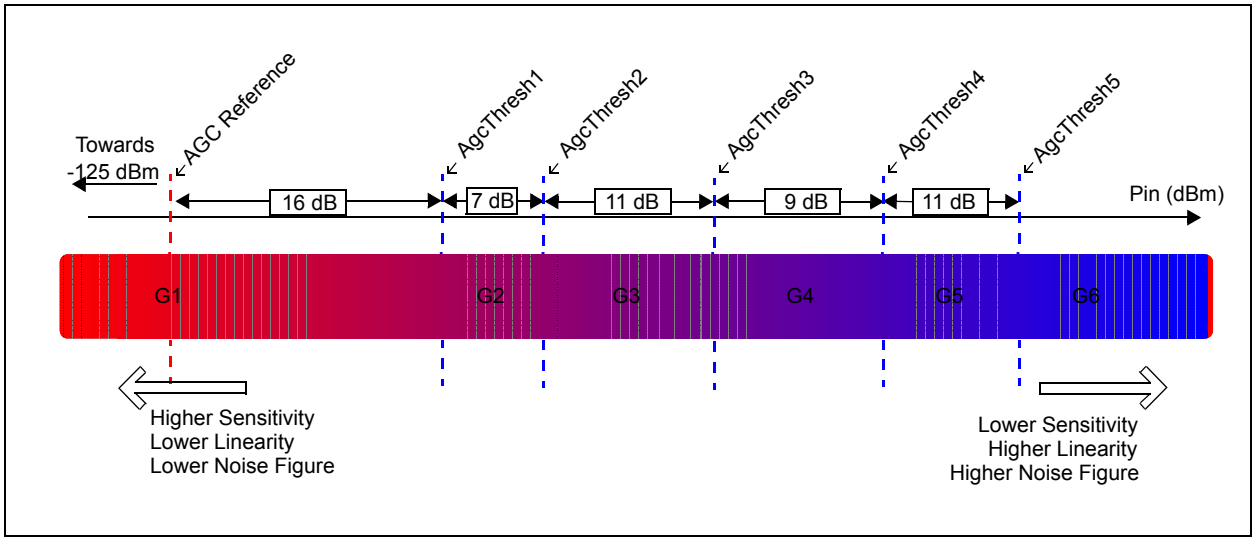


Table 2-2 summarizes the performance (typical figures) of the complete receiver.

TABLE 2-2: RECEIVER PERFORMANCE SUMMARY

Input Power Pin	Gain Setting	Receiver Performance (typ.)			
		P_{-1dB} [dBm]	NF [dB]	IIP3 [dBm]	IIP2 [dBm]
Pin < AgcThresh1	G1	-37	7	-18	+35
AgcThresh1 < Pin < AgcThresh2	G2	-31	13	-15	+40
AgcThresh2 < Pin < AgcThresh3	G3	-26	18	-8	+48
AgcThresh3 < Pin < AgcThresh4	G4	-14	27	-1	+62
AgcThresh4 < Pin < AgcThresh5	G5	>-6	36	+13	+68
AgcThresh5 < Pin	G6	>0	44	+20	+75

2.4.2.1 RssiThreshold Setting

For correct operation of the AGC, set the RssiThreshold in RegRssiThresh to the sensitivity of the receiver. The receiver remains in Wait mode until RssiThreshold is exceeded.

Note: When AFC is enabled and automatically performed at the receiver start-up, the channel filter used by the receiver during the AFC and AGC is RxBwAfc instead of the standard RxBw setting. This may impact the sensitivity of the receiver and the setting of RssiThreshold accordingly.

2.4.2.2 AGC Reference

The AGC reference level is automatically computed in the MRF39RA, according to the formula in Equation 2-4.

EQUATION 2-4: AGC REFERENCE LEVEL

$$AGC\ Reference\ [dBm] = -174 + NF + DemoSnr + 10.log(2*RxBw) + FadingMargin[dBm]$$

Where:

NF = 7 dB : LNA's Noise Figure at maximum gain

DemodSnr = 8 dB : SNR needed by the demodulator

RxBw : Single sideband channel filter bandwidth

FadingMargin = 5 dB : Fading margin

2.4.3 CONTINUOUS-TIME DAGC

In addition to the automatic gain control described in **Section 2.4.2 "Automatic Gain Control"**, the MRF39RA is capable of continuously adjusting its gain in the digital domain, after the Analog-to-Digital conversion has occurred. This feature, named DAGC, is fully transparent to the end user. The digital gain adjustment is repeated every two bits and has the following benefits:

- Fully transparent to the end user
- Improves the fading margin of the receiver during the reception of a packet, even if the gain of the LNA is frozen
- Improves the receiver robustness in fast fading signal conditions by quickly adjusting the receiver gain (every two bits)
- Works in Continuous, Packet and Unlimited Length Packet modes.

The DAGC is enabled by setting RegTestDagc to 0x20 for low modulation index systems (i.e., when AfcLowBetaOn = '1') and 0x30 for other systems. See **Section 2.4.17 "Optimized Setup for Low Modulation Index Systems"**. It is recommended to always enable the DAGC.

2.4.4 QUADRATURE MIXER – ADCs – DECIMATORS

The mixer is inserted between the output of the RF buffer stage and the input of the Analog-to-Digital Converter (ADC) of the receiver section. This block is designed to translate the spectrum of the input RF signal to base-band, and offer both high IIP2 and IIP3 responses.

In the lower bands of operation (290 to 510 MHz), the multi-phase mixing architecture with weighted phases improves the rejection of the LO harmonics in Receiver mode, hence increasing the receiver immunity to out-of-band interferers.

The I and Q digitalization is made by two 5th order continuous-time sigma-delta Analog-to-Digital Converters (ADC). Gain is not constant over temperature, but the whole receiver is calibrated before reception that this inaccuracy has no impact on the RSSI precision. The ADC output is one bit per channel. It needs to be decimated and filtered afterwards. This ADC can also be used for temperature measurement. For more details, refer to **Section 2.4.18 "Temperature Sensor"**.

The decimators decrease the sample rate of the incoming signal to optimize the area and power consumption of the following receiver blocks.

2.4.5 CHANNEL FILTER

The role of the channel filter is to filter out the noise and interferers outside of the channel. Channel filtering on the MRF39RA is implemented with a 16-tap finite impulse response (FIR) filter, providing an outstanding adjacent channel rejection performance, even for narrow-band applications.

Note:	To respect oversampling rules in the decimation chain of the receiver, the bit rate cannot be set at a higher value than two times the single-side receiver bandwidth (BitRate < 2 x RxBw)

The single-side channel filter bandwidth RxBw is controlled by the RxBwMant and RxBwExp parameters in RegRxBw, as shown in Equation 2-5.

EQUATION 2-5: RXBW

When FSK modulation is enabled:

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp + 2}}$$

When OOK modulation is enabled:

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp + 3}}$$

Table 2-3 lists the accessible channel filter bandwidths (oscillator is mandated at 32 MHz).

TABLE 2-3: AVAILABLE RxBw SETTINGS

RxBwMant (binary/value)	RxBwExp (decimal)	RxBw (kHz)	
		FSK ModulationType = 00	OOK ModulationType = 01
10b/24	7	2.6	1.3
01b/20	7	3.1	1.6
00b/16	7	3.9	2.0
10b/24	6	5.2	2.6
01b/20	6	6.3	3.1
00b/16	6	7.8	3.9
10b/24	5	10.4	5.2
01b/20	5	12.5	6.3
00b/16	5	15.6	7.8
10b/24	4	20.8	10.4
01b/20	4	25.0	12.5
00b/16	4	31.3	15.6
10b/24	3	41.7	20.8
01b/20	3	50.0	25.0
00b/16	3	62.5	31.3
10b/24	2	83.3	41.7
01b/20	2	100.0	50.0
00b/16	2	125.0	62.5
10b/24	1	166.7	83.3
01b/20	1	200.0	100.0
00b/16	1	250.0	125.0
10b/24	0	333.3	166.7
01b/20	0	400.0	200.0
00b/16	0	500.0	250.0

2.4.6 DC CANCELLATION

DC cancellation is required in zero-IF architecture transceivers to remove any DC offset generated through self-reception. It is built in the MRF39RA and its adjustable cutoff frequency (fc) is controlled in RegRxBw. Table 2-4 shows the available DCC cutoff frequencies.

TABLE 2-4: AVAILABLE DCC CUTOFF FREQUENCIES

DccFreq in RegRxBw	fc in % of RxBw
000	16
001	8
010 (default)	4
011	2
100	1
101	0.5
110	0.25
111	0.125

The default value of DccFreq cutoff frequency is typically 4% of the RxBw (channel filter BW). The cutoff frequency of the DCC can however be increased to slightly improve the sensitivity, under wider modulation conditions. It is advised to adjust the DCC setting while monitoring the receiver sensitivity.

2.4.7 COMPLEX FILTER – OOK

In OOK mode the MRF39RA is modified to a low-IF architecture. The IF frequency is automatically set to half the single-side bandwidth of the channel filter (FIF = 0.5 x RxBw). The Local Oscillator is automatically offset by the IF in the OOK receiver. A complex filter is implemented on the chip to attenuate the resulting image frequency by typically 30 dB.

Note:	This filter is automatically bypassed when receiving FSK signals (ModulationType = 00 in RegDataModul).

2.4.8 RSSI

The RSSI block evaluates the amount of energy available within the receiver channel bandwidth. Its resolution is 0.5 dB, and it has a wide dynamic range to accommodate both small and large signal levels that may be present. Its acquisition time is very short, only taking 2-bit periods. The RSSI sampling must occur during the reception of preamble in FSK and constant '1' reception in OOK. Figure 2-4 shows the RSSI dynamic curve.

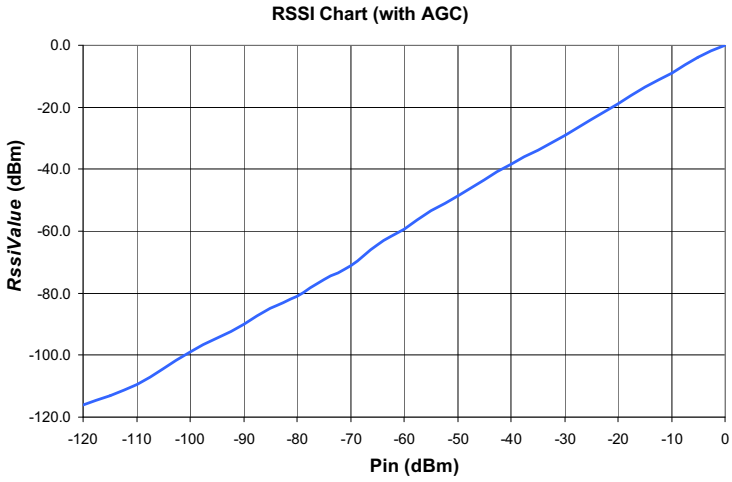
Note 1: RssiValue can only be read when it exceeds RssiThreshold.

2: RssiStart command and RssiDone flags are not usable when DAGC is turned on. See **Section 2.4.3 "Continuous-Time DAGC"**.

3: The receiver is capable of automatic gain calibration to improve the precision of its RSSI measurements. This function injects a known RF signal at the LNA input and calibrates the receiver gain accordingly. This calibration is automatically performed during the PLL start-up, making it a transparent process to the end user.

4: RSSI accuracy depends on all components located between the antenna port and pin RFIO and is therefore limited to a few decibels. Board-level calibration is advised to further improve accuracy.

FIGURE 2-4: RSSI DYNAMIC CURVE



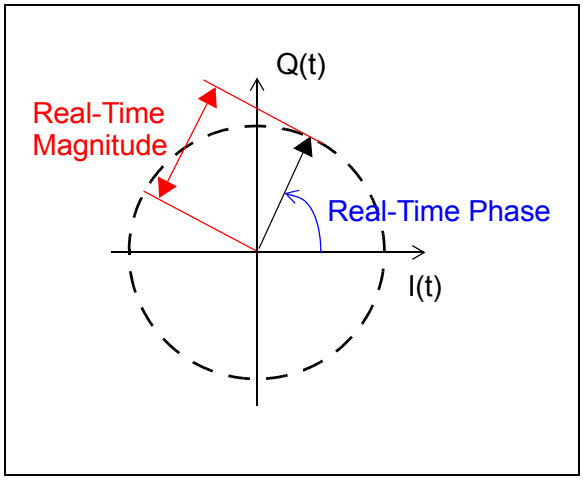
2.4.9 CORDIC

The Cordic task is to extract the phase and the amplitude of the modulation vector (I + j.Q). The following information is used, still in the digital domain:

- **Phase output**: used by the FSK demodulator and the AFC blocks
- **Amplitude output**: used by the RSSI block for FSK demodulation, AGC and automatic gain calibration purposes.

Figure 2-5 shows the cordic extraction.

FIGURE 2-5: CORDIC EXTRACTION



2.4.10 BIT RATE SETTING

The bit rate (BR) is controlled by the BitRate bits in RegBitrate, as shown in Equation 2-6 below.

EQUATION 2-6: BIT RATE

$$BR = \frac{F_{XOSC}}{BitRate}$$

Table 2-5 lists some of the accessible bit rates.

TABLE 2-5: BIT RATE EXAMPLES

Type	BitRate <15:8>	BitRate <7:0>	(G)FSK (G)MSK	OOK	Actual BR (b/s)
Classical Modem Baud Rates (multiples of 1.2 kbps)	0x68	0x2B	1.2 kbps	1.2 kbps	1200.015
	0x34	0x15	2.4 kbps	2.4 kbps	2400.060
	0x1A	0x0B	4.8 kbps	4.8 kbps	4799.760
	0x0D	0x05	9.6 kbps	9.6 kbps	9600.960
	0x06	0x83	19.2 kbps	19.2 kbps	19196.16
	0x03	0x41	38.4 kbps	—	38415.36
	0x01	0xA1	76.8 kbps	—	76738.60
	0x00	0xD0	153.6 kbps	—	153846.1
Classical Modem Baud Rates (multiples of 0.9 kbps)	0x02	0x2C	57.6 kbps	—	57553.95
	0x01	0x16	115.2 kbps	—	115107.9
Round Bit Rates (multiples of 12.5, 25 and 50 kbps)	0x0A	0x00	12.5 kbps	12.5 kbps	12500.00
	0x05	0x00	25 kbps	25 kbps	25000.00
	0x02	0x80	50 kbps	—	50000.00
	0x01	0x40	100 kbps	—	100000.0
	0x00	0xD5	150 kbps	—	150234.7
	0x00	0xA0	200 kbps	—	200000.0
	0x00	0x80	250 kbps	—	250000.0
	0x00	0x6B	300 kbps	—	299065.4
Watch Xtal Frequency	0x03	0xD1	32.768 kbps	32.768 kbps	32753.32

2.4.11 FSK DEMODULATOR

The FSK demodulator of the MRF39RA is designed to demodulate FSK, GFSK, MSK and GMSK modulated signals. It is most efficient when the modulation index of the signal is greater than 0.5 and below 10, see Equation 2-7.

EQUATION 2-7: MODULATION INDEX

$$0.5 \le \beta = \frac{2 \times F_{DEV}}{BR} \le 10$$

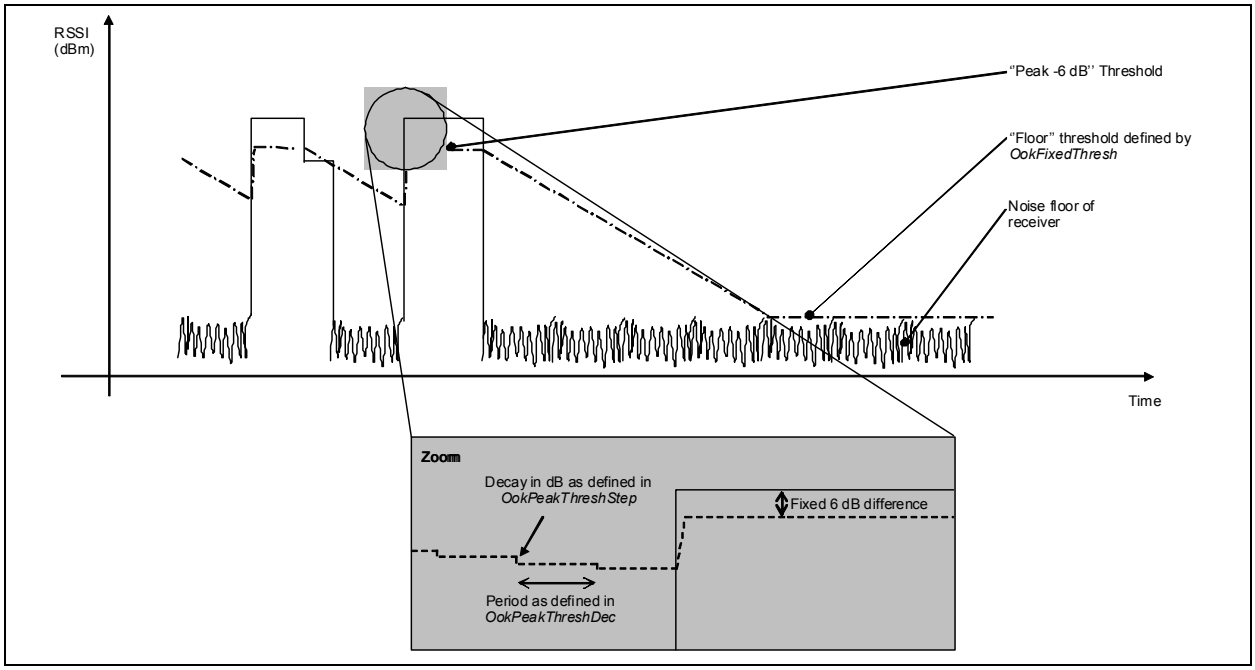
The output of the FSK demodulator can be fed to the bit synchronizer as described in **Section 2.4.14 "Bit Synchronizer"** to provide the companion processor with a synchronous data stream in Continuous mode.

2.4.12 OOK DEMODULATOR

The OOK demodulator performs a comparison of the RSSI output and a threshold value. Three different threshold modes are available, configured through bits OokThreshType in RegOokPeak.

The recommended mode of operation is the Peak Threshold mode as illustrated in Figure 2-6.

FIGURE 2-6: OOK PEAK DEMODULATOR DESCRIPTION



In Peak Threshold mode the comparison threshold level is the peak value of the RSSI, reduced by 6 dB. In the absence of an input signal or during the reception of a logical '0', the acquired peak value is decremented by one OokPeakThreshStep every OokPeakThreshDec period.

When the RSSI output is null for a long time (for instance after a long string of '0' received, or if no transmitter is present), the peak threshold level continues to fall until it reaches the Floor Threshold, programmed in OokFixedThresh.

The default settings of the OOK demodulator lead to the performance stated in the electrical specification. However, in applications in which sudden signal drops are awaited during a reception, the three parameters must be optimized accordingly.

2.4.13 OPTIMIZING THE FLOOR THRESHOLD

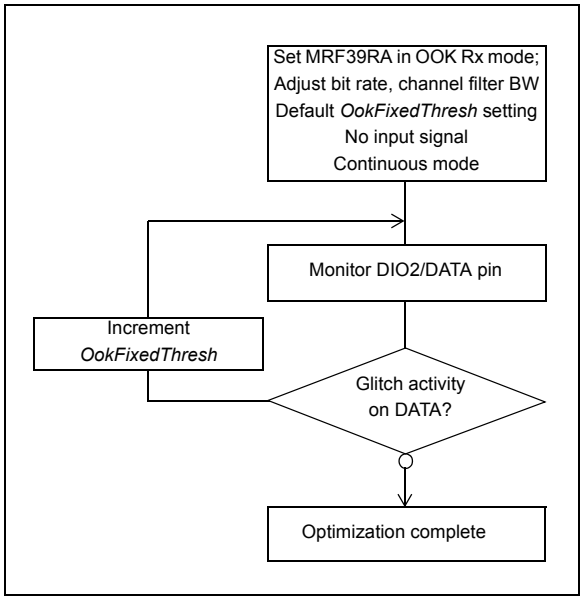
OokFixedThresh determines the sensitivity of the OOK receiver as it sets the comparison threshold for weak input signals (i.e., those close to the noise floor). Significant sensitivity improvements can be generated if configured correctly.

Note that the noise floor of the receiver at the demodulator input depends on:

- The noise figure of the receiver
- The gain of the receive chain from antenna to base band
- The matching, including SAW filter (if any)
- The bandwidth of the channel filters.

It is important to note that OokFixedThresh setting is application-dependent. The following procedure as illustrated in Figure 2-7 is recommended to optimize OokFixedThresh.

FIGURE 2-7: FLOOR THRESHOLD OPTIMIZATION



The new floor threshold value found during this test must be used for OOK reception with those receiver settings.

2.4.13.1 Optimizing OOK Demodulator for Fast Fading Signals

A sudden drop in signal strength can cause the bit error rate to increase. For applications where the expected signal drop can be estimated, the OokPeakThreshStep and OokPeakThreshDec parameters can be optimized for a given number of threshold decrements per bit. Refer to RegOokPeak to access those settings.

2.4.13.2 Alternative OOK Demodulator Threshold Modes

In addition to the Peak OOK Threshold mode, the user can alternatively select two other types of threshold detectors:

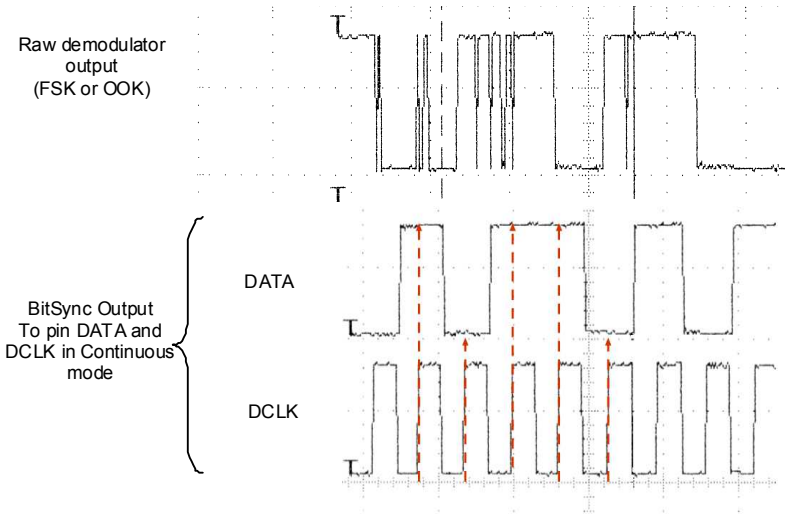
- **Fixed Threshold**: the value is selected through OokFixedThresh
- **Average Threshold**: data supplied by the RSSI block is averaged and this operation mode must be used only with DC-free encoded data.

2.4.14 BIT SYNCHRONIZER

The bit synchronizer is a block that provides a clean and synchronized digital output, free of glitches. Its output is made available on pin DIO1/DCLK in Continuous mode and can be disabled through register settings. However, for optimum receiver performance it is used when running Continuous mode is strongly advised.

The bit synchronizer is automatically activated in Packet mode. Its bit rate is controlled by BitRateMsb and BitRateLsb in RegBitrate.

FIGURE 2-8: BIT SYNCHRONIZER DESCRIPTION



To ensure correct operation of the bit synchronizer, the following conditions must be satisfied:

- A preamble (0x55 or 0xAA) of at least 12 bits is required for synchronization; the longer the synchronization, the better the packet success rate
- The subsequent payload bit stream must have at least one transition from '0' to '1' or '1' to '0' every 16 bits during data transmission
- The bit rate matching between the transmitter and the receiver must be better than 6.5%.

2.4.15 FREQUENCY ERROR INDICATOR (FEI)

This function provides information about the frequency error of the local oscillator (LO) compared with the carrier frequency of a modulated signal at the input of the receiver. When the FEI block is launched, the frequency error is measured and the signed result is loaded in FeiValue in RegFei, in two's complement format. The time required for an FEI evaluation is four times the bit period.

To ensure a proper behavior of the FEI:

- The operation must be done during the reception of preamble
- The sum of the frequency offset and the 20 dB signal bandwidth must be lower than the base band filter bandwidth.

The 20 dB bandwidth of the signal (double-side bandwidth) can be evaluated as shown in Equation 2-8.

EQUATION 2-8: 20 DB BANDWIDTH

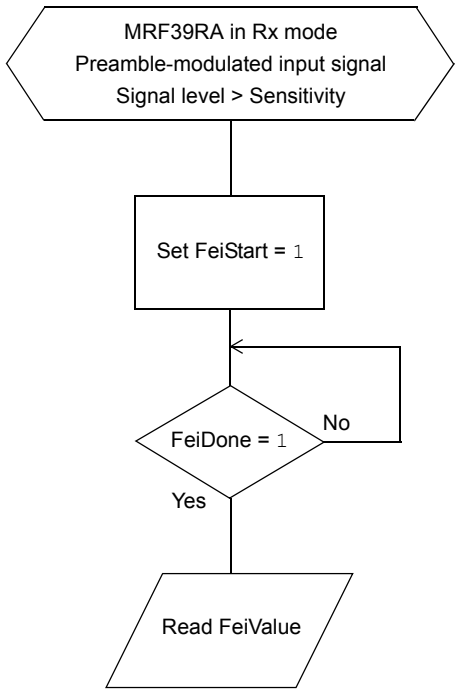
$$BW_{20dB} = 2 \times \left(F_{DEV} + \frac{BR}{2} \right)$$

The frequency error, in Hz, can be calculated with the formula in Equation 2-9.

EQUATION 2-9: FREQUENCY ERROR-HZ

$$FEI = F_{STEP} \times FeiValue$$

FIGURE 2-9: FEI PROCESS



2.4.16 AUTOMATIC FREQUENCY CORRECTION

The AFC is based on the FEI block and, therefore, the same input signal and receiver setting conditions apply. When the AFC procedure is done, AfcValue is directly subtracted to the register that defines the frequency of operation of the chip, FRF. The AFC can be launched in the following cases:

- Each time the receiver is enabled, if AfcAutoOn = 1
- Upon user request, by setting bit AfcStart in RegAfcFei, if AfcAutoOn = 0

When the AFC is automatically triggered (AfcAutoOn = 1), the user has the option to:

- Clear the former AFC correction value, if AfcAutoClearOn = 1
- Start the AFC evaluation from the previously corrected frequency. This may be useful in systems in which the LO keeps on drifting in the same direction. Aging compensation is a good example.

The MRF39RA offers an alternate receiver bandwidth setting during the AFC phase to accommodate large LO drifts. If the user considers that the received signal may be out of the receiver bandwidth, a higher channel filter bandwidth can be programmed in RegAfcBw, at the expense of the receiver noise floor, which produces impact upon sensitivity.

2.4.17 OPTIMIZED SETUP FOR LOW MODULATION INDEX SYSTEMS

For wide band systems, where AFC is usually not required (XTAL inaccuracies do not typically impact the sensitivity), it is recommended to offset the LO frequency of the receiver to avoid desensitization. This can be simply done by modifying Frf in RegFrfLsb. A good rule of thumb is to offset the receiver's LO by 10% of the expected transmitter frequency deviation.

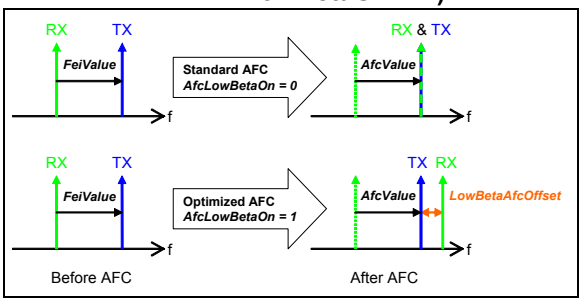
For narrow band systems, it is recommended to perform AFC. The MRF39RA has a dedicated AFC, enabled when AfcLowBetaOn in RegAfcCtrl is set to '1'. A frequency offset, programmable through LowBetaAfcOffset in RegTestAfc, is added and is calculated as shown in Equation 2-10.

EQUATION 2-10: FREQUENCY OFFSET

$$Offset = LowBetaAFCOffset \times 488\ Hz$$

The user must ensure that the programmed offset exceeds the DC canceler's cutoff frequency, set through DccFreqAfc in RegAfcBw.

FIGURE 2-10: OPTIMIZED AFC (Afc LowBetaOn = 1)



As shown in Figure 2-10, a standard AFC sequence uses the result of the FEI to correct the LO frequency and align both local oscillators. When the optimized AFC is enabled (AfcLowBetaOn = 1), the receiver's LO is corrected by FeiValue + LowBetaAfcOffset.

When the optimized AFC routine is enabled, the receiver start-up time can be computed as shown in Equation 2-11, see **Section 3.2.1 "Receiver Start-up Time"**.

EQUATION 2-11: RECEIVER START-UP TIME

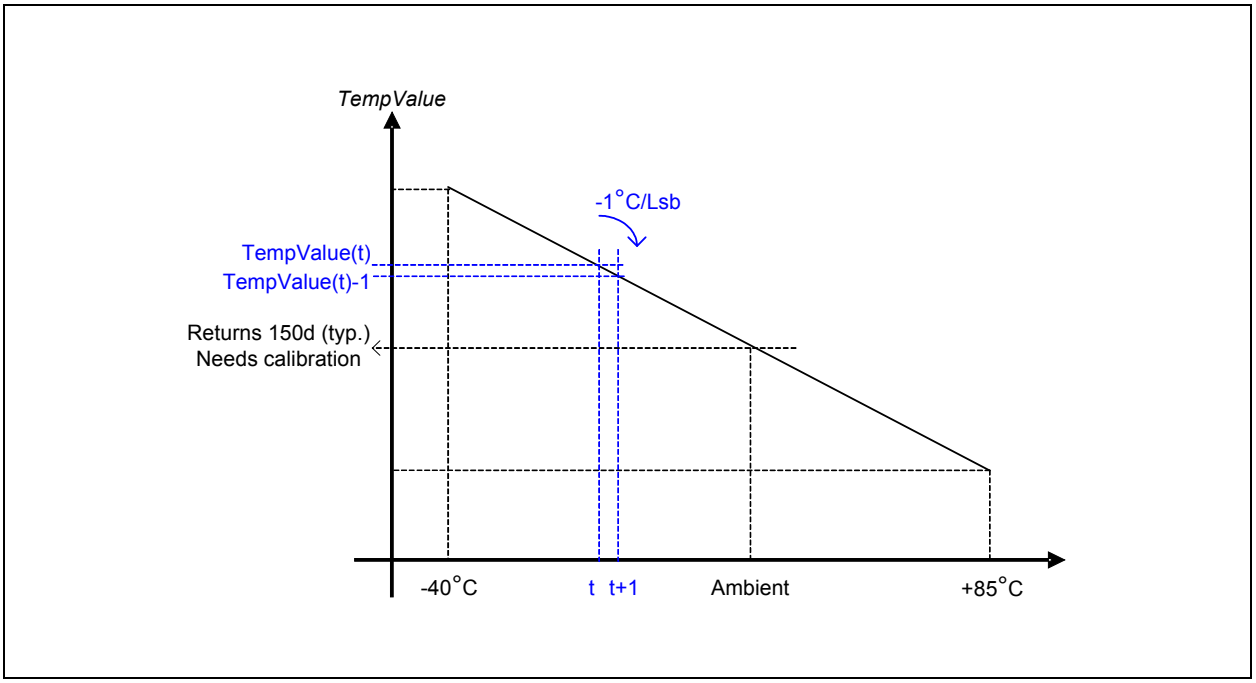
$$TS\_RE\_AGC\&AFC\ (optimized\ AFC) =$$
$$= T_{ANA} + 4.T_{CF} + 4.T_{DCC} + 3.T_{RSSI} + 2.T_{AFC} + 2.T_{PLLAFC}$$

2.4.18 TEMPERATURE SENSOR

When temperature is measured, the receiver ADC is used to digitize the sensor response. Most receiver blocks are disabled, and temperature measurement can only be triggered in Standby or Frequency Synthesizer modes.

As shown in Figure 2-11, the response of the temperature sensor is -1°C/Lsb. A CMOS temperature sensor is not accurate by nature; therefore, it must be calibrated at ambient temperature for precise temperature readings.

FIGURE 2-11: TEMPERATURE SENSOR RESPONSE



It takes less than 100 microseconds for the MRF39RA to evaluate the temperature from setting TempMeasStart to '1' to TempMeasRunning Reset.

2.4.19 TIME-OUT FUNCTION

The MRF39RA includes a time-out function, which enables it to automatically shut down the receiver after a receive sequence and, therefore, save energy.

- Time-out interrupt is generated, TimeoutRxStart x 16 x Tbit, after switching to RX mode if RssiThreshold flag does not raise within this time frame.
- Time-out interrupt is generated, TimeoutRssiThresh x 16 x Tbit, after RssiThreshold flag is raised.

Use Time-out interrupt to warn the companion processor to shut down the receiver and return to a lower power mode.

3.0 OPERATING MODES

3.1 Basic Modes

The circuit is set in four different basic modes as described in Table 3-1.

By default when switching from one mode to another, the sub-blocks wakes up according to a pre-defined and optimized sequence. Alternatively, these operating modes can be selected directly by disabling the automatic sequencer (SequencerOff in RegOpMode = 1).

TABLE 3-1: BASIC RECEIVER MODES

ListenOn in *RegOpMode*	Mode in *RegOpMode*	Selected mode	Enabled blocks
0	0 0 0	Sleep mode	None
0	0 0 1	Stand-by mode	Top regulator and crystal oscillator
0	0 1 0	FS mode	Frequency synthesizer
0	1 0 0	Receive mode	Frequency synthesizer and receiver
1	x	Listen mode	See **Section 3.3 "Listen Mode"**

3.2 Automatic Sequencer and Wake-up Times

By default when switching from one operating mode to another, the circuit takes care of the sequence of events in a manner that the transition timing is optimized. For example, when switching from Sleep mode to Receive mode, the MRF39RA first goes to Standby mode (XO started), then to Frequency Synthesizer mode, and finally, when the PLL has locked, to Receive mode.

The crystal oscillator wake-up time, TS_OSC, is directly related to the time for the crystal oscillator to reach its steady state. This depends notably on the crystal characteristics.

The frequency synthesizer wake-up time, TS_FS, is directly related to the time needed by the PLL to reach its steady state. The PLL_LOCK signal, provided on an external pin, gives an indication of the lock status. It goes high when the PLL reaches its locking range.

Three specific cases can be highlighted:

- Receiver wake-up time from Sleep mode = TS_OSC + TS_FS + TS_RE
- Receiver wake-up time from Sleep mode, AGC enabled = TS_OSC + TS_FS + TS_RE_AGC
- Receiver wake-up time from Sleep mode, AGC and AFC enabled = TS_OSC + TS_FS + TS_RE_AGC&AFC.

These timings are detailed in **Section 3.2.1 "Receiver Start-up Time"**.

In applications where the target average power consumption, or the target start-up time do not require setting the MRF39RA in the lowest power modes (Sleep or Standby), the respective TS_OSC and TS_FS timings in the equations above can be omitted.

3.2.1 RECEIVER START-UP TIME

It is highly recommended to use the built-in sequencer of the MRF39RA to optimize the delays when setting the chip in Receive mode. It ensures the shortest start-up times, hence the lowest possible energy usage for battery-operated systems.

The start-up times of the receiver can be calculated as shown in Figure 3-1 through Figure 3-3.

FIGURE 3-1: Rx START-UP – NO AGC, NO AFC

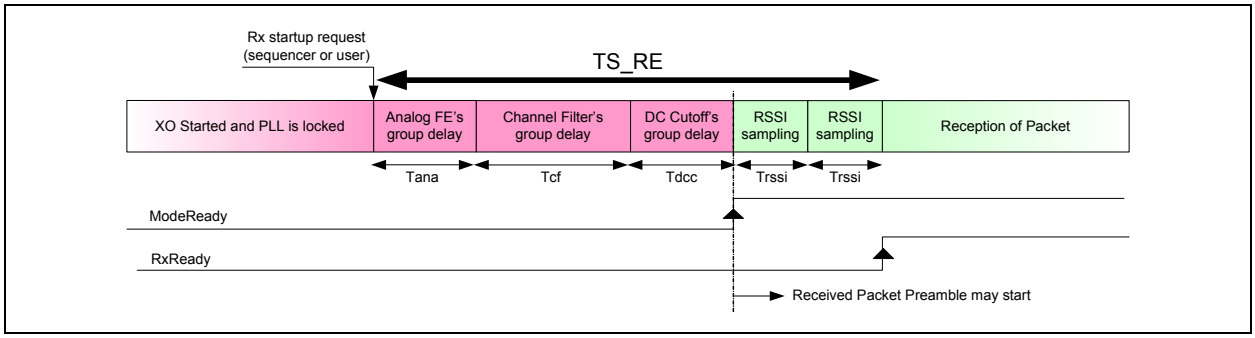


FIGURE 3-2: Rx START-UP – AGC, NO AFC

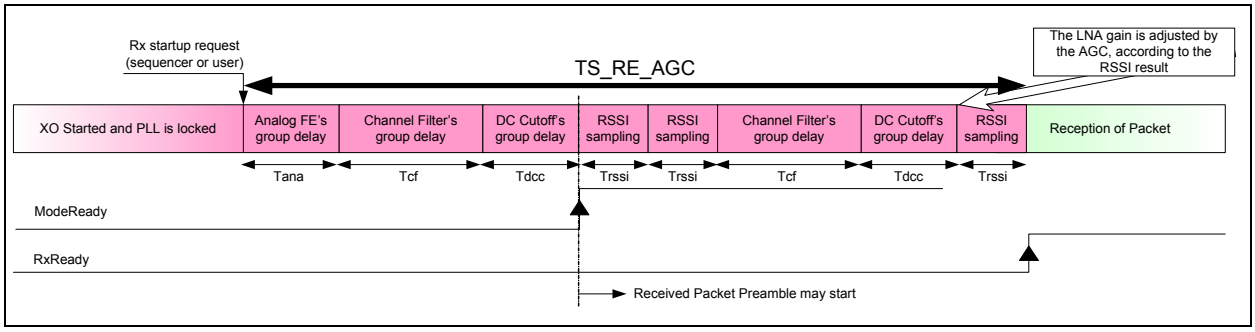
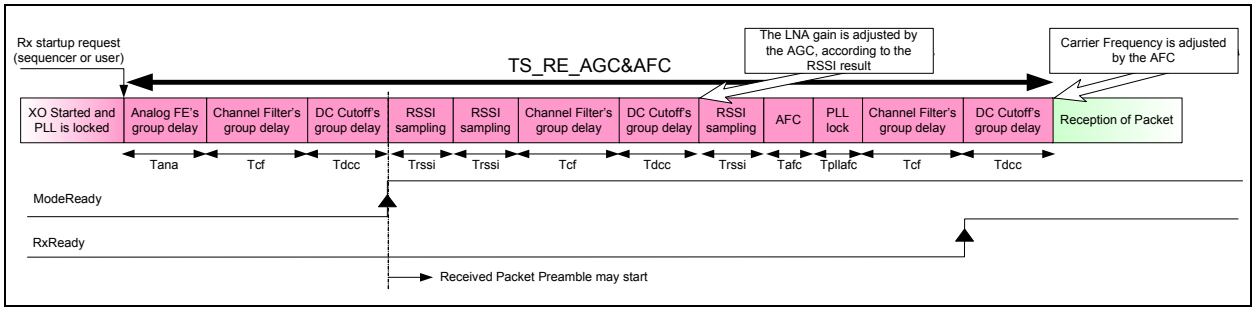


FIGURE 3-3: Rx START-UP – AGC AND AFC



The different timings shown above are as follows:

- Group delay of the analog front end: Tana = 20 µs
- Channel filter's group delay in FSK mode: Tcf = 21/(4.RxBw)
- Channel filter's group delay in OOK mode: Tcf = 34/(4.RxBw)
- DC Cutoff's group delay: Tdcc = max(8, 2^(round(log2(8.RxBw.Tbit)+1))/(4.RxBw)
- PLL lock time after AFC adjustment: Tpllafc = 5/ PLLBW (PLLBW = 300 kHz)
- AFC sample time: Tafc = 4 x Tbit (also denoted TS_AFC in the general specification)
- RSSI sample time: Trssi = 2 x int(4.RxBw.Tbit)/ (4.RxBw) (also known as TS_RSSI).

Note: The timings represent maximum settling times. Shorter settling times may be observed in real cases.

3.2.2 Rx Start Procedure

As described in the previous sections, the RxReady interrupt warns the uC that the receiver is ready.

- In Continuous mode with bit synchronizer, the receiver starts locking its bit synchronizer on a minimum or 12 bits of received preamble before the reception of correct data or sync word (if enabled) can occur. See **Section 2.4.14 "Bit Synchronizer"** for details.
- In Continuous mode without bit synchronizer, valid data is available on DIO2/DATA right after the RxReady interrupt.
- In Packet mode, the receiver starts locking its bit synchronizer on a minimum or 12 bits of received preamble before the reception of correct data or sync word (if enabled) can occur. See **Section 2.4.14 "Bit Synchronizer"** for details.

3.2.3 Optimized Frequency Hopping Sequences

In a frequency hopping-like application, it is required to turn off the receiver when hopping from one channel to another, to optimize the hopping sequence:

Receiver hop from Ch A to Ch B:

1. MRF39RA is in Rx mode in Ch A
2. Change the carrier frequency in the RegFrf registers
3. Program the MRF39RA in FS mode
4. Turn the receiver back to Rx mode
5. Respect the Rx start procedure, described in **Section 3.2.2 "Rx Start Procedure"**.

Note:	The sequence assumes that the sequencer is turned on (SequencerOff = 0 in RegOpMode).

3.3 Listen Mode

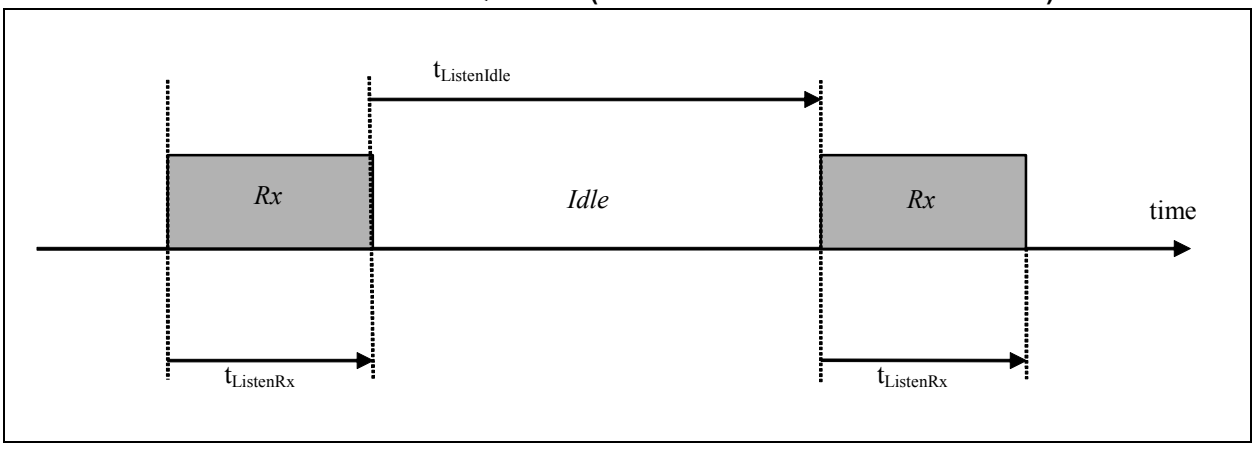
To set the circuit to Listen mode, ListenOn in RegOpMode must be set to '1' while in Standby mode. In this mode, MRF39RA spends most of the time in Idle mode, during which only the RC oscillator runs. Periodically the receiver wakes up and listens for an RF signal. If a wanted signal is detected, the receiver is kept on and the data is demodulated.

Otherwise, if a wanted signal is not detected after a predefined period of time, the receiver is disabled until the next time period.

This periodical Rx wake-up requirement is very common in low-power applications. On MRF39RA, it is locally handled by the Listen mode block without using uC resources or energy.

The simplified timing diagram of this procedure is illustrated in Figure 3-4.

FIGURE 3-4: LISTEN MODE SEQUENCE (NO WANTED SIGNAL IS RECEIVED)



3.3.1 Timings

The duration of the idle phase is given by $t_{ListenIdle}$. The time during which the receiver is on and is waiting for a signal is given by $t_{ListenRx}$. The $t_{ListenRx}$ includes the wake-up time of the receiver as described in **Section 3.2.1 "Receiver Start-up Time"**. This duration is programmed in the Configuration registers via the serial interface.

Both time periods $t_{ListenRx}$ and $t_{ListenIdle}$ (denoted $t_{ListenX}$ in the text below) are fixed by two parameters from the Configuration register and are calculated as follows:

EQUATION 3-1: TIME PERIODS

$$t_{ListenX} = ListenCoefX \bullet ListenResolX$$

Where:

ListenResolX is the Rx or idle resolution and is independently programmable on three values (64 µs, 4.1 ms or 262 ms), whereas ListenCoefX is an integer between 1 and 255. All parameters are located in RegListen registers.

The timing ranges are tabulated in Table 3-2.

TABLE 3-2: RANGE OF DURATIONS IN LISTEN MODE

ListenResolX	Min duration (ListenCoef = 1)	Max duration (ListenCoef = 255)
01	64 µs	16 ms
10	4.1 ms	1.04s
11	0.26s	67s

Note 1: The accuracy of the typical timings given in Table 3-2 depends on the RC oscillator calibration.

2: RC oscillator calibration is required and must be performed at power-up. See **Section 3.3.5 "RC Timer Accuracy"** for details.

3.3.2 Criteria

The criteria taken for detecting a wanted signal and hence deciding to maintain the receiver on is defined by ListenCriteria in RegListen1.

TABLE 3-3: SIGNAL ACCEPTANCE CRITERIA IN LISTEN MODE

ListenCriteria	Input Signal Power ≥ *RssiThreshold*	*SyncAddressMatch*
0	Required	Not Required
1	Required	Required

3.3.3 End of Cycle Actions

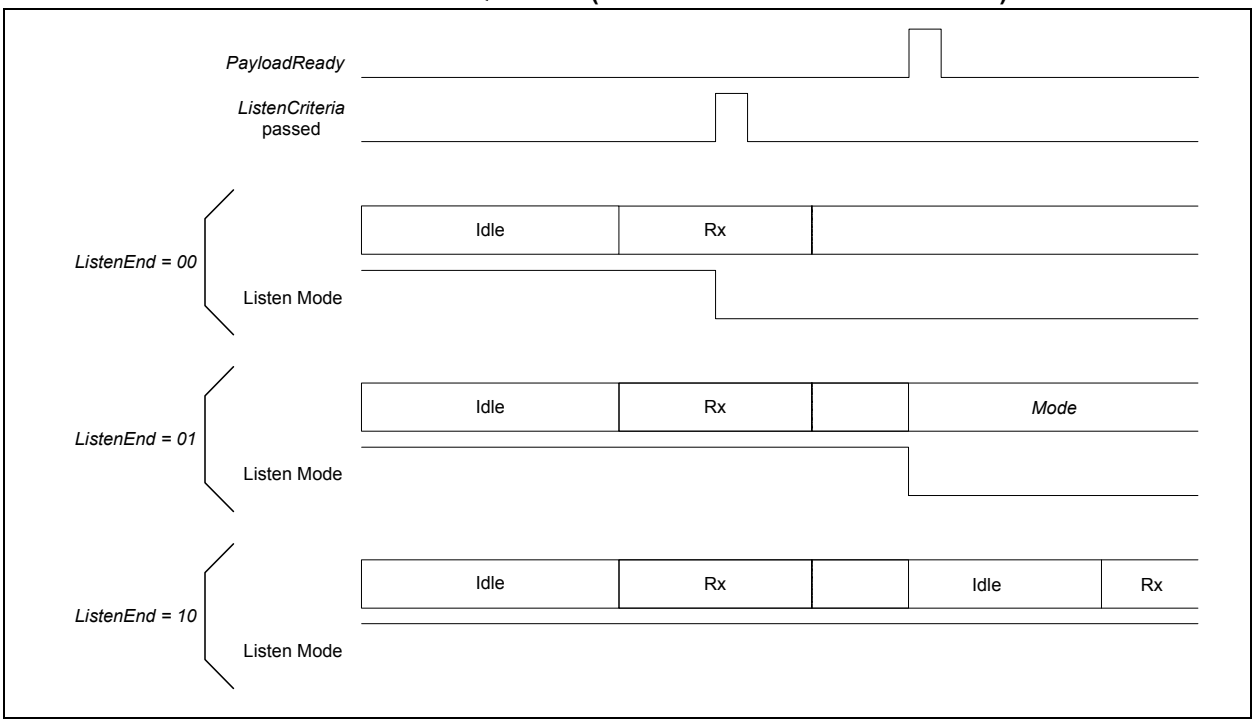
The action taken after detection of a packet is defined by ListenEnd in RegListen3 as described in Table 3-4.

TABLE 3-4: END OF LISTEN CYCLE ACTION

ListenEnd	Description
00	Chip stays in Rx mode. Listen mode stops and must be disabled.
01	Chip stays in Rx mode until *PayloadReady* or *Time-out* interrupt occurs. It then goes to the mode defined by *Mode*. Listen mode stops and must be disabled.
10	Chip stays in Rx mode until *PayloadReady* or *Time-out* interrupt occurs. Listen mode then resumes in Idle state. FIFO content is lost at next Rx wake-up.

Upon detection of a valid packet, the sequencing is altered as shown in Figure 3-5.

FIGURE 3-5: LISTEN MODE SEQUENCE (WANTED SIGNAL IS RECEIVED)



Listen mode can be disabled by writing ListenOn to '0'.

3.3.4 Stopping Listen Mode

To abort Listen mode operation, observe the following procedure:

- Program RegOpMode with ListenOn = 0, ListenAbort = 1 and the desired setting for the Mode bits (Sleep, Stdby, FS, Rx or Tx mode) in a single SPI access
- Program RegOpMode with ListenOn = 0, ListenAbort = 0 and the desired setting for the Mode bits (Sleep, Stdby, FS, Rx or Tx mode) in a second SPI access.

3.3.5 RC Timer Accuracy

All timings of the Listen mode rely on the accuracy of the internal low-power RC oscillator. This oscillator is automatically calibrated at the device power-up. This is a user-transparent process.

For applications enduring large temperature variations and for which the power supply is never removed, RC calibration can be performed on user request. RcCalStart in RegOsc1 is used to trigger this calibration and the flag RcCalDone automatically sets when the calibration is over.

3.4 Auto Modes

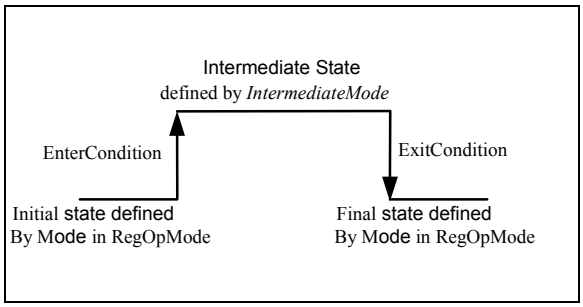
Automatic modes of packet handler can be enabled by configuring the related parameters in RegAutoModes.

The Intermediate mode of the chip is called *IntermediateMode* and the Enter and Exit conditions to and from this Intermediate mode can be configured through the parameters EnterCondition and ExitCondition.

The Enter and Exit conditions cannot be used independently of each other (i.e., both must be enabled at the same time).

The initial and the final state is the one configured in the mode in RegOpMode. The initial and final states can be different by configuring the Modes register while the chip is in Intermediate mode. The pictorial description of the AutoModes is shown in Figure 3-6.

FIGURE 3-6: AUTO MODES OF PACKET HANDLER



Some typical examples of AutoModes usage are described below:

- Automatic reception (AutoRx):
  - Mode = Rx
  - IntermediateMode = Sleep
  - EnterCondition = CrcOk
  - ExitCondition = falling edge of FifoNotEmpty