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MRF49XA
Data Sheet

ISM Band Sub-GHz
RF Transceiver

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MRF49XA

ISM Band Sub-GHz RF Transceiver

Features

- Fully Integrated Sub-GHz Transceiver
- Supports Proprietary Sub-GHz Wireless Protocols
- 4-Wire Serial Peripheral Interface (SPI) Compatible Interface
- CMOS/TTL Compatible I/Os
- Clock and Reset Signals for Microcontroller
- Integrated 10 MHz Oscillator Circuitry
- Integrated Low Battery Voltage Detector
- Supports Power-Saving modes
- Operating Voltage: 2.2V–3.8V
- Low-Current Consumption, Typically:
  - 11 mA in RX mode
  - 15 mA in TX mode
  - 0.3 µA in Sleep mode
- Industrial Temperature Range
- 16-Pin TSSOP Package

RF/Analog Features

- Supports ISM Band Sub-GHz Frequency Ranges (433 MHz, 868 MHz and 915 MHz)
- Modulation Technique: FSK with Frequency Hopping Spread Spectrum (FHSS) Capability
- Supports High Data Rates:
  - Digital mode 115.2 kbps, max.
  - Analog mode 256 kbps, max.
- Differential RF Input/Output:
  - -110 dBm Typical Sensitivity with 0 dBm Maximum Input Level
  - +7 dBm Typical Transmit Output Power
- High-Resolution Programmable Phase-Locked Loop (PLL) Synthesizer
- Integrated Power Amplifier
- Integrated Low Phase Noise Voltage Controlled Oscillator (VCO) Frequency
- Synthesizer and PLL Loop Filter
- Automatic Frequency Control (AFC)

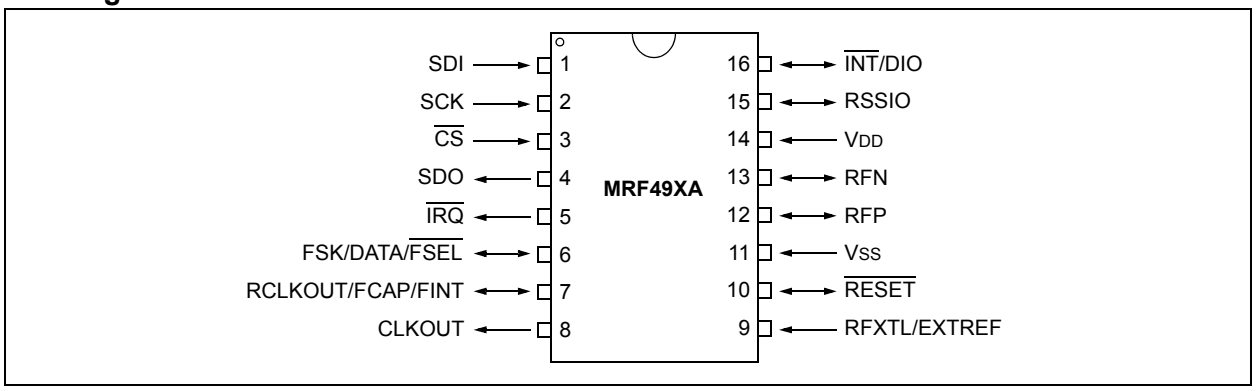
Baseband Features

- Supports Programmable TX Frequency Deviation and RX Baseband Bandwidth (BBBW)
- Analog and Digital RSSI Outputs with Dynamic Range
- RX Synchronous Pattern Recognition
- 16-Bit RX Data FIFO
- Two 8-Bit TX Data Registers
- Low-Power Duty Cycle mode
- Advanced Adjacent Channel Rejection/Blocking Capability
- Internal Data and Clock Recovery
- Supports Data Filtering
- Data Quality Indicator (DQI)

Typical Applications

- Home/Industrial Automation
- Remote Control
- Wireless PC Peripherals
- Remote Keyless Entry
- Vehicle Sensor Monitoring
- Telemetry
- Data Logging Systems
- Remote Automatic Meter Reading
- Security Systems for Home/Industrial Environment
- Automobile Immobilizers
- Sports and Performance Monitoring
- Wireless Toy Controls
- Medical Applications

Pin Diagram: 16-Pin TSSOP



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NOTES:

1.0 INTRODUCTION

Microchip's MRF49XA is a fully integrated Sub-GHz RF transceiver. This low-power single chip Frequency Shift Keying (FSK) baseband transceiver supports:

- Zero-IF architecture
- Multi-channel and multi-band
- Synthesizer with PLL
- Power Amplifier (PA)
- Low Noise Amplifier (LNA)
- I/Q down converter mixers
- I/Q demodulator
- Baseband filters (BBFs) and amplifiers

The simplified functional block diagram of MRF49XA is shown in Figure 1-1. The MRF49XA is an ideal choice for low-cost, high-volume, low data rate (<256 kbps), two-way and short range wireless applications. This transceiver can be used in the unlicensed 433 MHz, 868 MHz and 915 MHz frequency bands, and for applications looking for FCC, IC or ETSI certification in the ISM band.

The MRF49XA has a low phase noise and provides an excellent adjacent channel interference, Bit Error Rate (BER) and larger communication coverage along with higher output power. The MRF49XA device's AFC feature allows for the use of a low-accuracy, low-cost crystal. In order to minimize the total system cost, a communication link in most of the applications can be created using a low-cost, generic 10 MHz crystal, a bypass filter and an affordable microcontroller. The MRF49XA provides a clock signal for the microcontroller and avoids the need for a second crystal on the circuit board. The transceiver can be interfaced with many popular Microchip PIC® microcontrollers through a 4-wire SPI, interrupt ($\overline{IRO}$) and Reset. The interface between the microcontroller and MRF49XA is shown in Figure 1-2.

The MRF49XA supports the following digital data processing features:

- PLL and I/Q VCO with Calibration
- Receiver Signal Strength Indicator
- Data Quality Indicator
- AFC
- Baseband Power Amplifier
- TX and RX Buffers

The receiver's Baseband Bandwidth (BBBW) can be programmed to accommodate various deviations, data rates and crystal tolerance requirements.

The high-resolution PLL allows:

- The usage of multiple channels in any of the bands
- The rapid settling time allows for faster frequency hopping, bypassing multipath fading and interference to achieve robust wireless links

The transceiver is integrated with different Sleep modes and an internal wake-up timer to reduce the overall current consumption, and to extend the battery life. The device's small size with low-power consumption makes it ideal for various short range radio applications.

FIGURE 1-1: FUNCTIONAL NODE BLOCK DIAGRAM

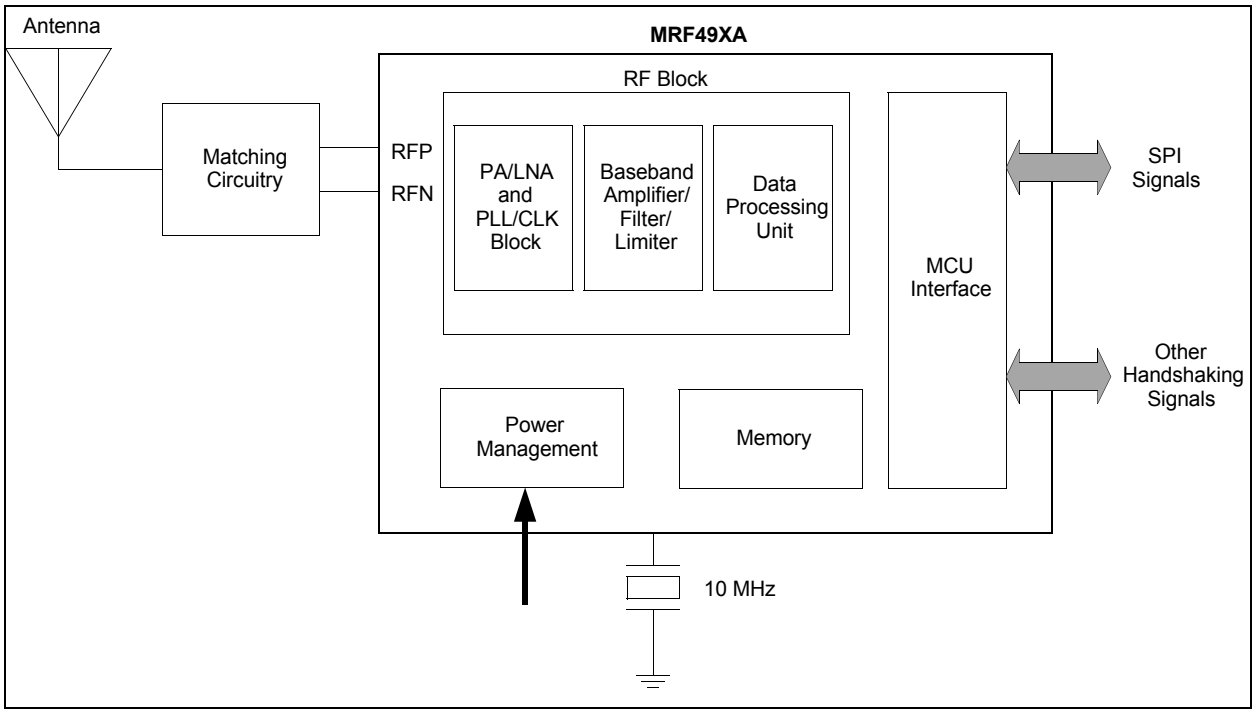
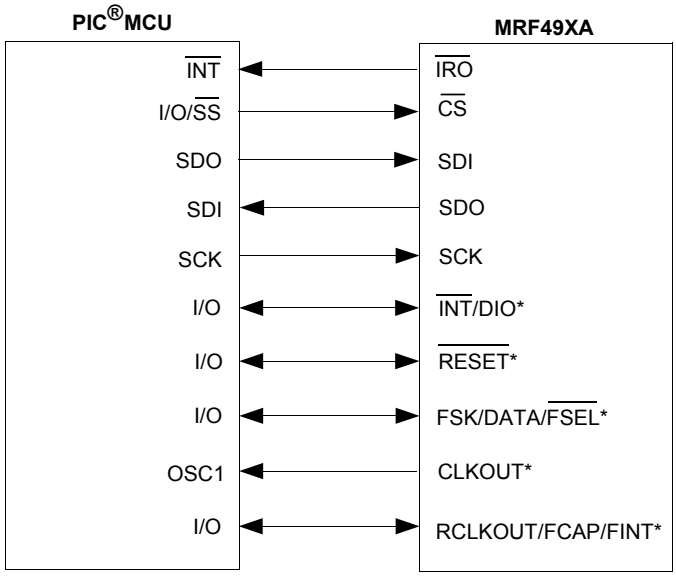


FIGURE 1-2: MICROCONTROLLER TO MRF49XA INTERFACE



* Implies optional signals.

2.0 HARDWARE DESCRIPTION

The MRF49XA is an integrated, single chip ISM Band Sub-GHz Transceiver. A simplified architectural block diagram of the MRF49XA is shown in Figure 2-1.

The frequency synthesizer is clocked by an external 10 MHz crystal and generates the 433, 868 and 915 MHz radio frequency. The receiver with a Zero-IF architecture consists of the following components:

- LNA
- Down Conversion Mixers
- Channel Filters
- Baseband Limiting Amplifiers
- Receiver Signal Strength Indicator

The transmitter with a direct conversion architecture has a typical output power of +7 dBm. An internal transmit/receive switch combines the transmitter and receiver circuits into differential RFP and RFN pins. These pins are connected to the impedance matching circuitry (Balun) and to the external antenna connected to the device.

The device operates in the low-voltage range of 2.2V–3.8V, and in Sleep mode, it operates at a very low-current state, typically 0.3 µA.

The quality of the data is checked or validated using the RSSI and DQI blocks built into the transceiver. Data is buffered in transmitter registers and receiver FIFOs. The AFC feature allows the use of a low-accuracy and low-cost crystal. The CLKOUT is used to clock the external controller. The transceiver is controlled through a 4-wire SPI, interrupt (INT/DIO and IRO), FSK/DATA/FSEL, RCLKOUT/FCAP/FINT and RESET pins. See Table 2-1 for pin details.

The MRF49XA supports the following feature blocks:

- Clock Generation
- Data Filtering and Amplification
- Data Pattern Recognition and Timing
- Data Processing and Storage
- Independent Transmit and Receiver FIFO Buffers
- Registers

These features reduce the processing load, and hence, allows the use of low-cost 8-bit microcontrollers for data processing.

FIGURE 2-1: MRF49XA ARCHITECTURAL BLOCK DIAGRAM

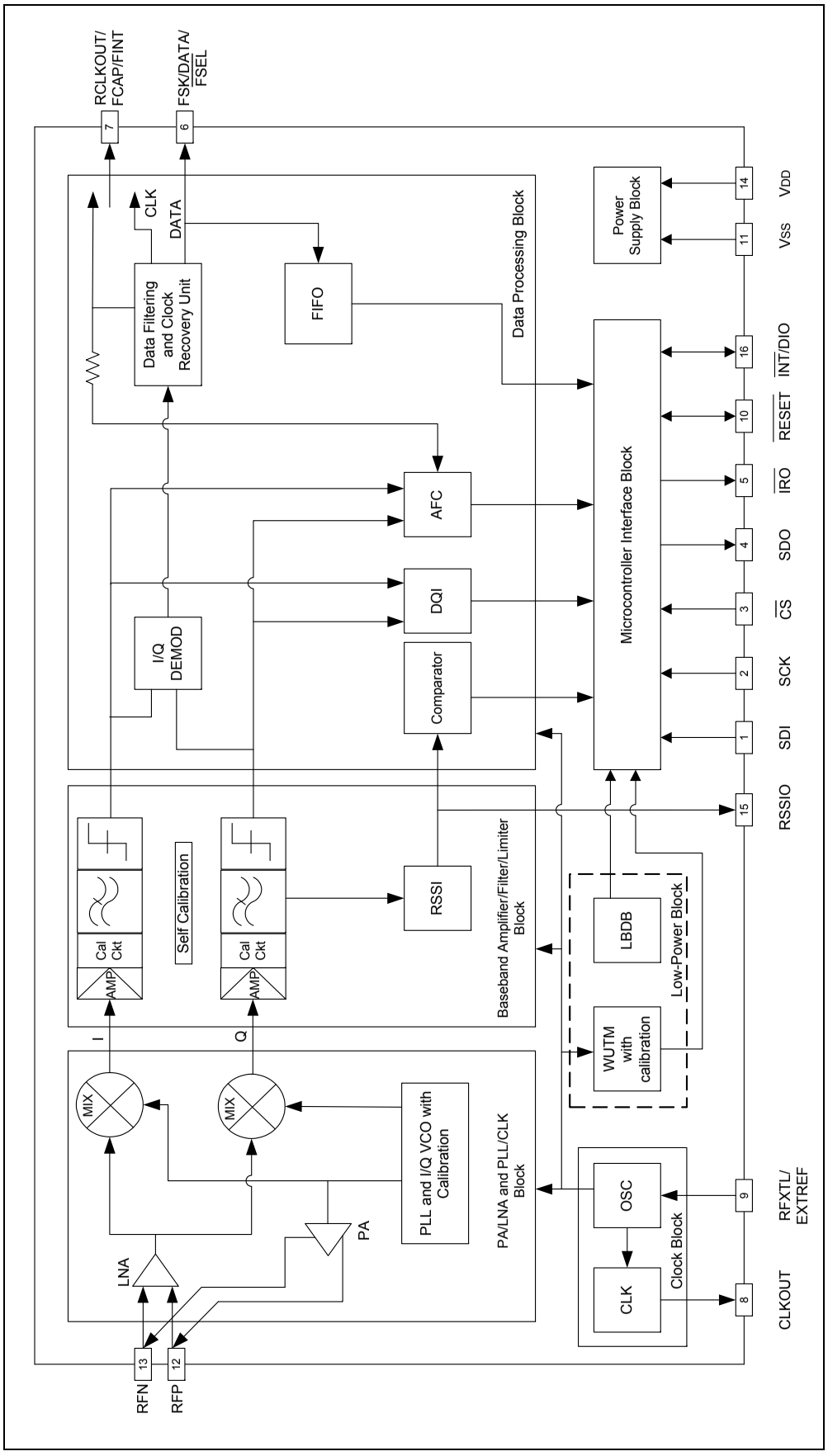


TABLE 2-1: PIN DESCRIPTION

Pin	Symbol	Type	Description
1	SDI	Digital Input	Serial data input interface to MRF49XA (SPI input signal).
2	SCK	Digital Input	Serial clock interface (SPI clock).
3	$\overline{CS}$	Digital Input	Serial interface chip select (SPI chip/device select).
4	SDO	Digital Output	Serial data output interface from MRF49XA (SPI output signal).
5	$\overline{IRO}$	Digital Output	**Interrupt Request Output:** Receiver generates an active-low interrupt request for the microcontroller on the following events: • The TXBREG (see Table 2-4) is ready to receive the next byte. • The RXFIFOREG (see Table 2-4) has received the preprogrammed amount of bits. • RXFIFOREG overflow/TXBREG underrun. • Negative pulse on interrupt input pin ($\overline{INT}$). • Wake-up timer time-out. • Supply voltage below the preprogrammed value is detected. • Power-on Reset (POR).
6	FSK/DATA/$\overline{FSEL}$	Digital Input/Output	**Frequency Shift Keying:** Transmit FSK data input (with internal pull-up resistor of 133 kΩ). **Data:** When configured as DATA, this pin functions as follows: • Data In: Manually modulates the data from the external host microcontroller when the internal TXBREG is disabled. If the TXBREG is enabled, this pin can be tied “high” or left unconnected. When reading the internal RXFIFOREG, this pin must be pulled “low”. • Data Out: Receives data in conjunction with RCLKOUT when the internal FIFO is not used. **FIFO Select:** Selects the FIFO and the first bit appears on the next clock when reading the RXFIFOREG. The $\overline{FSEL}$ pin has an internal pull-up resistor. This pin must be “high” when the TX register is enabled. In order to achieve minimum current consumption, keep this pin “high” in Sleep mode.
7	RCLKOUT/FCAP/ FINT	Digital Input/Output	**Recovery Clock Output:** Provides the clock recovered from the incoming data if: • FTYPE bit of BBFCREG (see Table 2-10) is configured as digital filter and • FIFO is disabled by configuring FIFOEN bit of GENCREG (see Table 2-10) **Filter Capacitor:** This pin is a raw baseband data if the FTYPE bit of BBFCREG is configured as a configuration filter. The pin can be used by the host microcontroller for data recovery. **FIFO Interrupt:** When the internal FIFO, FIFOEN bit of GENCREG is enabled, this pin acts as a FIFO full interrupt, indicating that the FIFO has been filled to its preprogrammed limit (see FFBC<3:0> bits in FIFORSTREG in Table 2-10).
8	CLKOUT	Digital Output	**Clock Output:** The transceiver’s clock output can be used by the host microcontroller as a clock source. Refer Register 2 for more details.

TABLE 2-1: PIN DESCRIPTION (CONTINUED)

Pin	Symbol	Type	Description
9	RFXTL/EXTREF	Analog Input	**RF Crystal:** This pin is connected to a 10 MHz series crystal or to an external oscillator reference. The crystal is used as a reference for the PLL which generates the local oscillator frequency. It is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. **External Reference Input:** An external reference input, such as an oscillator, can be connected as a reference source. Connect the oscillator through a 0.01 µF capacitor.
10	$\overline{\text{RESET}}$	Digital Input/Output	Active-low hardware pin. This pin has an open-drain Reset output with internal pull-up and input buffer. Refer to Section 3.1, Reset for more details.
11	Vss	Ground	Ground reference.
12	RFP	RF Input/Output	Differential RF input/output (+).
13	RFN	RF Input/Output	Differential RF input/output (-).
14	VDD	Power	RF power supply. Bypass with a capacitor close to the pin. See Section 2.1, Power and Ground Pins for more details.
15	RSSIO	Analog Input/Output	**Received Signal Strength Indicator Output:** The analog RSSI output is used to determine the signal strength. The response and settling time depends on the external filter capacitor. Typically, a 4-10 nF capacitor provides optimum response time for most applications.
16	$\overline{\text{INT}}$/DIO	Digital Input/Output	**Interrupt:** This pin can be configured as an active-low external interrupt to the device. If a logic ‘0’ is applied to this pin, it causes the $\overline{\text{IRO}}$ pin to toggle, signaling an interrupt to the external microcontroller. The source of interrupt can be determined by reading the first four bits of STSREG (see Table 2-4). This pin can be used to wake-up the device from Sleep. **Data Indicator Output:** This pin can be configured to indicate valid data based on the actual internal settings.

2.1 Power and Ground Pins

The power supply bypassing is very essential for better handling of signal surges and noise in the power line. The large value decoupling capacitors should be placed at the PCB power input. The smaller value decoupling capacitors should be placed at every power point of the device and at bias points for the RF port. Poor bypassing leads to conducted interference which can cause noise and spurious signals to couple into the RF sections, thereby significantly reducing the performance.

The VDD pin requires two bypass capacitors to ensure sufficient bypass and decoupling. However, based on the selected carrier frequency, the bypass capacitor values vary. The recommended bypass capacitor values are listed in Table 2-2 and the type of capacitor to be used is listed in Table 2-3. The bypass capacitors are connected to pin 14, as shown in Figure 4-1. The trace length (VDD pin to bypass capacitors) should be made as short as possible.

TABLE 2-2: RECOMMENDED BYPASS CAPACITORS VALUE

Band (MHz)	C1(µF)	C2 (nF)	C3 (pF)
433	2.2	10	220
868	2.2	10	47
915	2.2	10	33

TABLE 2-3: RECOMMENDED BYPASS CAPACITORS

Property	C1	C2	C3
SMD Size	A	0603	0603
Dielectric	Tantalum	Ceramic	Ceramic

2.2 $\overline{\text{RESET}}$ Pin

An external hardware Reset of MRF49XA can be performed by asserting the $\overline{\text{RESET}}$ (pin 10) to low. After releasing the pin, it takes slightly more than 0.25 ms for the transceiver to be released from the Reset. The pin is driven with an open-drain output, and hence, it is pulled down while the device is in POR. The $\overline{\text{RESET}}$ pin has an internal, weak, on-chip, pull-up resistor. The device will not accept commands during the Reset period.

The device enters the Reset mode if any of the following events take place:

- Power-on Reset
- Power Glitch Reset
- Software Reset
- $\overline{\text{RESET}}$ Pin

Software Reset can be issued by sending the appropriate control command to the device. The result of the command is similar to POR, but the duration of the Reset event is much less, typically 0.25 ms. The Software Reset works only when the Sensitive Reset mode is selected. See Section 3.1, Reset for details on Reset; for connection details, see Figure 4-1.

2.3 Power Amplifier

The PA has an open-collector differential output and can directly drive different PCB antennas, like loop or dipole, with a programmable output power level during signal transmission. However, certain types of antennas, like monopole, need an additional matching circuitry. A built-in, automatic antenna tuning circuit is used to avoid the manual tuning and trimming procedures during production process; the so called “hand effect”.

2.4 Low Noise Amplifier

The LNA has approximately 250Ω of differential input impedance which functions well with the proposed antenna (PCB/Monopole) during signal transmission. The LNA, when connected to the 50Ω device, needs an external matching circuit (Balun) for correct matching and to minimize the noise figure of the receiver.

The LNA gain can be selected in four steps for different gain factors (between 0 dB and -20 dB relative to the highest gain) based on the required RF signal strength. This gain selection feature is useful in a noisy environment.

2.5 RFXTL/EXTREF and CLKOUT Pins

The MRF49XA has an internal, integrated crystal oscillator circuit, and therefore, a single RFXTL/EXTREF pin is used as a crystal oscillator. The crystal oscillator circuit, with internal loading capacitors, provides a 10 MHz reference signal for the PLL. The PLL, in turn, generates the local oscillator frequency. It is possible to "pull" the crystal to the accurate frequency by changing the load capacitor value. This reduces the external component count and simplifies the design. The crystal load capacitor is programmable from 8.5 pF–16 pF in 0.5 pF steps. Thus, the crystal oscillator circuit can accept a wide range of crystals from different manufacturers with different load capacitance requirements. The ability to vary the load capacitance also helps in fine tuning the final carrier frequency as the crystal itself is the PLL reference for the carrier. An external reference input, such as an oscillator, can be connected as a reference source. The oscillator can be connected through a 0.01 µF capacitor. Choosing better crystal results in a lesser TX to RX frequency offset and smaller deviation in BBBW. Hence, the recommended crystal accuracy should be ≤40 ppm. Deviation and BBBW are discussed in detail in Section 2.8, Baseband/Data Filters. The guidelines for selecting the appropriate crystal are explained in Section 3.6, Crystal Selection Guidelines.

The transceiver can provide a clock signal through the Clock Output (CLKOUT) pin to the microcontroller for accurate timing, and thus, eliminating the need for a second crystal. This also results in reducing the component count.

2.6 Phase-Locked Loop

The PLL circuitry determines the operating frequency of the device. This programmable PLL synthesizer requires only a single 10 MHz crystal reference source. The PLL maintains accuracy using the on-chip crystal controlled reference oscillator and provides maximum flexibility in performance to the designers. It is possible to change the crystal to the accurate frequency by changing the load capacitor value. The RF stability can be controlled by selecting a crystal with specifications which satisfy the application and by providing the functions required to generate the carriers, and by tuning each of the bands. For more details, see Section 3.6, Crystal Selection Guidelines. The PLL's high resolution allows the use of multiple channels in any of the bands. The on-chip PLL is able to perform manual and automatic calibration to compensate for the changes in temperature or operating voltage.

2.7 Automatic Frequency Control

The PLL in MRF49XA is capable of performing automatic fine adjustment for the carrier frequency by using an integrated AFC feature. The receiver uses the AFC feature to minimize the frequency offset between the TX/RX signals in discrete steps, which gives the advantage of:

- Narrower receiver bandwidth for increased sensitivity can be achieved
- Higher data rates can be achieved
- Usability of any locally available, low-accuracy and inexpensive crystals can be used

The MRF49XA can be programmed to automatically control the frequency or can be manually activated by a strobe signal.

2.8 Baseband/Data Filters

The BBFs are user-programmable. The receiver bandwidth can be set by programming the bandwidth of the BBFs. The receiver, when programmed, is set up according to the characteristics of the signal to be received. The baseband receiver has several programming options to optimize the communication for a variety of applications. The programmable functions are as follows:

- Baseband Analog Filter
- Baseband Digital Filter
- Receive Bandwidth
- Receive Data Rate
- Clock Recovery

The output data filtering can be performed using either an external capacitor or a digital filter based on the user application. The RCLKOUT/FCAP/FINT pin in MRF49XA provides the raw baseband data if configured as a configuration filter. It can be used by the host microcontroller to perform the data recovery.

2.9 Clock Recovery Circuit

The Clock Recovery Circuit (CLKRC) is used to render a synchronized clock source to recover the data using an external microcontroller. The CLKRC works by sampling the preamble on the received data. The preamble contains a sequence of 1 and 0 for the CLKRC to properly extract the data timing. In Slow mode, the CLKRC requires more sampling (12–16 bits), and hence, has a longer settling time before locking. In Fast mode, it uses less samples (6–8 bits) before locking, and thereby, the settling time is short which makes timing accuracy less critical. The RCLKOUT/FCAP/FINT pin provides the clock recovered from the incoming data if the baseband filter is configured as a digital filter.

2.10 Data Validity Blocks

2.10.1 RECEIVE SIGNAL STRENGTH INDICATOR

The MRF49XA provides the RSSI signal to the host microcontroller, and hence, supports the monitoring of analog and digital signal strengths. A digital RSSI output is provided to monitor the input signal level through an internal STATUS register. The digital RSSI goes high, if the received signal strength exceeds a given preprogrammed RSSI threshold level. The digital RSSI can be monitored by reading the STSREG. Alternatively, an analog RSSI signal is also available at pin 15 (RSSIO) to determine the signal strength. The analog RSSI settling time depends on the external filter capacitor. Typically, a 4–10 nF capacitor provides optimum response time for most of the applications. See Section 4.0, Application Details and Section 5.0, Electrical Characteristics for details on filter capacitors for analog RSSI. The typical relationship between analog RSSI voltage and RF input power is graphically represented in Figure 2-2.

2.10.2 DATA QUALITY INDICATOR

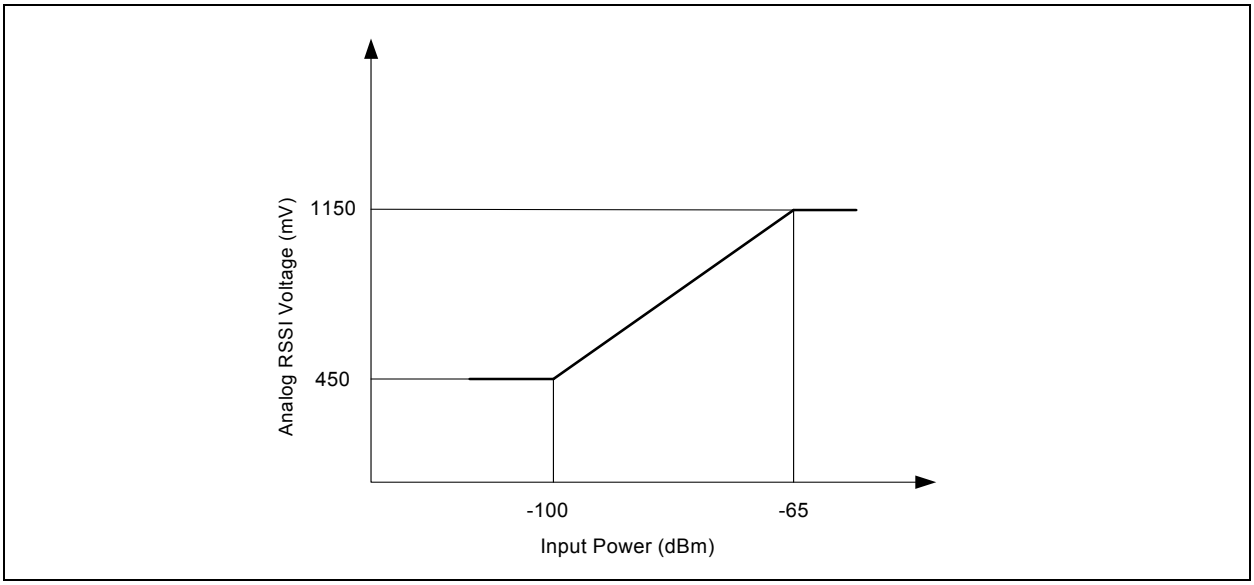
The Data Quality Indicator (DQI) is a special function which indicates the quality of the received signal and the link. The unfiltered received data is sampled and the number of spikes are counted in the received data for a specified time. If the input signals are of high value, it indicates the operating FSK transmitter of the high output signal within the baseband filter bandwidth from the local oscillator.

2.10.3 DATA INDICATOR OUTPUT

The Data Indicator Output (DIO) is an extension of DQI. The DIO pin can be configured to indicate valid data based on the actual internal settings. When an incoming signal is detected, the DIO uses the DQI clock recovery lock and digital RSSI signals to determine the validity of the incoming signal. The DIO searches for the valid data transitions at an expected data rate. The desired data rate and the acceptance criteria for valid data are user-programmable through the SPI port. The DIO signal is valid when using the internal receive FIFO or an external pin to capture baseband data.

The DIO has three modes of operation: Slow, Medium and Fast. Each mode is dependent on the type of signals it uses to determine the valid data and the number of incoming preamble bits present at the beginning of the packet. The DIO can be multiplexed with the $\overline{INT}$ pin for external usage.

FIGURE 2-2: ANALOG RSSI VOLTAGE vs. RF INPUT POWER



2.11 Power-Saving Blocks

2.11.1 LOW BATTERY VOLTAGE DETECTOR

The integrated low-battery voltage detector circuit monitors the supply voltage against a preprogrammed value and generates an interrupt on the $\overline{IRO}$ pin if it falls below the programmed threshold level. The detector circuit has a built-in 50 mV hysteresis.

2.11.2 WAKE-UP TIMER

The current consumption of the programmable wake-up timer is very low, typically 1.5 µA. It is programmable from 1 ms to several days with an accuracy level of ±10%. The calibration of the wake-up timer takes place at every start-up and every 30s thereafter, and is referenced with the crystal oscillator. The calibration is performed even in Sleep mode. The calibration process for the wake-up timer takes around 500 µs, and for proper calibration, the crystal oscillator must be running before the wake-up timer is enabled.

If any wake-up event occurs, including the wake-up timer, the wake-up logic generates an interrupt signal on the $\overline{IRO}$ pin which can be used to wake-up the microcontroller and this reduces the period that the microcontroller needs to be active. If the oscillator circuit is disabled, the calibration circuit turns it on for a brief period to perform the calibration in order to maintain accurate timing before returning to Sleep.

2.11.3 LOW DUTY CYCLE MODE

The MRF49XA can be made to enter into a Low Duty Cycle mode operation to decrease the average power consumption in Receive mode. The Low Duty Cycle mode is normally used in conjunction with the wake-up timer for its operation. The DCSREG may be configured so that when the wake-up timer brings the device out of Sleep mode, the receiver is turned on for a short time to sample for a signal. Then, the device returns to Sleep and this process repeats.

2.12 $\overline{INT}$, $\overline{IRO}$ Pins and Interrupts

The Interrupt pin ($\overline{INT}$) can be configured as an active-low external interrupt to MRF49XA which is provided from the host microcontroller.

The device generates an interrupt request for the host microcontroller by pulling the $\overline{IRO}$ pin low if the following events occur:

- TX register is ready to receive the next byte
- RX FIFO has received the preprogrammed amount of bits
- FIFO overflow/TX register underrun (TXUROW overflow in Receive mode and underrun in Transmit mode)
- Negative pulse on interrupt input pin, $\overline{INT}$
- Wake-up timer time-out
- Supply voltage below the preprogrammed value is detected
- Power-on Reset

The Status bits should be read out to identify the source of interrupt. The interrupts are cleared by reading the STATUS register.

See Section 3.9, Interrupts for functional description of interrupts.

2.13 Transmit Register

The Transmit register in MRF49XA is configured as two, 8-bit shift registers connected in series to form a single 16-bit shift register. When the transmitter is enabled, it starts sending out data from the first register with respect to the set bit rate. After power-up and with the Transmit registers enabled, the transmitter preloads the TX latch with 0xAAAA. This can be used to generate a preamble before sending actual data.

In hardware, the FSK/DATA/$\overline{FSEL}$ has two functions:

- As Frequency Shift Keying pin, it basically takes care of transmitting the FSK data input. The pin has an internal pull-up resistor of 133 kΩ. This pin must be “high” when the TX register is enabled to take care of the transmission.
- As DATA (Data Out), this pin receives the data in conjunction with RCLKOUT when the internal FIFO is not used. When reading the internal RXFIFOREG, this pin must be pulled “low”.

2.14 Receive FIFO

The received data in MRF49XA is filled into a 16-bit First In First Out (FIFO) register. The FIFO is configured to generate an interrupt after receiving a defined number of bits. When the internal FIFO is enabled, the FIFO interrupt pin (RCLKOUT/FCAP/FINT) acts as a FIFO full interrupt, indicating that the FIFO has been filled to its preprogrammed limit. The receiver starts filling FIFO with data when it identifies the synchronous pattern through the synchronous pattern recognition circuit. During this process, the FINTDIO bit changes its state. The FIFO interrupt level is programmable from 1 to 16 bits. It is recommended to set the threshold to at least half the length of the register (8 bits) to ensure that the external host microcontroller has time to set up. The synchronous pattern recognition circuit prevents the FIFO from being filled up with noise, and hence, avoids overloading the external host microcontroller.

Note:	The synchronous word is not accessible in the RX FIFO. The SYNBREG provides this information to the host microcontroller.

The FIFO read clock (SCK) must be < $f_{XTAL}/4$ or < 2.5 MHz for 10 MHz on RFXTAL. The FSK/DATA/$\overline{FSEL}$ as the FIFO select pin, selects the FIFO and the first bit appears on the next clock when reading the RXFIFOREG.

In hardware, the FSK/DATA/$\overline{FSEL}$ pin is configured as DATA (Data In) and with internal TXBREG disabled; this manually modulates the data from the external host microcontroller. If the TXBREG is enabled, this pin can be tied “high” or can be left unconnected.

The internal synchronous pattern and the pattern length are user-programmable. If the Chip Select ($\overline{CS}$) pin is low, the data bits on the SDI pin are shifted into the device on the rising edge of the clock on the SCK pin.The serial interface is initialized if the $\overline{CS}$ signal is high.

2.15 Serial Peripheral Interface

The MRF49XA communicates with the host microcontroller through a 4-wire SPI port as a slave device. An SPI compatible serial interface lets the user select, command and monitor the status of the MRF49XA through the host microcontroller. All registers consist of a command code, followed by a varying number of parameter or data bits. As the device uses word writes, the $\overline{CS}$ pin should be pulled low for 16 bits. Data bits on the SDI pin are shifted into the device upon the rising edge of the clock on the SCK pin whenever the $\overline{CS}$ pin is low.

The maximum clock frequency for the SPI bus is 20 MHz. The MRF49XA supports SPI mode 0,0 which requires the SCK to remain Idle in a low state. The $\overline{CS}$ pin must be held low to enable communication between the host microcontroller and the MRF49XA. The device’s timing specification details are given in Table 5-8. Data is received by the transceiver through the SDI pin and is clocked on the rising edge of SCK. The timing diagram is shown in Figure 5-1. MRF49XA sends out the data through the SDO pin and is clocked out on the falling edge of SCK. The Most Significant bit (MSb) is sent first (e.g., bit 15 for a 16-bit command) in any data. The POR circuit sets default values in all control and command registers.

Note:	Special care must be taken when the microcontroller’s built-in hardware serial port is used. If the port cannot be switched to a 16-bit mode, then a separate I/O line should be used to control the $\overline{CS}$ pin to ensure a low level during the complete duration of the communication (command) or a software serial control interface should be implemented.

The SDO pin defaults to a low state when the $\overline{CS}$ pin is high (the MRF49XA is not selected). This pin has a tri-state buffer and uses a bus hold logic. For the SPI interface, see Figure 4-1.

The following parameters can be programmed and set through SPI:

- Frequency band
- Center frequency of the synthesizer
- Division ratio for the microcontroller clock
- Wake-up timer period
- Bandwidth of the baseband signal path
- Low supply voltage detector threshold

Any of these auxiliary functions can be disabled when not required. After power-on, all parameters are set to default values. The programmed values are retained during Sleep mode. The interface supports the read out of a status register which provides detailed information about the status of the transceiver and the received data.

Note:	To test the SPI interface lines, set the LBD (Low Battery Detector) threshold below the actual V_{DD} and the device must generate an interrupt.

2.16 Memory Organization

The memory in MRF49XA is implemented as static RAM and is accessible through the SPI port. Each memory location functionally addresses a register, control, status or data/FIFO fields, as shown in Table 2-10. The command/control registers provide control, status and device address for transceiver operations. The FIFOs serve as temporary buffers for data transmission and reception.

The commands to the device are sent serially. All 17 commands basically address the 17 registers affiliated to it. The registers consist of a command code, followed by control, data, status or parameter bits. The MSb is sent first in all of the commands (e.g., bit 15 for a 16-bit command). The POR circuit sets the default values in all control and command registers.

In general, MRF49XA registers are read only. Hence the chip status can only be read by the Status Read Register. During write, only appropriate byte is written to the desired register. It is not desired to read/write all registers and there is no way to read back the register.

TABLE 2-4: CONTROL (COMMAND) REGISTER DESCRIPTION

Sl. No.	Register Name	Register Description	Related Control Functions
1	STSREG	Status Read Register	Receive register/FIFO, transmit register, interrupt, frequency control and signal strength, POR, wake-up timer, low battery detect, data quality, clock recovery
2	GENCREG	General Configuration Register	Frequency band select, enables TX and RX registers, crystal load capacitor bank value
3	AFCCREG	AFC Configuration Register	AFC locking range, mode, accuracy and enable
4	TXCREG	Transmit Configuration Register	Modulation polarity, modulation bandwidth, transmit power and deviation
5	TXBREG	Transmit Byte Register	Transmit data byte
6	CFSREG	Center Frequency Value Set Register	Transmit or receive frequency
7	RXCREG	Receive Control Register	Function of pin 16, DIO mode, RX BBBW, LNA gain, digital RSSI threshold
8	BBFCREG	Baseband Filter Configuration Register	Clock Recovery mode, data indicator parameter value and filter type
9	RXFIFOREG	Receiver FIFO Read Register	Receive data byte
10	FIFORSTREG	FIFO and Reset mode Configuration Register	FIFO interrupt level, FIFO start control and FIFO enable, POR Sensitivity mode, synchronous character length
11	SYNBREG	Synchronous Byte Configuration Register	Synchronous character pattern
12	DRSREG	Data Rate Value Set Register	Data rate prescalar set
13	PMCREG	Power Management Configuration Register	Enables receive and transmit chain, baseband circuit, synthesizer circuit, oscillator, wake-up timer, low battery detect and clock out
14	WTSREG	Wake-up Timer Value Set Register	Wake-up timer values for time interval
15	DCSREG	Duty Cycle Value Set Register	Duty Cycle mode and value
16	BCSREG	Battery Threshold Detect and Clock Output Value Set Register	Low battery detect threshold values and clock output frequency
17	PLLCREG	PLL Configuration Register	Clock out buffer speed, PLL bandwidth, dithering and delay

2.17 Control (Command) Register Details

REGISTER 2-1: STSREG: STATUS READ REGISTER (POR: 0x0000)(1)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TXRXFIFO	POR	TXOWRXOF	WUTINT	LCEXINT	LBTD	FIFOEM	ATRSSI
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DQDO	CLKRL	AFCCT	OFFSV	OFFSB<3:0>			
bit 7							bit 0

Legend:	r = reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TXRXFIFO:** Transmit Register or Receive FIFO bit

Transmit mode: Transmit Register Ready bit(2)

Indicates whether the transmit register is ready to receive the next byte for transmission.

1 = Ready(5)

0 = Not ready

Receive mode: Receive FIFO Fill (Interrupt) bit(2,3)

Indicates whether the RX FIFO has reached the preprogrammed limit.

1 = Reached the preprogrammed limit(5)

0 = Programming limit has not been reached

bit 14 **POR:** Power-on Reset bit

1 = POR has occurred(5)

0 = POR has not occured

bit 13 **TXOWRXOF:** Transmit Overwrite Receive Overflow bit

Transmit mode: Transmit Register Underrun or Overwrite bit

1 = Underrun or overwrite(5)

0 = Operating normally

Receive mode: Receive FIFO Overflow bit

1 = FIFO overflow(5)

0 = Operating normally

bit 12 **WUTINT:** Wake-up Timer (Interrupt) Overflow bit

1 = Timer overflow has occurred(5)

0 = Operating normally

bit 11 **LCEXINT:** Logic Change on External Interrupt bit

Indicates a high-to-low logic level change on external interrupt pin ($\overline{INT}$/DIO)(5).

1 = High-to-low transition has occurred

0 = High-to-low transition has not occured

Note 1: All register commands begin with logic '1' and only the STATUS register read command begins with logic '0'.

2: This bit is multiplexed for Transmit or Receive mode.

3: See the FFBC bits (FIFORSTREG<3:0>) in Register 2-10.

4: To get accurate values, the AFC should be disabled during the read by clearing the FOFEN bit (AFCCREG<0>). The AFC offset value (OFFSB bits in the status word) is represented as a two's complement number. The actual frequency offset can be calculated as the AFC offset value multiplied by the current PLL frequency step from CFSREG (FREQB<11:0>).

5: This bit is cleared after STSREG is read.

REGISTER 2-1: STSREG: STATUS READ REGISTER (POR: 0x0000)(1) (CONTINUED)

bit 10 **LBTD:** Low Battery Threshold Detect bit
Indicates whether the battery or supply voltage is below the preprogrammed threshold limit.
1 = Supply voltage is below threshold
0 = Normal supply voltage feed

bit 9 **FIFOEM:** FIFO Empty bit
Indicates whether the receive FIFO is empty or filled.
1 = FIFO is empty
0 = FIFO is filled

bit 8 **ATRSSI:** Antenna Tuning and Received Signal Strength Indicator bit
Transmit mode:
The bit indicates that the antenna tuning circuit has detected a strong RF signal.
1 = Strong RF signal present
0 = Weak or absence of RF signal
Receive mode:
The bit indicates that the incoming RF signal is above the preprogrammed digital RSSI limit.
1 = RF signal is above the threshold value set
0 = RF signal is less than the threshold value set

bit 7 **DQDO:** Data Quality Detect/Indicate Output bit
Indicates good data quality output.
1 = Quality data is detected
0 = Quality data is unavailable

bit 6 **CLKRL:** Clock Recovery Lock bit
Indicates clock recovery is locked.
1 = Clock recovery locked
0 = Clock recovery unlocked

bit 5 **AFCCT:** Automatic Frequency Control Cycle Toggle bit
For each AFC cycle run, this bit toggles between logic '1' and logic '0'.
1 = AFC cycle has occurred
0 = No AFC in this cycle

bit 4 **OFFSV:** Offset Sign Value bit
Indicates the measured difference or frequency offset of any AFC cycle (sign of the offset value).
1 = Higher than the chip frequency
0 = Lower than the chip frequency

bit 3-0 **OFFSB<3:0>:** Offset bits
The offset value to be added to the frequency control parameter (internal PLL)(4).
1 = Result is negative
0 = Result is positive

Note 1: All register commands begin with logic '1' and only the STATUS register read command begins with logic '0'.
2: This bit is multiplexed for Transmit or Receive mode.
3: See the FFBC bits (FIFORSTREG<3:0>) in Register 2-10.
4: To get accurate values, the AFC should be disabled during the read by clearing the FOFEN bit (AFCCREG<0>). The AFC offset value (OFFSB bits in the status word) is represented as a two's complement number. The actual frequency offset can be calculated as the AFC offset value multiplied by the current PLL frequency step from CFSREG (FREQB<11:0>).
5: This bit is cleared after STSREG is read.

Note: See **Appendix A: "Read Sequence and Packet Structures"** for the STSREG read sequence.

REGISTER 2-2: GENCREG: GENERAL CONFIGURATION REGISTER (POR: 0x8008)

W-1	W-0	W-0	W-0	W-0	W-0	W-0	W-0
CCB<15:8>							
bit 15							bit 8

W-0	W-0	W-0	W-0	W-1	W-0	W-0	W-0
TXDEN	FIFOEN	FBS<1:0>		LCS<3:0>			
bit 7							bit 0

Legend:	r = reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **CCB<15:8>:** Command Code bits
The command code bits (10000000b) are serially sent to the microcontroller to identify the bits to be written in the GENCREG.

bit 7 **TXDEN:** TX Data Register Enable bit
1 = Internal TX Data register enabled**(1)**
0 = Internal TX Data register disabled; no transmit

bit 6 **FIFOEN:** FIFO Enable bit
1 = Internal data FIFO enabled; the FIFO is used to store data during receive**(2)**
0 = FIFO disabled; FSK/DATA/$\overline{\text{FSEL}}$ and RCLKOUT/FCAP/FINT are used to receive data

bit 5-4 **FBS<1:0>:** Frequency Band Select bits
These bits set the frequency band to be used in Sub-GHz range.
11 = 915 MHz
10 = 868 MHz
01 = 433 MHz
00 = Reserved

bit 3-0 **LCS<3:0>:** Load Capacitance Select bits
These bits set and vary the internal load capacitance for the crystal reference.
1111 = 16.0 pF
1110 = 15.5 pF
1101 = 15.0 pF
1100 = 14.5 pF
1011 = 14.0 pF
1010 = 13.5 pF
1001 = 13.0 pF
1000 = 12.5 pF
0111 = 12.0 pF
0110 = 11.5 pF
0101 = 11.0 pF
0100 = 10.5 pF
0011 = 10.0 pF
0010 = 9.5 pF
0001 = 9.0 pF
0000 = 8.5 pF

Note 1: If the internal TX data register is used, the DATA/FSK/$\overline{\text{FSEL}}$ pin must be pulled "high".
2: If the data FIFO is used, the DATA/FSK/$\overline{\text{FSEL}}$ pin must be pulled "low".

REGISTER 2-3: AFCCREG: AUTOMATIC FREQUENCY CONTROL CONFIGURATION REGISTER (POR: 0xC4F7)

W-1	W-1	W-0	W-0	W-0	W-1	W-0	W-0
CCB<15:8>							
bit 15							bit 8

W-1	W-1	W-1	W-1	W-0	W-1	W-1	W-1
AUTOMS<1:0>		ARFO<1:0>		MFCS	HAM	FOREN	FOFEN
bit 7							bit 0

Legend:	r = reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **CCB<15:8>:** Command Code bits

The command code bits (11000100b) are serially sent to the microcontroller to identify the bits to be written in the AFCCREG.

bit 7-6 **AUTOMS<1:0>:** Automatic mode Selection bits (for AFC)

These bits select the operation type (automatic/manual) for performing AFC based on the status of the MFCS bit.
11 = Keeps offset independent for the state of the DIO signal
10 = Keeps offset only while receiving (DIO = High)
01 = Runs and measures only once after each power-up cycle
00 = Auto mode off (controlled by microcontroller)

bit 5-4 **ARFO<1:0>:** Allowable Range for Frequency Offset bits

These bits select the offset range allowable between transmitter and receiver frequencies.
11 = +3 FRES to -4 FRES(1)
10 = +7 FRES to -8 FRES
01 = +15 FRES to -16 FRES
00 = No restriction

bit 3 **MFCS:** Manual Frequency Control Strobe bit

This bit is the strobe signal which initiates the manual frequency control sample to calculate the offset error.
1 = A sample of a received signal is compared with a receiver Local Oscillator (LO) signal and an offset error is calculated. If bit 1 is enabled, the value is stored in the Offset register of the AFC block.(2)
0 = Ready for the next sample

bit 2 **HAM:** High-Accuracy (Fine) mode bit(3)

1 = Switches the Frequency Control mode to High-Accuracy mode
0 = Frequency Control mode works in regular mode

bit 1 **FOREN:** Frequency Offset Register Enable bit

1 = Enables the offset value calculated by the offset sample. The offset value is added to the frequency control word of the PLL which tunes the desired carrier frequency.
0 = Denies the addition of the offset value to the frequency control word of the PLL

bit 0 **FOFEN:** Frequency Offset Enable bit

1 = Enables the frequency offset calculation using the AFC circuit
0 = Disables the frequency offset calculation using the AFC circuit

Note 1: The FRES is the frequency tuning resolution for each band. The FRES for each band is as follows:
433 MHz = 2.5 kHz
868 MHz = 5 kHz
915 MHz = 7.5 kHz

2: The offset error value is stored in the Offset register (FOREN bit should be enabled) in the AFC block and is added to the frequency control word of the PLL. Reset this bit before initiating another sample.

3: In High-Accuracy (Fine) mode, the processing time is twice the regular mode, but the uncertainty of the measurement is significantly reduced.

REGISTER 2-4: TXCREG: TRANSMIT CONFIGURATION REGISTER (POR: 0x9800)

W-1	W-0	W-0	W-1	W-1	W-0	W-0	W-0
CCB<15:9>							MODPLY
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
MODBW<3:0>				r	OTXPWR<2:0>		
bit 7							bit 0

Legend:	r = reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **CCB<15:9>:** Command Code bits

The command code bits (1001100b) are serially sent to the microcontroller to identify the bits to be written in the TXCREG.

bit 8 **MODPLY:** Modulation Polarity bit (for FSK)

When MODPLY is configured as high/low:

1 = Logic '0' is the higher channel frequency and logic '1' is the lower channel frequency (negative deviation)

0 = Logic '0' is the lower channel frequency and logic '1' is the higher channel frequency (positive deviation)

bit 7-4 **MODBW<3:0>:** Modulation Bandwidth bits

These bits set the FSK frequency deviation for transmitting the logic '1' and logic '0'**(1)**.

1111 = 240 kHz
1110 = 225 kHz
1101 = 210 kHz
1100 = 195 kHz
1011 = 180 kHz
1010 = 165 kHz
1001 = 150 kHz
1000 = 135 kHz
0111 = 120 kHz
0110 = 105 kHz
0101 = 90 kHz
0100 = 75 kHz
0011 = 60 kHz
0010 = 45 kHz
0001 = 30 kHz
0000 = 15 kHz

bit 3 **Reserved:** Write as '0'

Note 1: The transmitter FSK modulation parameters are used for calculating the resulting output frequency, as shown in Equation 2-1.

2: The output transmit power range is relative to the maximum available power, which depends on the actual antenna impedance.

REGISTER 2-4: TXCREG: TRANSMIT CONFIGURATION REGISTER (POR: 0x9800) (CONTINUED)

bit 2-0 **OTXPWR<2:0>:** Output Transmit Power Range bits(2)

These bits set the transmit output power range. The output power is programmable from 0 dB (Max.) to -17.5 dB in -2.5 dB steps.

111 = -17.5 dB
110 = -15.0 dB
101 = -12.5 dB
100 = -10.5 dB
011 = -7.5 dB
010 = -5.0 dB
001 = -2.5 dB
000 = 0 dB

Note 1: The transmitter FSK modulation parameters are used for calculating the resulting output frequency, as shown in Equation 2-1.

2: The output transmit power range is relative to the maximum available power, which depends on the actual antenna impedance.

EQUATION 2-1:

$f_{FSKOUT} = f_0 + [(-1)^{SIGN} \times (MB + 1) \times (15\ kHz)]$

where:

f_0 is the Channel Center Frequency (see Register 2-6 for f_0 Calculation)

MB is the 4-bit Binary Number (MODBW<3:0>)

SIGN = MODPLY XOR FSK

REGISTER 2-5: TXBREG: TRANSMIT BYTE REGISTER (POR: 0xB8AA)

W-1	W-0	W-1	W-1	W-1	W-0	W-0	W-0
CCB<15:8>							
bit 15							bit 8

W-1	W-0	W-1	W-0	W-1	W-0	W-1	W-0
TXDB<7:0>							
bit 7							bit 0

Legend:	r = reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **CCB<15:8>:** Command Code bits

The command code bits (10111000b) are serially sent to the microcontroller to identify the bits to be written in the TXBREG.

bit 7-0 **TXDB<7:0>:** Transmit Data Byte bits

The transmit data bits hold the 8 bits that are to be transmitted. To use this register, set the bit, TXDEN = 1 (GENCREG<7>). If TXDEN is not set, use the FSK/DATA/$\overline{\text{FSEL}}$ pin to manually modulate the data.