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MRF89XA
Data Sheet

Ultra Low-Power, Integrated ISM Band Sub-GHz Transceiver

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MRF89XA

Ultra Low-Power, Integrated ISM Band Sub-GHz Transceiver

Features

- Fully integrated ultra low-power, sub-GHz transceiver
- Wide-band half-duplex transceiver
- Supports proprietary sub-GHz wireless protocols
- Simple 4-wire SPI-compatible interface
- CMOS/TTL-compatible I/Os
- On-chip oscillator circuit
- Dedicated clock output
- Supports power-saving modes
- Operating voltage: 2.1-3.6V
- Low-current consumption, typically:
  - 3 mA in RX mode
  - 25 mA @ +10 dBm in TX mode
  - 0.1 µA (Typical) and 2 µA (Maximum) in Sleep mode
- Supports Industrial temperature range (-40ºC to +85ºC)
- Complies with ETSI EN 300-220 and FCC part 15
- Small, 32-pin TQFN package

RF/Analog Features

- Supports ISM band sub-GHz frequency ranges: 863–870, 902–928 and 950–960 MHz
- Modulation technique: Supports FSK and OOK
- Supports high data rates: Up to 200 kbps, NRZ coding
- Reception sensitivity: Down to -107 dBm at 25 kbps in FSK, -113 dBm at 2 kbps in OOK
- RF output power: +12.5 dBm programmable in eight steps
- Wide Received Signal Strength Indicator (RSSI), dynamic range: 70 dB from RX noise floor
- Signal-ended RF input/output
- On-chip frequency synthesizer
- Supports PLL loop filter with lock detect
- Integrated Power Amplifier (PA) and Low Noise Amplifiers (LNA)
- Channel filters
- On-chip IF gain and mixers
- Integrated low-phase noise VCO

Baseband Features

- Packet handling feature with data whitening and automatic CRC generation
- Incoming sync word (pattern) recognition
- Built-in bit synchronizer for incoming data, and clock synchronization and recovery
- 64-byte transmit/receive FIFO with preload in Stand-by mode
- Supports Manchester encoding/decoding techniques

Typical Applications

- Home/industrial/building automation
- Remote wireless control
- Wireless PC peripherals
- Remote keyless entry
- Wireless sensor networks
- Vehicle sensor monitoring
- Telemetry
- Data logging systems
- Wireless alarm
- Remote automatic meter reading
- Security systems for home/industrial environments
- Automobile immobilizers
- Sports and performance monitoring
- Wireless toy controls
- Medical applications

General Description

The MRF89XA is a single chip, multi-channel FSK/OOK transceiver capable of operating in the 863-870 MHz and 902-928 MHz license-free ISM frequency bands, as well as the 950-960 MHz frequency band. The low-cost MRF89XA is optimized for very low-power consumption. It incorporates a baseband modem with data rates up to 200 kbps. Data handling features include a 64-byte FIFO, packet handling, automatic CRC generation and data whitening.

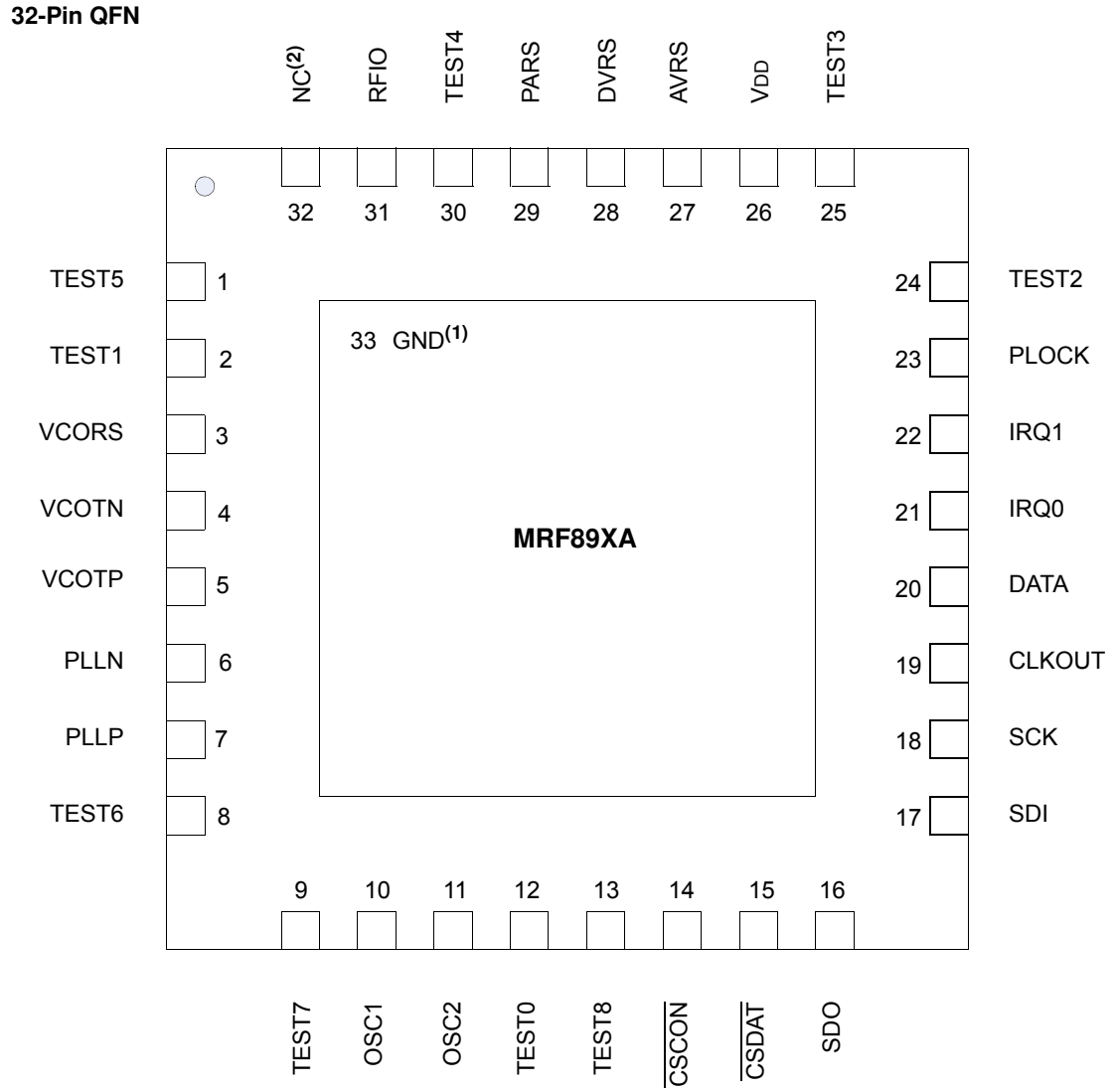
Its highly integrated architecture allows for minimum external component count while still maintaining design flexibility.

All critical RF and baseband functions are integrated in the MRF89XA, which minimizes the external component count and reducing design time. The RF communication parameters are made programmable and most of them may be dynamically set. A microcontroller, RF SAW filter, 12.8 MHz crystal and a few passive components are required to create a complete, reliable radio function. The MRF89XA uses several low-power mechanisms to reduce overall current consumption and extend battery life. Its small size and low-power consumption makes the MRF89XA ideal for a wide variety of short range radio applications. The MRF89XA complies with European (ETSI EN 300-220) and United States (FCC Part 15.247 and 15.249) regulatory standards.

Pin Diagram

Figure 1 illustrates the top view pin arrangement of the 32-pin QFN package.

FIGURE 1: MRF89XA 32-PIN QFN PIN DIAGRAM



Note 1: Pin 33 (GND) is located on the underside of the IC package.

2: It is recommended to connect Pin 32 (NC) to GND.

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NOTES:

1.0 OVERVIEW

Microchip's MRF89XA is a fully integrated, half-duplex, sub-GHz transceiver. This low-power, single chip FSK and OOK baseband transceiver supports:

- Superheterodyne architecture
- Multi-channel, multi-band synthesizer with Phase Locked Loop (PLL) for easy RF design
- Power Amplifier (PA)
- Low Noise Amplifier (LNA)
- I/Q two stage down converter mixers
- I/Q demodulator, FSK/OOK
- Baseband filters and amplifiers

The simplified block diagram of the MRF89XA is illustrated in Figure 1-1.

The MRF89XA is a good option for low-cost, high-volume, low data rate (≤200 kbps), and two-way short range wireless applications. This device is a single chip FSK and OOK transceiver capable of operating in the 863-870 MHz and 902-928 MHz license-free ISM frequency bands, and the 950-960 MHz frequency band.

The low-cost MRF89XA is optimized for very low-power consumption (3 mA in Receive mode). It incorporates a baseband modem with data rates up to 200 kbps in FSK and 32 kbps in OOK. Data handling features include a 64-byte FIFO, packet handling, automatic CRC generation and data whitening. The device also supports Manchester coding techniques. Its highly integrated architecture allows for minimum external component count while maintaining design flexibility. All major RF communication parameters are programmable and most of them may be dynamically set.

The MRF89XA supports a stable sensitivity and linearity characteristics for a wide supply range and is internally regulated. The frequency synthesizer of the MRF89XA is a fully integrated integer-N type PLL. The oscillator circuit provided on the MRF89XA device provides the reference clock for the PLL. The frequency synthesizer requires only five external components which includes PLL loop filter and the VCO tank circuit. Low-phase noise provides for excellent adjacent channel rejection capability, Bit Error Rate (BER) and longer communication range.

The high-resolution PLL allows:

- Usage of multiple channels in any of the bands
- Rapid settling time, which allows for faster frequency hopping

A communication link in most applications can be created using a low-cost 12.8 MHz crystal, a SAW filter and a low-cost microcontroller. The MRF89XA provides a clock signal for the microcontroller. The transceiver can be interfaced with many popular Microchip PIC® microcontrollers through a 4-wire Serial Peripheral Interface (SPI), interrupts (IRQ0 and IRQ1), PLL lock and clock out. The interface between the microcontroller and MRF89XA (a typical MRF89XA RF node) is illustrated in Figure 1-2.

The MRF89XA supports the following digital data processing features:

- Received Signal Strength Indicator (RSSI)
- Sync word recognition
- Packet handling
- Interrupt and flags
- Different operating Modes (Continuous, Buffer and Packet)
- Data filtering/whitening/encoding
- Baseband power amplifier
- 64-byte TX/RX FIFO

The role of the digital processing unit is to interface the data to/from the modulator/demodulator and the microcontroller access points (SPI, IRQ and DATA pins). It also controls all of the Configuration registers. The receiver's Baseband Bandwidth (BBBW) can be programmed to accommodate various deviations and data rates requirements.

An optional Bit Synchronizer (BitSync) is provided, to supply a synchronous clock and data stream to a companion microcontroller in Continuous mode, or to fill the FIFO with glitch-free data in Buffered mode. The transceiver is integrated with different power-saving modes and a software wake-up time through the host microcontroller to keep track of the activities, which reduces the overall current consumption and extends the battery life. The small size and low-power consumption of the MRF89XA makes it ideal for various short range radio applications.

The MRF89XA complies with European (ETSI EN 300-220) and United States (FCC Part 15.247 and 15.249) regulatory standards.

FIGURE 1-1: MRF89XA SIMPLIFIED BLOCK DIAGRAM

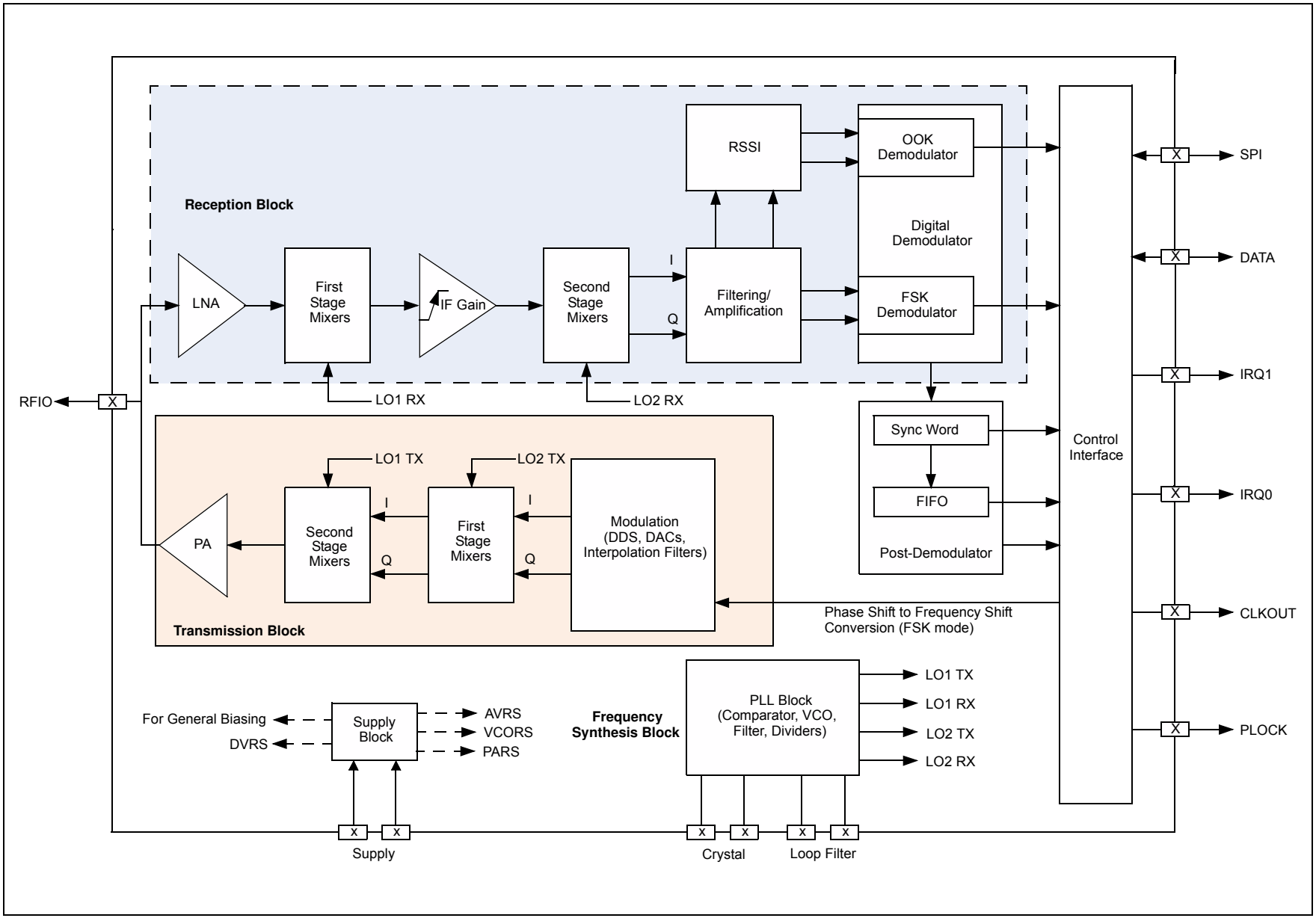
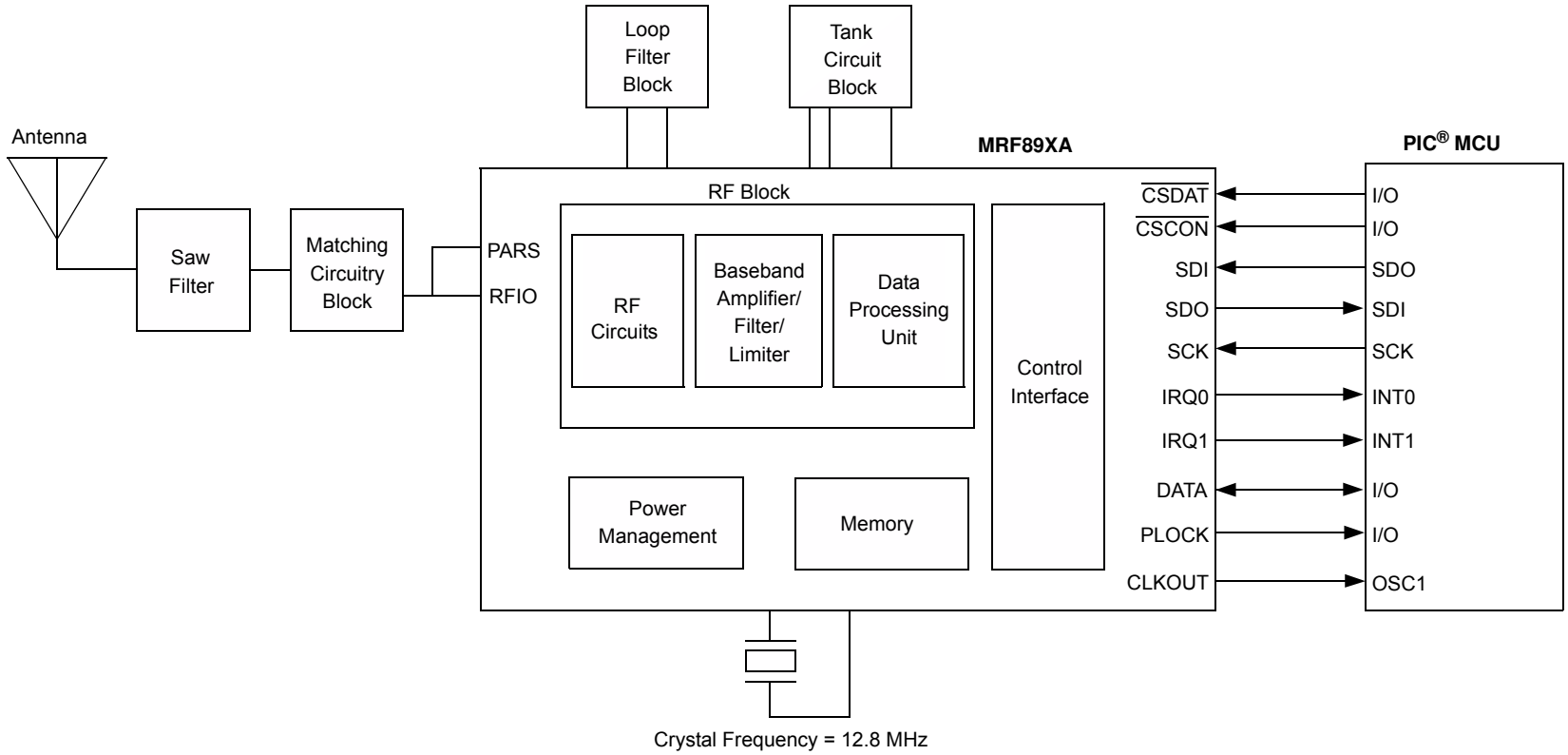


FIGURE 1-2: MRF89XA TO MICROCONTROLLER INTERFACE (NODE) BLOCK DIAGRAM



Note: The interface between the MRF89XA and the MCU depends on the Data mode of operation. For more information, refer to Section 3.8, Data Processing.

NOTES:

2.0 HARDWARE DESCRIPTION

The MRF89XA is an integrated, single chip, low-power ISM band sub-GHz transceiver. A detailed block diagram of the MRF89XA is illustrated in Figure 2-1. The frequency synthesizer is clocked by an external 12.8 MHz crystal, and frequency ranges from 863-870 MHz, 902-928 MHz and 950-960 MHz are possible.

The MRF89XA receiver employs a superheterodyne architecture. The first IF is one-ninth of the RF frequency (approximately 100 MHz). The second down conversion, down converts the I and Q signals to baseband in the case of the FSK receiver (zero-IF) and to a low-IF (IF2) for the OOK receiver. After the second down-conversion stage, the received signal is channel select filtered and amplified to a level adequate for demodulation. Both FSK and OOK demodulation are available. Image rejection is achieved using a SAW filter.

The baseband I and Q signals at the transmitter side are digitally generated by a Direct Digital Synthesis (DDS) whose Digital-to-Analog Converters (DAC) are followed by two anti-aliasing low-pass filters that transform the digital signal into analog In-Phase (I) and Quadrature (Q) components with frequency as the selected Frequency Deviation (f_{dev}). The transmitter supports both FSK and OOK modes of operation. The transmitter has a typical output power of +12.5 dBm. An internal transmit/receive switch combines the transmitter and receiver circuits into a single-ended RFIO pin (pin 31). The RFIO pin is connected through the impedance matching circuitry to an external antenna. The device operates in the low-voltage range of 2.1-3.6V, and in Sleep mode, it operates at a very low-current state, typically 0.1 µA.

The frequency synthesizer is based on an integer-N PLL having PLL bandwidth of 15 kHz. Two programmable frequency dividers in the feedback loop of the PLL and one programmable divider on the reference oscillator allow the LO frequency to be adjusted. The reference frequency is generated by a crystal oscillator running at 12.8 MHz.

The MRF89XA is controlled by a digital block that includes registers to store the configuration settings of the radio. These registers are accessed by a host microcontroller through a Serial Peripheral Interface (SPI). The quality of the data is validated using the RSSI and bit synchronizer blocks built into the transceiver. Data is buffered in a 64-byte transmitter or receiver FIFO. The transceiver is controlled through a 4-wire SPI, interrupts (IRQ0 and IRQ1), PLOCK, DATA and Chip Select pins for SPI are illustrated in Figure 2-1. On-chip regulators provide stable supply voltages to sensitive blocks and allow the MRF89XA to be used with supply voltages from 2.1-3.6V. Most blocks are supplied with a voltage below 1.4V.

The MRF89XA supports the following feature blocks:

- Data filtering and whitening
- Bit synchronization
- 64-byte transmit/receive FIFO buffer
- General configuration registers

These features reduce the processing load, which allows the use of simple, low-cost, 8-bit microcontrollers for data processing.

FIGURE 2-1: DETAILED BLOCK DIAGRAM OF THE MRF89XA

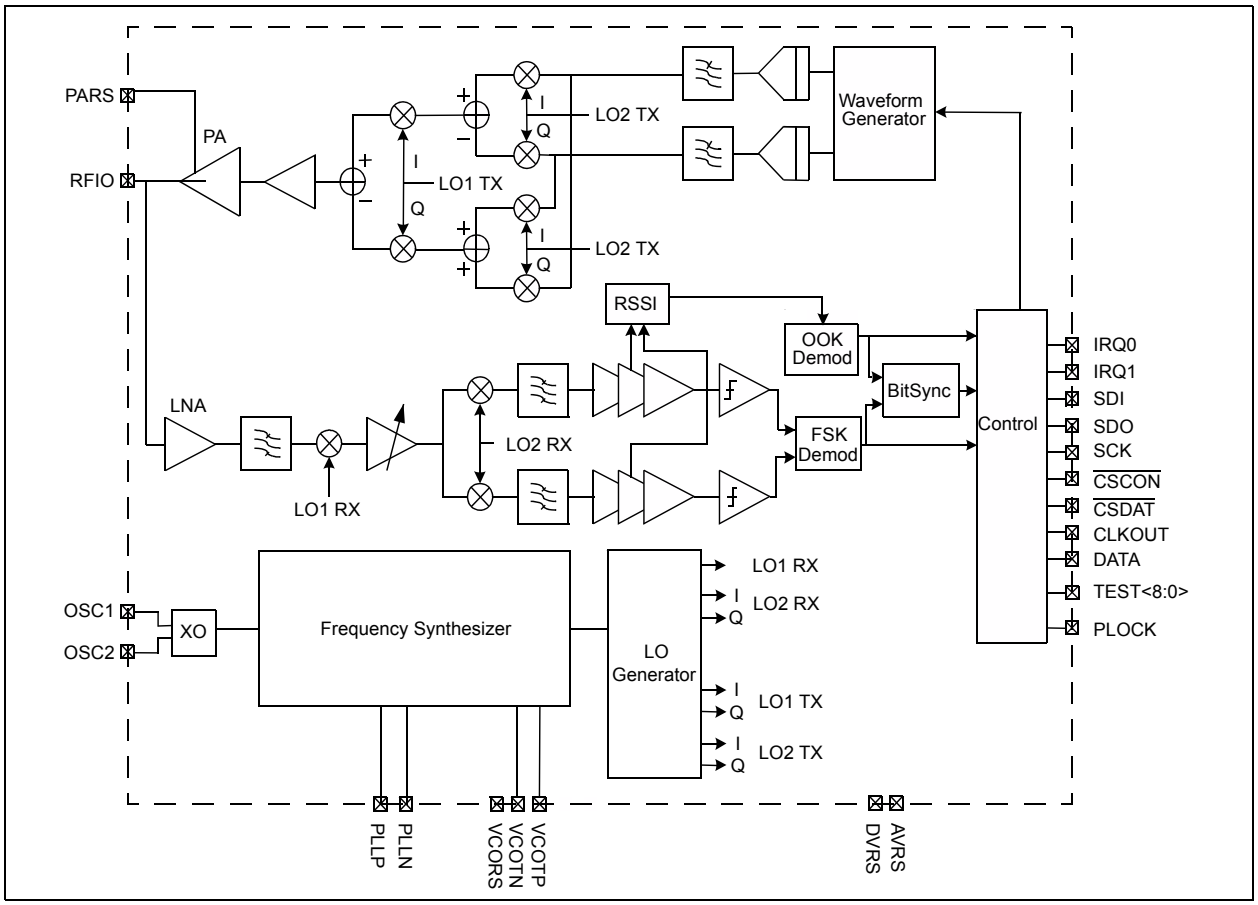


TABLE 2-1: PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Type	Description
1	TEST5	Digital I/O	Test Pin. Connected to Ground during normal operation.
2	TEST1	Digital I/O	Test Pin. Connected to Ground during normal operation.
3	VCORS	Analog Output	Regulated voltage supply of the VCO (0.85V).
4	VCOTN	Analog I/O	VCO tank.
5	VCOTP	Analog I/O	VCO tank.
6	PLLN	Analog I/O	PLL loop filter.
7	PLLP	Analog I/O	PLL loop filter.
8	TEST6	Digital I/O	Test Pin. Connected to Ground during normal operation.
9	TEST7	Digital I/O	Test Pin. Connected to Ground during normal operation.
10	OSC1	Analog Input	Crystal connection.
11	OSC2	Analog Input	Crystal connection.
12	TEST0	Digital Input	Test Pin. Connected to Ground during normal operation.
13	TEST8	Digital I/O	Test Pin. Allow pin to float; do not connect signal during normal operation.
14	$\overline{\text{CSCON}}$	Digital Input	SPI Configure Chip Select.
15	$\overline{\text{CSDAT}}$	Digital Input	SPI Data Chip Select.
16	SDO	Digital Output	Serial data output interface from MRF89XA.
17	SDI	Digital Input	Serial data input interface to MRF89XA.
18	SCK	Digital Input	Serial clock interface.
19	CLKOUT	Digital Output	Clock output. Output clock at reference frequency divided by a programmable factor. Refer to the Clock Output Control Register (Register 2-28) for more information.
20	DATA	Digital I/O	NRZ data input and output (Continuous mode).
21	IRQ0	Digital Output	Interrupt request output.
22	IRQ1	Digital Output	Interrupt request output.
23	PLOCK	Digital Output	PLL lock detection output. Refer to the FIFO Transmit PLL and RSSI Interrupt Request Configuration Register (Register 2-15) for more information.
24	TEST2	Digital I/O	Test Pin. Connected to Ground during normal operation.
25	TEST3	Digital I/O	Test Pin. Connected to Ground during normal operation.
26	V_{DD}	Power	Supply voltage.
27	AVRS	Analog Output	Regulated supply of the analog circuitry (1.0V).
28	DVRS	Analog Output	Regulated supply of the digital circuitry (1.0V).
29	PARS	Analog Output	Regulated supply of the PA (1.8V).
30	TEST4	Digital I/O	Test Pin. Connected to Ground during normal operation.
31	RFIO	Analog I/O	RF input/output (for more information, see Section 2.3, RFIO Pin).
32	NC	—	No Connection. Connected to Ground during normal operation.
33	Vss	Ground	Exposed Pad. Connected to Ground during normal operation.

2.1 Power Supply and Ground Block Pins

To provide stable sensitivity and linearity characteristics over a wide supply range, the MRF89XA is internally voltage regulated. This internal regulated power supply block structure is illustrated in Figure 2-2.

The power supply bypassing is essential for better handling of signal surges and noise in the power line. To ensure correct operation of the regulator circuit, the decoupling capacitor connection (shown in Figure 2-2) is recommended. These decoupling components are recommended for any design. The power supply block generates four regulated supplies for the analog, digital, VCO and the PLL blocks to reduce the voltages for their specific requirements. However, Power-on Reset (POR), Configuration registers and the SPI use the VDD supply given to the MRF89XA.

The large value decoupling capacitors should be placed at the PCB power input. The smaller value decoupling capacitors should be placed at every power point of the device and at bias points for the RF port. Poor bypassing can lead to conducted interference, which can cause noise and spurious signals to couple into the RF sections, thereby significantly reducing the performance.

It is recommended that the VDD pin have two bypass capacitors to ensure sufficient bypass and decoupling. However, based on the selected carrier frequency, the bypass capacitor values vary. The trace length (VDD pin to bypass capacitors) should be made as short as possible.

FIGURE 2-2: POWER SUPPLY BLOCK DIAGRAM

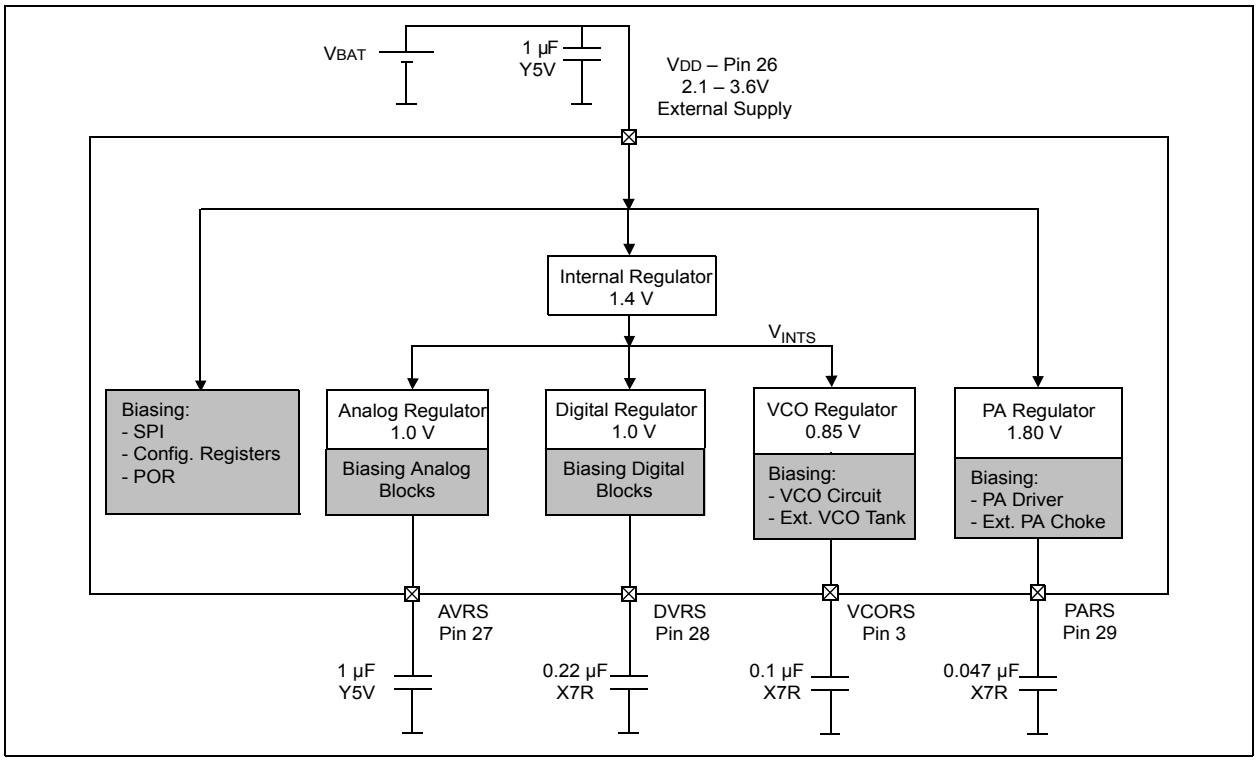


TABLE 2-2: POWER SUPPLY PIN DETAILS

Blocks	Biasing Through	Associated Pins	Regulated Voltage (in Volts)
POR, SPI and Configuration Registers	VDD	VDD	2.1–3.6
Regulated Supply (VINTS)	VDD	VDD	1.4
Analog	VINTS	AVRS	1.0
Digital	VINTS	DVRS	1.0
VCO	VINTS	VCORS	0.85
PA	VDD	PARS	1.8

2.2 Reset Pin

The device enters the Reset mode if any of the following events take place:

- Power-on Reset (POR)
- Manual Reset

The POR happens when the MRF89XA is switched on using VDD. The POR cycle takes at least 10 ms to execute any communication operations on the SPI bus.

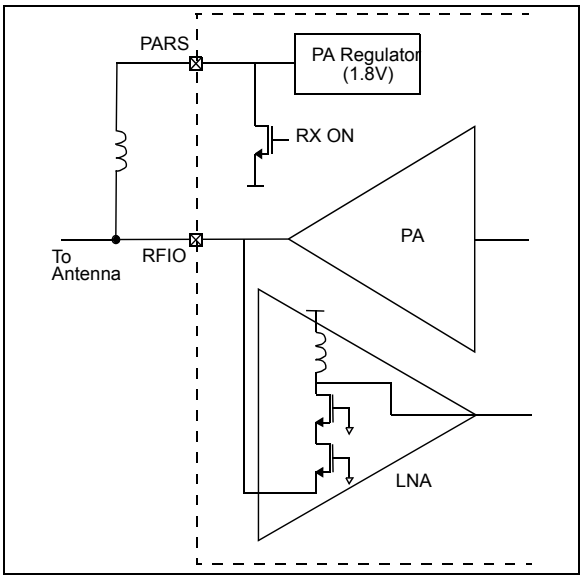
An external hardware or manual Reset of the MRF89XA can be performed by asserting the TEST8 pin (pin 13) to high for 100 µs and then releasing the pin. After releasing the pin, it takes more than 5 ms for the transceiver to be ready for any operations. The pin is driven with an open-drain output, therefore, is pulled high while the device is in POR. The device will not accept commands during the Reset period. For more information, refer to Section 3.1.2, Manual Reset.

2.3 RFIO Pin

The receiver and the transmitter share the same RFIO pin (pin 31). Figure 2-3 illustrates the configuration of the common RF front-end.

- In Transmit mode, the PA and the PA regulator are ON with voltage on the PARS pin (pin 29) equal to the nominal voltage of the regulator (about 1.8V). The external RF choke inductance is used to bias the PA.
- In Receive mode, the PA and PA regulator are OFF and PARS is tied to ground. The external RF choke inductor is used for biasing and matching the LNA (this is basically implemented as a common gate amplifier).

FIGURE 2-3: COMMON RF INPUT AND OUTPUT PIN DIAGRAM



The PA and the LNA front-ends in the MRF89XA, which share the same Input/Output pin, are internally matched to approximately 50Ω.

2.4 Filters and Amplifiers Block

2.4.1 INTERPOLATION FILTER

After digital-to-analog conversion during transmission, both I and Q signals are smoothed by interpolation filters. These low-pass filters the digitally generated signal, and prevents the alias signals from entering the modulators.

2.4.2 POWER AMPLIFIER

The Power Amplifier (PA) integrated in the MRF89XA operates under a regulated voltage supply of 1.8V. The external RF choke inductor is biased by an internal regulator output made available on the PARS pin (pin 29). Therefore, the PA output power is consistent over the power supply range. This is important for applications which allows both predictable RF performance and battery life.

An open collector output requires biasing using an inductor as an RF choke. For the recommended PA bias and matching circuit details see Section 4.4.2, Suggested PA Biasing And Matching.

Note:	Image rejection is achieved using a SAW filter on the RF input.

The matching of the SAW filter depends on the SAW filter selected. Many modern SAW filters have 50Ω input and output, which simplifies matching for the MRF89XA. This is demonstrated in the application circuit. If the choice of SAW filter is different than 50Ω, the required impedance match on the input and output of the SAW filter will be needed.

2.4.3 LOW NOISE AMPLIFIER (WITH FIRST MIXER)

In Receive mode, the RFIO pin (pin 31) is connected to a fixed gain, common-gate, Low Noise Amplifier (LNA). The performance of this amplifier is such that the Noise Figure (NF) of the receiver is estimated to be approximately 7 dB.

The LNA has approximately 50Ω impedance, which functions well with the proposed antenna (PCB/Monopole) during signal transmission. The LNA is followed by an internal RF band-pass filter.

2.4.4 IF GAIN AND SECOND I/Q MIXER

Following the LNA and first down-conversion, there is an IF amplifier whose gain can be programmed from 13.5-0 dB in 4.5 dB steps, through the register DMODREG. For more information, refer to Section 2.14.2, DATA AND MODULATION CONFIGURATION REGISTER DETAILS. The default setting corresponds to 0 dB gain, but lower values can be used to increase the RSSI dynamic range.

2.4.5 CHANNEL FILTERS

The second mixer stages are followed by the channel select filters. The channel select filters have a strong influence on the noise bandwidth and selectivity of the receiver and therefore, its sensitivity. Each channel select filter features a passive second-order RC filter, with a programmable bandwidth and the “fine” channel selection is performed by an active, third-order, Butterworth filter, which acts as a low-pass filter for the zero-IF configuration (FSK), or a complex polyphase filter for the low-IF (OOK) configuration. For more information on configuring passive and active filters see Section 3.4.4, Channel Filters.

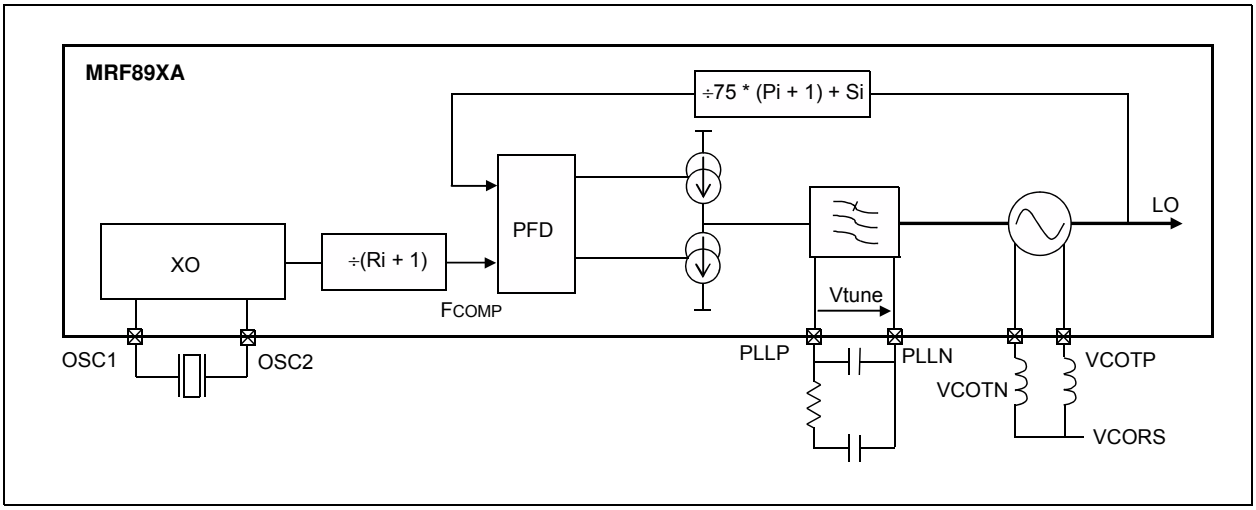
2.5 Frequency Synthesizer Block

The frequency synthesizer of the MRF89XA is a fully integrated integer-N type PLL. The crystal oscillator provides the reference frequency for the PLL. The PLL circuit requires only a minimum of five external components for the PLL loop filter and the VCO tank circuit.

Figure 2-4 illustrates a block schematic of the MRF89XA PLL. Here the crystal reference frequency and the software controlled dividers R, P and S blocks determine the output frequency of the PLL.

The VCO tank inductors are connected on an external differential input. Similarly, the loop filter is also located externally.

FIGURE 2-4: FREQUENCY SYNTHESIZER BLOCK DIAGRAM



2.5.1 REFERENCE OSCILLATOR PINS (OSC1/OSC2)

The MRF89XA has an internal, integrated oscillator circuit and the OSC1 and OSC2 pins are used to connect to an external crystal resonator. The crystal oscillator provides the reference frequency for the PLL. The crystal oscillator circuit, with the required loading capacitors, provides a 12.8 MHz reference signal for the PLL. The PLL then generates the local oscillator frequency. It is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The crystal oscillator load capacitance is typically 15 pF, which allows the crystal oscillator circuit to accept a wide range of crystals.

Choosing a higher tolerance crystal results in a lower TX to RX frequency offset and the ability to select a smaller deviation in baseband bandwidth. Therefore, the recommended crystal accuracy should be ≤ 40 ppm. The guidelines for selecting the appropriate crystal with specifications are explained in Section 4.6, Crystal Specification and Selection Guidelines.

Note:	Crystal frequency error will directly translate to carrier frequency (f_{rf}), bit rate and frequency deviation error.

2.5.2 CLKOUT OUTPUT PIN (CLKOUT)

The transceiver can provide a clock signal through the CLKOUT pin (pin 19) to the microcontroller for accurate timing, thereby eliminating the need for a second crystal. This results in reducing the component count. The CLKOUT is a sub-multiple of the reference frequency and is programmable.

The two main functions of the CLKOUT output are:

- To provide a clock output for a host microcontroller, thus saving the cost of an additional oscillator.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note:	To minimize the current consumption of the MRF89XA, ensure that the CLKOUT signal is disabled when unused.

CLKOUT can be made available in any operation mode, except Sleep mode, and is automatically enabled at power-up.

2.5.3 PHASE-LOCKED LOOP ARCHITECTURE

The Integer-N Phase-Locked Loop (PLL) circuitry determines the operating frequency of the device. The PLL maintains accuracy using the crystal-controlled reference oscillator and provides maximum flexibility in performance to the designers.

The high resolution of the PLL allows the use of multiple channels in any of the bands. The on-chip PLL is capable of performing manual and automatic calibration to compensate for the changes in temperature or operating voltage.

2.5.3.1 PLL Lock Pin (PLOCK)

The MRF89XA features a PLL lock (PLOCK) detect indicator. This is useful for optimizing power consumption, by adjusting the synthesizer wake-up time. The lock status can also be read on the LSTSPLL bit from the FTPRIREG register (Register 2-15), and must be cleared by writing a '1' to this same register. The lock status is available on the PLOCK pin (pin 23), by setting the LENPLL bit in the FTPRIREG register.

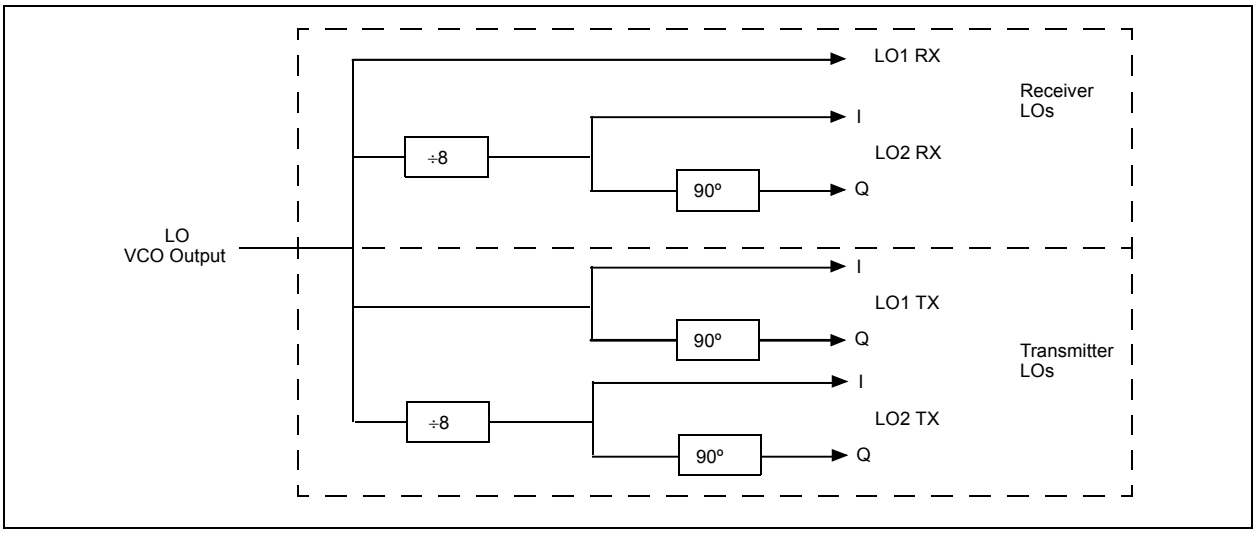
2.5.4 VOLTAGE CONTROLLED OSCILLATOR

The integrated Voltage Controlled Oscillator (VCO) requires two external tank circuit inductors. As the input is differential, the two inductors must have the same nominal value. The performance of these components are essential for both the phase noise and the power consumption of the PLL. It is recommended that a pair of high Q inductors is selected. These should be mounted orthogonally to other inductors in the circuit (in particular the PA choke) to reduce spurious coupling between the PA and VCO. For best performance, wire wound high-Q inductors with tight tolerance should be used as described in Section 4.0, Application Details. In addition, such measures may reduce radiated pulling effects and undesirable transient behavior, thus minimizing spectral occupancy.

Note:	Ensuring a symmetrical layout of the VCO inductors will further improve PLL spectral purity.

The output signal of the VCO is used as the input to the local oscillator (LO) generator stage, as illustrated in Figure 2-5.The VCO frequency is subdivided and used in a series of up/down conversions for transmission/reception.

FIGURE 2-5: LO VCO OUTPUT GENERATOR



2.6 MRF89XA Operating Modes (Includes Power-Saving Mode)

This section summarizes the settings for each operating modes of the MRF89XA to save power that are based on the operations and available functionality. The timing requirements for switching between modes described in Section 5.3, Switching Times and Procedures.

2.6.1 MODES OF OPERATION

Table 2-3 lists the different operating modes of the MRF89XA, which can be used to save power.

2.6.2 DIGITAL PIN CONFIGURATION VS. CHIP MODE

Table 2-4 lists the state of the digital I/Os in each of the above described modes of operation, regardless of the data operating mode (Continuous, Buffered, or Packet).

TABLE 2-3: OPERATING MODES

Mode	CMOD<2:0> bits (GCONREG<7:5>	Active Blocks
Sleep	000	SPI, POR.
Stand-by	001	SPI, POR, Top regulator, digital regulator, XO, CLKOUT (if activated through CLKOREG).
FS	010	Same as Stand-by + VCO regulator, all PLL and LO generation blocks.
Receive	011	Same as FS mode + LNA, first mixer, IF amplifier, second mixer set, channel filters, baseband amplifiers and limiters, RSSI, OOK or FSK demodulator, BitSync and all digital features if enabled.
Transmit	100	Same as FS mode + DDS, Interpolation filters, all up-conversion mixers, PA driver, PA and external PARS pin (pin 29) output for the PA choke.

TABLE 2-4: PIN CONFIGURATION VS. CHIP MODE

Chip Mode Pin	Sleep Mode	Stand-by Mode	FS Mode	Receive Mode	Transmit Mode	Comment
$\overline{\text{CSCON}}$	Input	Input	Input	Input	Input	$\overline{\text{CSCON}}$ has priority over $\overline{\text{CSDAT}}$.
$\overline{\text{CSDAT}}$	Input	Input	Input	Input	Input	—
SDO(4)	Output	Output	Output	Output	Output	Output only if $\overline{\text{CSCON}}$ or $\overline{\text{CSDAT}}$ = 0.
SDI	Input	Input	Input	Input	Input	—
SCK	Input	Input	Input	Input	Input	—
IRQ0(3)	High-Z	Output(1)	Output(1)	Output	Output	—
IRQ1(3)	High-Z	Output(1)	Output(1)	Output	Output	—
DATA	Input	Input	Input	Output	Input	—
CLKOUT	High-Z	Output	Output	Output	Output	—
PLOCK	High-Z	Output(2)	Output(2)	Output(2)	Output(2)	—

Note 1: High-Z if Continuous mode is activated; otherwise, Output.

2: Output if LENPLL = 1; otherwise, High-Z.

3: Valid logic states must be applied to inputs at all times to avoid unwanted leakage currents. Suggestions for designers,

- Use external pull down resistor.
- Tristate the Microcontroller interrupt pin to output when setting the MRF89XA to sleep. Then reverse when waking it up. Since the Microcontroller is in control, this should be easy to do and not require an external pull down resistor.

4: The SDO pin defaults to a high impedance (High-Z) state when any of the CS pins are high (the MRF89XA is not selected).

2.7 Interrupt (IRQ0 and IRQ1) Pins

The Interrupt Requests (IRQ0 and IRQ1) pins 21 and 22, provide an interrupt signal to the host microcontroller from the MRF89XA. Interrupt requests are generated for the host microcontroller by pulling the IRQ0 (pin 21) or IRQ1 (pin 22) pins low or high based on the events and configuration settings of these interrupts. Interrupts must be enabled and unmasked before the IRQ pins are active. For detailed functional description of interrupts, see Section 3.8, Data Processing .

2.8 DATA Pin

After OOK or FSK demodulation, the baseband signal is available to the user on the DATA pin (pin 20), when Continuous mode is selected. Therefore, in Continuous mode, the NRZ data to or from the modulator or demodulator respectively is directly accessed by the host microcontroller on the bidirectional DATA pin. The SPI Data, FIFO and packet handler are therefore inactive. In Buffered and Packet modes, the data is retrieved from the FIFO through the SPI.

During transmission, the DATA pin is configured as DATA (Data Out) and with internal Transmit mode disabled; this manually modulates the data from the external host microcontroller. If the Transmit mode is enabled, this pin can be tied “high” or can be left unconnected.

During reception, the DATA pin is configured as DATA (Data In); this pin receives the data in conjunction with DCLK. DATA pin (unused in packed mode) should be pulled-up to VDD through a 100 kΩ resistor.

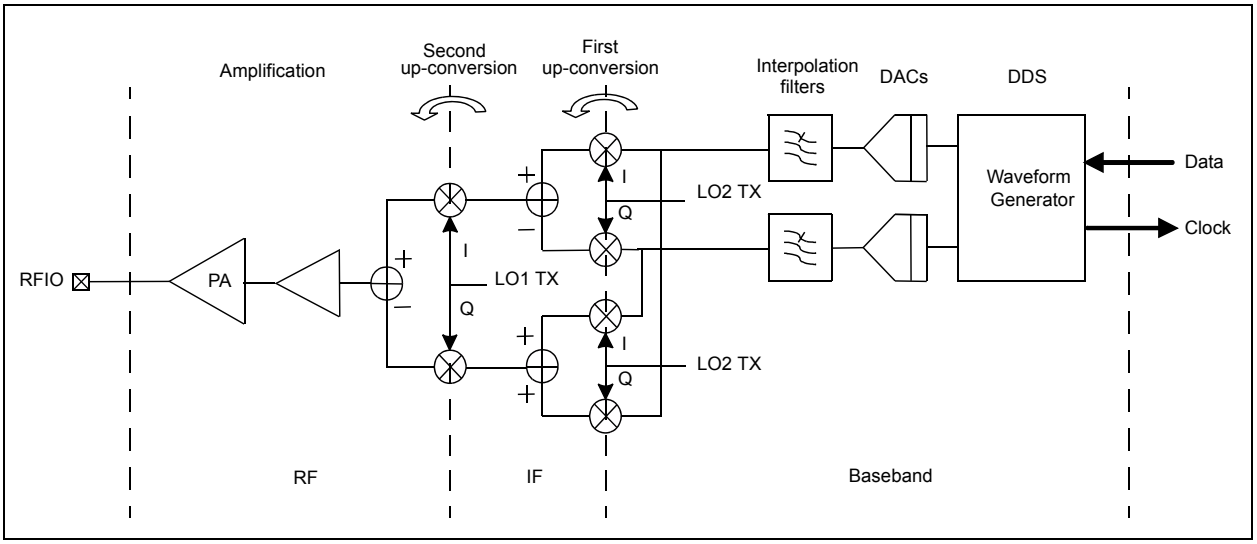
2.9 Transmitter

The transmitter chain is based on the same double-conversion architecture and uses the same intermediate frequencies as the receiver chain. The main blocks include:

A digital waveform generator that provides the I and Q base-band signals. This block includes digital-to-analog converters and anti-aliasing low-pass filters.

A compound image-rejection mixer to up-convert the baseband signal to the first IF at one-ninth of the carrier frequency (f_{rf}), and a second image-rejection mixer to up-convert the IF signal to the RF frequency transmitter driver and power amplifier stages to drive the antenna port.

FIGURE 2-6: TRANSMITTER ARCHITECTURE BLOCK DIAGRAM



2.9.1 TRANSMITTER ARCHITECTURE

Figure 2-6 illustrates the transmitter architecture block diagram. The baseband I and Q signals are digitally generated by a DDS whose Digital-to-Analog Converters (DAC) followed by two anti-aliasing low-pass filters transform the digital signal into analog in-phase (I) and quadrature (Q) components whose frequency is the selected frequency deviation, is set using the FDVAL<7:0> bits from FDEVREG<7:0>.

In FSK mode, the relative phase of I and Q is switched by the input data between -90° and +90° with continuous phase. The modulation is therefore performed at this initial stage, because the information contained in the phase difference will be converted into a frequency shift when the I and Q signals are up-converted in the first mixer stage. This first up-conversion stage is duplicated to enhance image rejection. The FSK convention is such that:

$$DATA = 1 \rightarrow f_{rf} + f_{dev}$$

$$DATA = 0 \rightarrow f_{rf} - f_{dev}$$

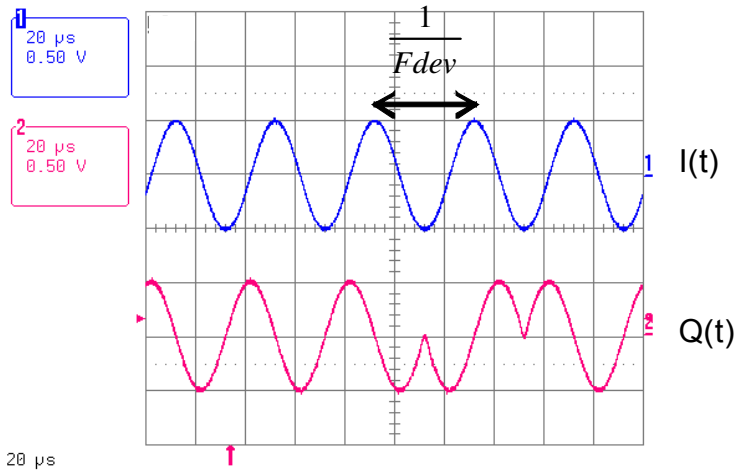
In OOK mode, the phase difference between the I and Q channels is kept constant (independent of the transmitted data). Thus, the first stage of up-conversion creates a fixed frequency signal at the low IF = f_{dev} (this explains why the transmitted OOK spectrum is offset by f_{dev}). OOK Modulation is accomplished by switching the PA and PA regulator stages ON and OFF. By convention:

$$DATA = 1 \rightarrow PAon$$

$$DATA = 0 \rightarrow PAoff$$

After the interpolation filters, a set of four mixers combines the I and Q signals and converts them into a pair of complex signals at the second intermediate frequency, equal to one-eighth of the LO frequency, or one-ninth of the RF frequency. These two new I and Q signals are then combined and up-converted to the final RF frequency by two quadrature mixers fed by the LO signal. The signal is pre-amplified, and then the transmitter output is driven by a final power amplifier stage. The I and Q signal details are illustrated in Figure 2-7.

FIGURE 2-7: I(t), Q(t) Signals Overview



2.10 Receiver

The receiver is based on a superheterodyne architecture and comprises the following major blocks:

- An LNA that provides low-noise RF gain followed by an RF band-pass filter.
- A first mixer, which down-converts the RF signal to an intermediate frequency equal to one-ninth of the carrier frequency (f_{rf} 100 MHz for 915 MHz signals).
- A variable gain first-IF preamplifier followed by two second mixers, which down-convert the first IF signal to I and Q signals at a low frequency (zero-IF for FSK, low-IF for OOK).
- A two-stage IF filter followed by an amplifier chain are available for both I and Q channels. Limiters at the end of each chain drive the I and Q inputs to the FSK demodulator function. An RSSI signal is also derived from the I and Q IF amplifiers to drive the OOK detector. The second filter stage in each channel can be configured as either a third-order Butterworth low-pass filter for FSK operation or an image reject polyphase band-pass filter for OOK operation.
- An FSK arctangent type demodulator driven from the I and Q limiter outputs, and an OOK demodulator driven by the RSSI signal. Either detector can drive a data and clock recovery function that provides matched filter enhancement of the demodulated data.

2.10.1 RECEIVER ARCHITECTURE

Figure 2-8 illustrates the receiver architecture block diagram. The first IF is one-ninth of the RF frequency (approximately 100 MHz). The second down-conversion down-converts the I and Q signals to baseband in the case of the FSK receiver (zero-IF) and to a low-IF (IF2) for the OOK receiver.

After the second down-conversion stage, the received signal is channel-select filtered and amplified to a level adequate for demodulation. Both FSK and OOK demodulation are available. Finally, an optional bit synchronizer (BitSync) is provided to supply a synchronous clock and data stream to a companion microcontroller in Continuous mode, or to fill the FIFO buffers with glitch-free data in Buffered mode.

Note:	Image rejection is achieved using a SAW filter on the RF input.

FIGURE 2-8: RECEIVER ARCHITECTURE BLOCK DIAGRAM

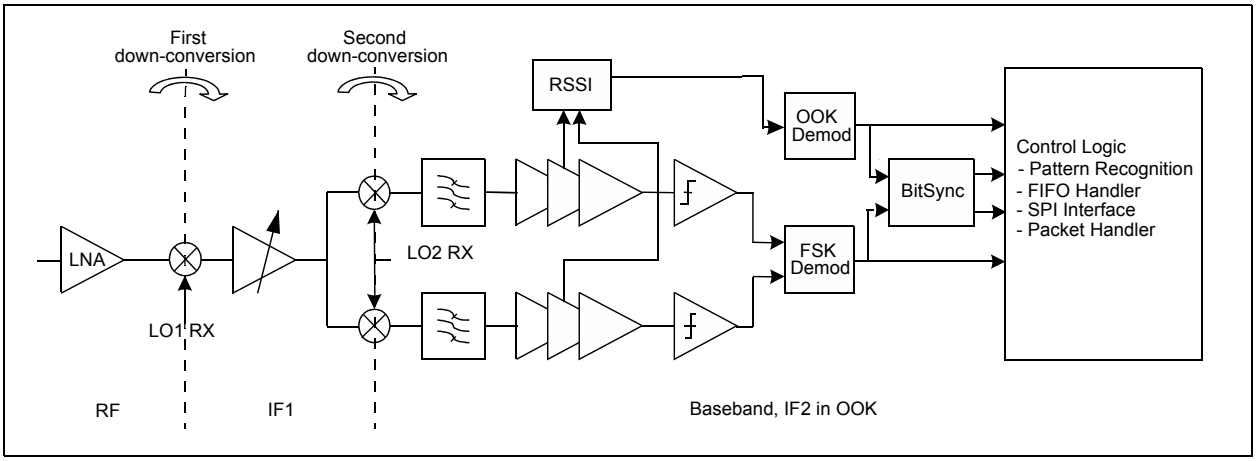


FIGURE 2-9: FSK RECEIVER SETTING

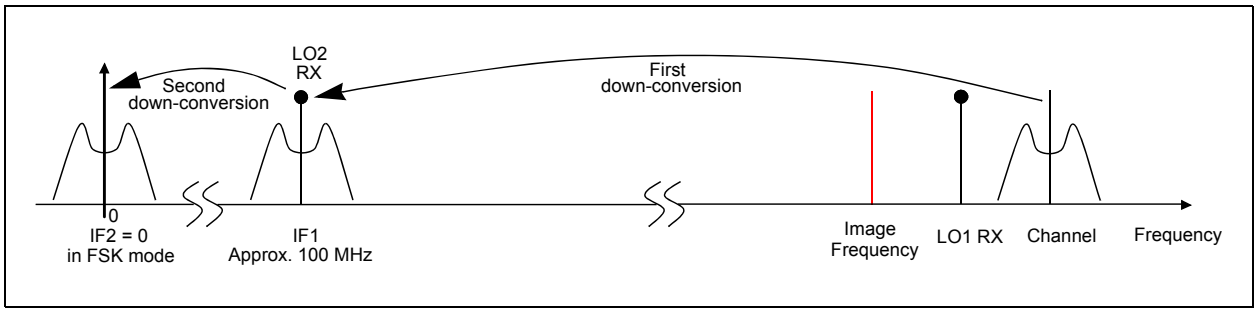
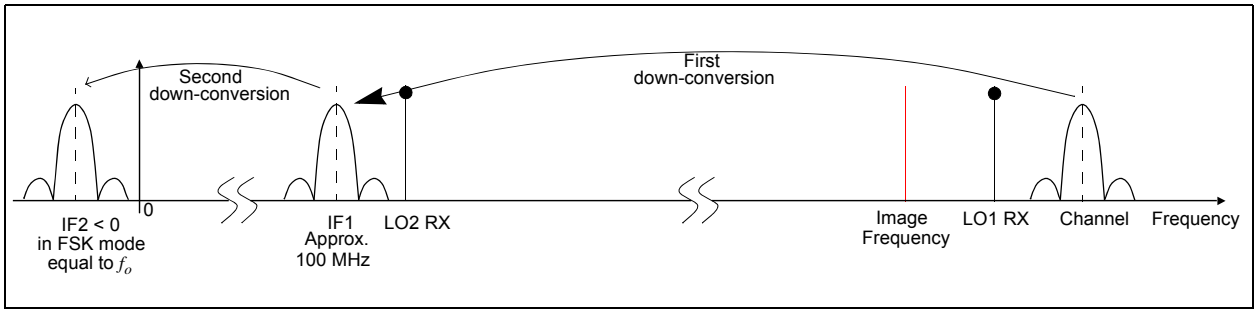


FIGURE 2-10: OOK RECEIVER SETTING



2.11 Serial Peripheral Interface (SPI)

The MRF89XA communicates with the host microcontroller through a 4-wire SPI port as a slave device. An SPI-compatible serial interface allows the user to select, command and monitor the status of the MRF89XA through the host microcontroller. All the registers are addressed through the specific addresses to control, configure and read status bytes.

The SPI in the MRF89XA consists of the following two sub-blocks, as illustrated in Figure 2-11.

- SPI CONFIG: This sub-block is used in all data operation modes to read and write the configuration registers which control all the parameters of the chip (operating mode, frequency and bit rate).
- SPI DATA: This sub-block is used in Buffered and Packet mode to write and read data bytes to and from the FIFO. (FIFO Interrupts can be used to manage the FIFO content).

Both of these SPIs are configured in Slave mode while the host microcontroller is configured as the master. They have separate selection pins ($\overline{\text{CSCON}}$ and $\overline{\text{CSDAT}}$) but share the remaining pins:

- SCK (SPI Clock): Clock signal provided by the host microcontroller
- SDI (SPI Input): Data Input signal provided by the host microcontroller
- SDO (SPI Output): Data Output signal provided by the MRF89XA

As listed in Table 2-5, only one interface can be selected at a time with $\overline{\text{CSCON}}$ is having the priority:

TABLE 2-5: CONFIG VS. DATA SPI SELECTION

$\overline{\text{CSDAT}}$	$\overline{\text{CSCON}}$	SPI
0	0	CONFIG
0	1	DATA
1	0	CONFIG
1	1	None

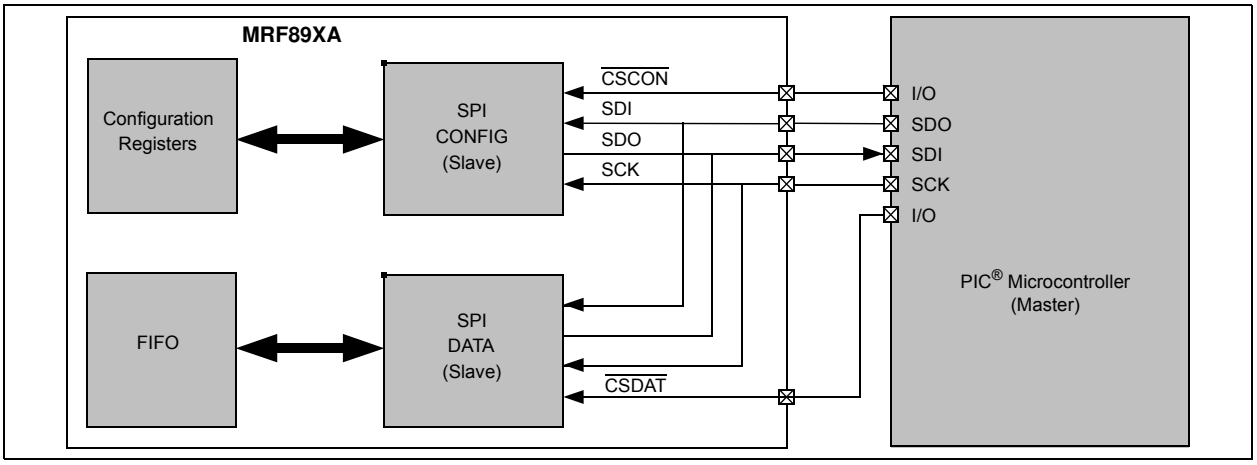
All the parameters can be programmed and set through the SPI module. Any of these auxiliary functions can be disabled when it is not required. After power-on, all parameters are set to default values. The programmed values are retained during Sleep mode. The interface supports the read out of a status register, which provides detailed information about the status of the transceiver and the received data.

The MRF89XA supports SPI mode 0,0, which requires the SCK to remain idle in a low state. The CS pins, $\overline{\text{CSCON}}$ and $\overline{\text{CSDAT}}$ based on the mode (pin 14 and 15), must be held low to enable communication between the host microcontroller and the MRF89XA. The device's timing specification details are listed in Table 5-7. The SDO pin defaults to a high impedance (hi-Z) state when any of the CS pins are high (the MRF89XA is not selected). This pin has a tri-state buffer and uses a bus hold logic.

As the device uses byte writes, any of the Chip Select (CS) pins should be pulled low for 8 bits. Data bits on the SDI pin (pin 17) are shifted into the device upon the rising edge of the clock on the SCK pin (pin 18) whenever the CS pins are low. The maximum clock frequency for the SPI clock for CONFIG mode is 6 MHz. However, maximum SPI Clock for DATA mode (to read/write FIFO) is 1 MHz. Data is received by the transceiver through the SDI pin and is clocked on the rising edge of SCK. The MRF89XA sends the data through the SDO pin and is clocked out on the falling edge of SCK. The Most Significant bit (MSb) is sent first in any data.

The SPI sequence diagrams are illustrated in Figure 2-12 through Figure 2-15.

FIGURE 2-11: SPI OVERVIEW AND HOST MICROCONTROLLER CONNECTIONS

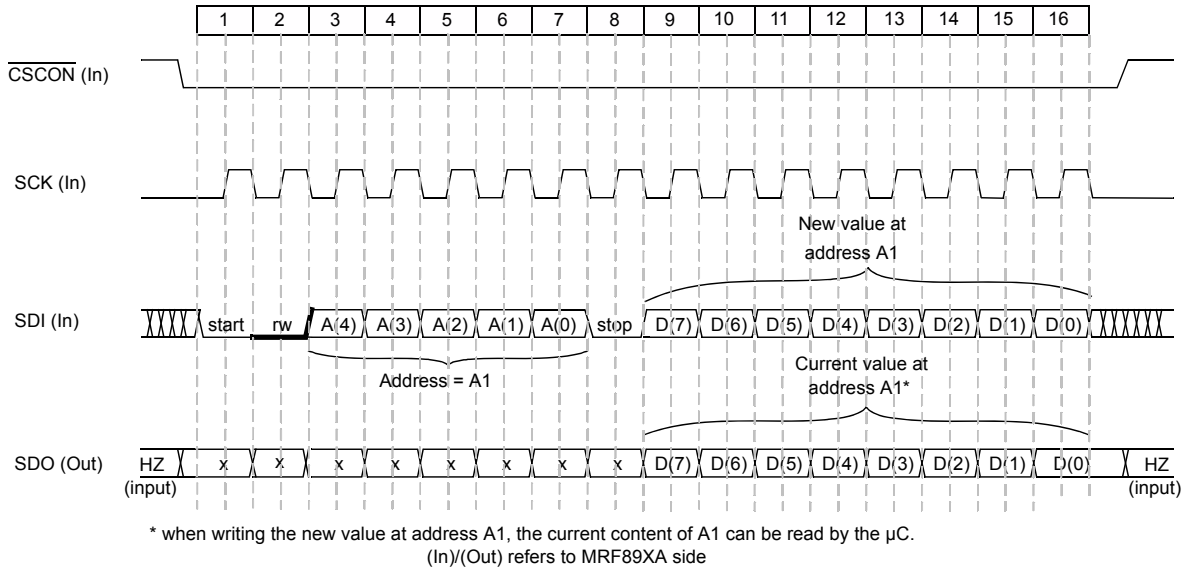


2.11.1 SPI CONFIG

Write Register - To write a value into a Configuration register, the timing diagram illustrated in Figure 2-12 should be followed by the host microcontroller. The new value of the register is effective from the rising edge of CSCON.

Note: When writing more than one register successively, it is not compulsory to toggle CSCON back high between two write sequences. The bytes are alternatively considered as address and value. In this instance, all new values will become effective on rising edge of CSCON.

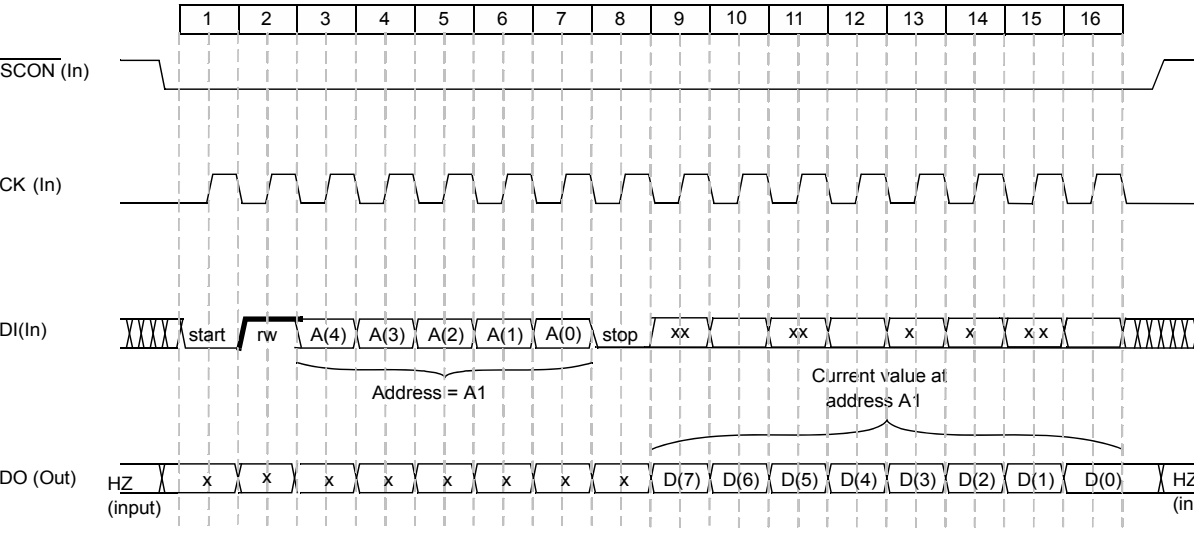
FIGURE 2-12: WRITE REGISTER SEQUENCE



Read Register - To read the value of a Configuration register, the timing diagram illustrated in Figure 2-13 should be followed by the host microcontroller.

Note: When reading more than one register successively, it is not compulsory to toggle CSCON back high between two read sequences. The bytes are alternatively considered as address and value.

FIGURE 2-13: READ REGISTER SEQUENCE

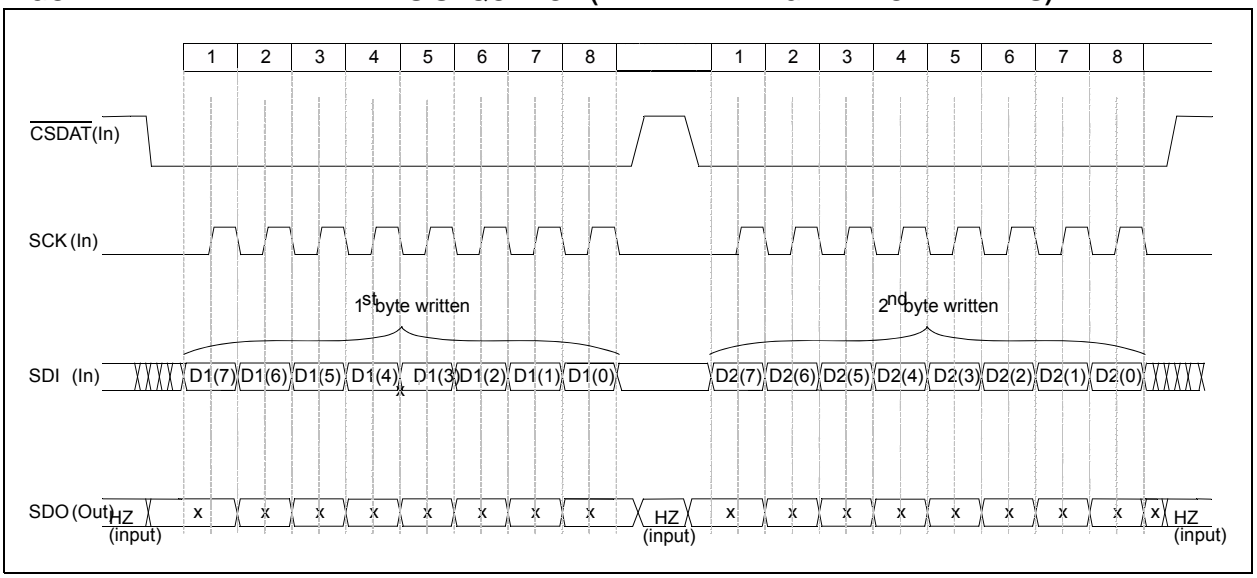


2.11.2 SPI DATA

Write Byte (before/during TX) - To write bytes into the FIFO, the timing diagram illustrated in Figure 2-14 should be followed by the host microcontroller.

Note: It is compulsory to toggle $\overline{\text{CSDAT}}$ back high between each byte written. The byte is pushed into the FIFO on the rising edge of $\overline{\text{CSDAT}}$.

FIGURE 2-14: WRITE BYTES SEQUENCE (EXAMPLE DIAGRAM FOR 2 BYTES)



Read Byte (after/during RX) - To read bytes from the FIFO, the timing diagram illustrated in Figure 2-15 should be followed by the host microcontroller.

Note: It is recommended to toggle $\overline{\text{CSDAT}}$ back high between each byte read.

FIGURE 2-15: READ BYTES SEQUENCE (EXAMPLE DIAGRAM FOR 2 BYTES)