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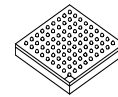
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MSC7110

Low-Cost 16-bit DSP with DDR Controller



MAP-BGA-400
17 mm × 17 mm

- StarCore® SC1400 DSP extended core with one SC1400 DSP core, 64 Kbyte of internal SRAM M1 memory, 16 way 16 Kbyte instruction cache (ICache), four-entry write buffer, programmable interrupt controller (PIC), and low-power Wait and Stop processing modes.
- 8 Kbyte boot ROM.
- AHB-Lite crossbar switch that allows parallel data transfers between four master ports and six slave ports, where each port connects to an AHB-Lite bus; fixed or round robin priority programmable at each slave port; programmable bus parking at each slave port; low power mode.
- Internal PLL generates up to 266 MHz clock for the SC1400 core and up to 133 MHz for the crossbar switch, DMA channels, and other peripherals.
- Clock synthesis module provides predivision of PLL input clock; independent clocking of the internal timers and DDR module; programmable operation in the SC1400 low power Stop mode; independent shutdown of different regions of the device.
- Enhanced 16-bit wide host interface (HDI16) provides a glueless connection to industry-standard microcomputers, microprocessors, and DSPs and can also operate with an 8-bit host data bus, making it fully compatible with the DSP56300 HI08 from the external host side.
- DDR memory controller that supports byte enables for up to a 32-bit data bus; glueless interface to 133 MHz 14-bit page mode DDR-RAM; 14-bit external address bus supporting up to 1 Gbyte; and 16-bit or 32-bit external data bus.
- Programmable memory interface with independent read buffers, programmable predictive read feature for each buffer, and a write buffer.
- System control unit performs software watchdog timer function; includes programmable bus time-out monitors on AHB-Lite slave buses; includes bus error detection and programmable time-out monitors on AHB-Lite master buses; and has address out-of-range detection on each crossbar switch buses.
- Event port collects and counts important signal events including DMA and interrupt requests and trigger events such as interrupts, breakpoints, DMA transfers, or wake-up events; units operate independently, in sequence, or triggered externally; can be used standalone or with the OCE10.
- Multi-channel DMA controller with 32 time-multiplexed unidirectional channels, priority-based time-multiplexing between channels using 32 internal priority levels, fixed- or round-robin-priority operation, major-minor loop structure, and DONE or DRACK protocol from requesting units.
- One TDM module with independent receive and transmit, programmable sharing of frame sync and clock, programmable word size (8 or 16-bit), hardware-base A-law/ μ -law conversion, up to 50 Mbps data rate, up to 128 channels, with glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses.
- UART with full-duplex operation up to 5.0 Mbps.
- Up to 41 general-purpose input/output (GPIO) ports.
- I²C interface that allows booting from EEPROM devices up to 1 Mbyte.
- Two quad timer modules, each with sixteen configurable 16-bit timers.
- fieldBIST™ unit detects and provides visibility into unlikely field failures for systems with high availability to ensure structural integrity, that the device operates at the rated speed, is free from reliability defects, and reports diagnostics for partial or complete device inoperability.
- Standard JTAG interface allows easy integration to system firmware and internal on-chip emulation (OCE10) module.
- Optional booting external host via 8-bit or 16-bit access through the HDI16, I²C, or SPI using in the boot ROM to access serial SPI Flash/EEPROM devices; different clocking options during boot with the PLL on or off using a variety of input frequency ranges.

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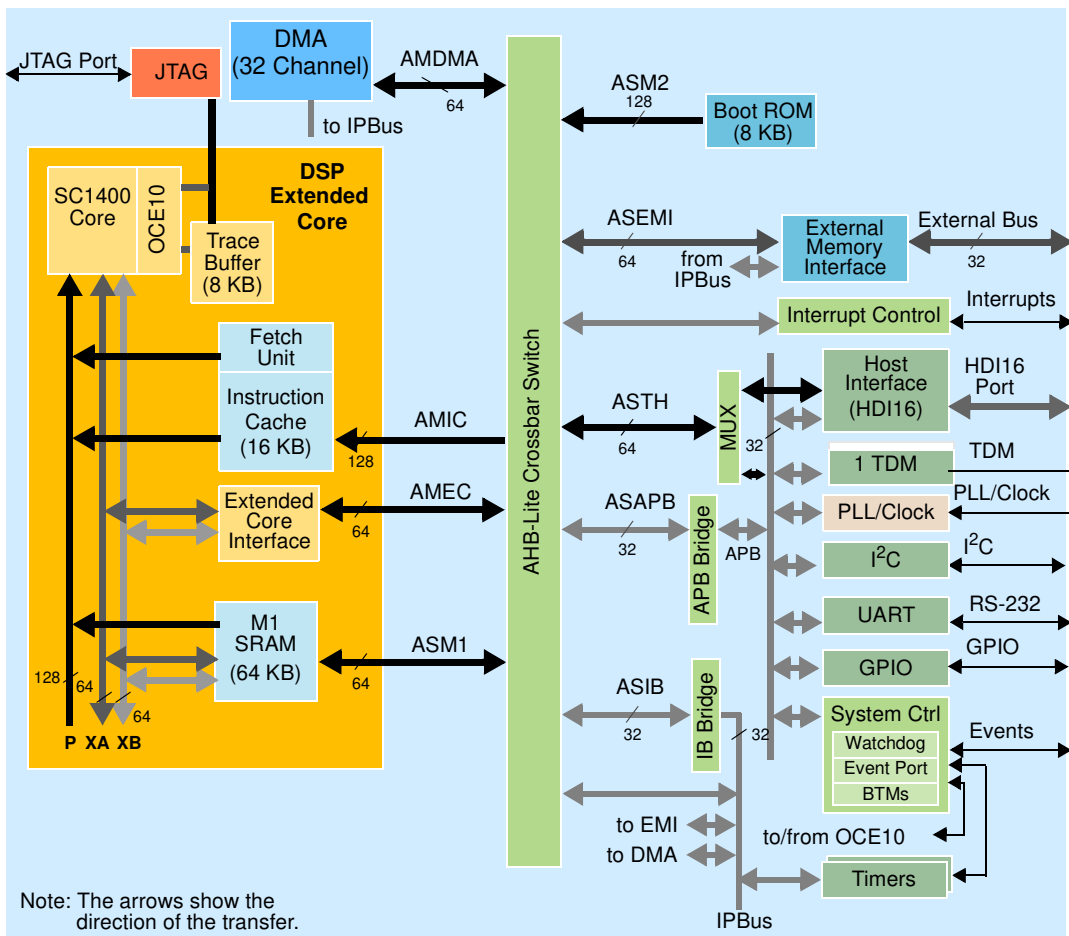


Figure 1. MSC7110 Block Diagram

1 Pin Assignments

This section includes diagrams of the MSC7110 package ball grid array layouts and pinout allocation tables.

1.1 MAP-BGA Ball Layout Diagrams

Top and bottom views of the MAP-BGA package are shown in **Figure 2** and **Figure 3** with their ball location index numbers.

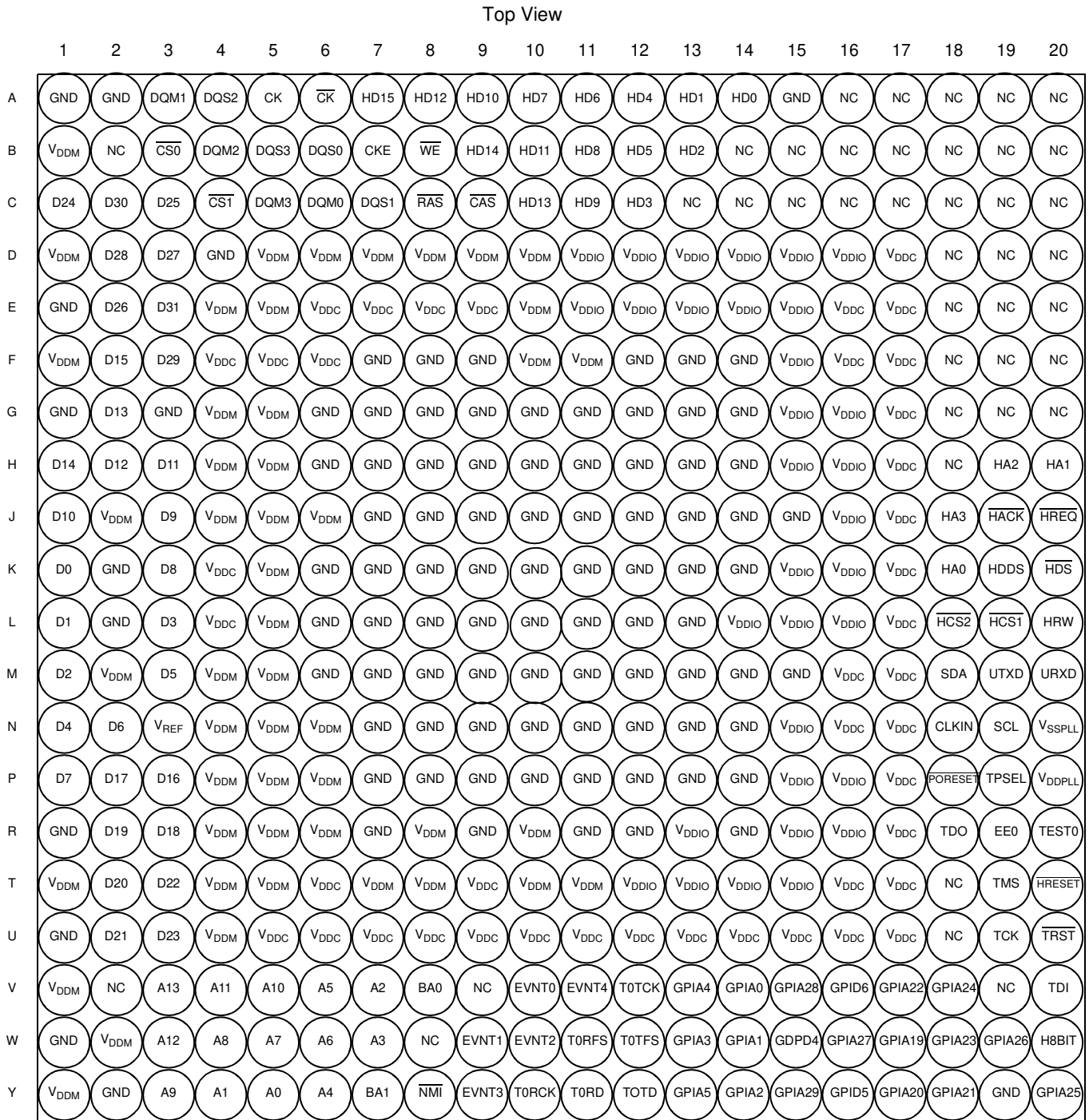


Figure 2. MSC7110 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

Bottom View

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	NC	NC	NC	NC	GND	HD0	HD1	HD4	HD6	HD7	HD10	HD12	HD15	\overline{CK}	CK	DQS2	DQM1	GND	GND
B	NC	NC	NC	NC	NC	NC	NC	HD2	HD5	HD8	HD11	HD14	\overline{WE}	CKE	DQS0	DQS3	DQM2	$\overline{CS0}$	NC	V _{DDM}
C	NC	NC	NC	NC	NC	NC	NC	NC	HD3	HD9	HD13	\overline{CAS}	\overline{RAS}	DQS1	DQM0	DQM3	$\overline{CS1}$	D25	D30	D24
D	NC	NC	NC	V _{DD}	V _{DDIO}	V _{DDIO}	V _{DDIO}	V _{DDIO}	V _{DDIO}	V _{DDIO}	V _{DDM}	V _{DDM}	V _{DDM}	V _{DDM}	V _{DDM}	V _{DDM}	GND	D27	D28	V _{DDM}
E	NC	NC	NC	V _{DD}	V _{DD}	V _{DDIO}	V _{DDIO}	V _{DDIO}	V _{DDIO}	V _{DDIO}	V _{DDM}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DDM}	V _{DDM}	D31	D26	GND
F	NC	NC	NC	V _{DD}	V _{DD}	V _{DDIO}	GND	GND	GND	V _{DDM}	V _{DDM}	GND	GND	GND	V _{DD}	V _{DD}	V _{DD}	D29	D15	V _{DDM}
G	NC	NC	NC	V _{DD}	V _{DDIO}	V _{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V _{DDM}	V _{DDM}	GND	D13	GND
H	HA1	HA2	NC	V _{DD}	V _{DDIO}	V _{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V _{DDM}	V _{DDM}	D11	D12	D14
J	\overline{HREQ}	\overline{HACK}	HA3	V _{DD}	V _{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V _{DDM}	V _{DDM}	V _{DDM}	D9	V _{DDM}	D10
K	HDS	HDDS	HA0	V _{DD}	V _{DDIO}	V _{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V _{DDM}	V _{DD}	D8	GND	D0
L	HRW	HCS1	HCS2	V _{DD}	V _{DDIO}	V _{DDIO}	V _{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V _{DDM}	V _{DD}	D3	GND	D1
M	URXD	UTXD	SDA	V _{DD}	V _{DD}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V _{DDM}	V _{DDM}	D5	V _{DDM}	D2
N	V _{SSPLL}	SCL	CLKIN	V _{DD}	V _{DD}	V _{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V _{DDM}	V _{DDM}	V _{DDM}	V _{REF}	D6	D4
P	V _{DDPLL}	TPSEL	$\overline{PORESET}$	V _{DD}	V _{DDIO}	V _{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V _{DDM}	V _{DDM}	V _{DDM}	D16	D17	D7
R	TEST0	EE0	TDO	V _{DD}	V _{DDIO}	V _{DDIO}	GND	V _{DDIO}	GND	GND	V _{DDM}	GND	V _{DDM}	GND	V _{DDM}	V _{DDM}	V _{DDM}	D18	D19	GND
T	\overline{HRESET}	TMS	NC	V _{DD}	V _{DD}	V _{DDIO}	V _{DDIO}	V _{DDIO}	V _{DDIO}	V _{DDM}	V _{DDM}	V _{DD}	V _{DDM}	V _{DDM}	V _{DD}	V _{DDM}	V _{DDM}	D22	D20	V _{DDM}
U	\overline{TRST}	TCK	NC	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DDM}	D23	D21	GND
V	TDI	NC	GPIA24	GPIA22	GPIA28	GPIA0	GPIA4	T0TCK	EVNT4	EVNT0	NC	BA0	A2	A5	A10	A11	A13	NC	V _{DDM}	
W	H8BIT	GPIA26	GPIA23	GPIA19	GPIA27	GDPD4	GPIA1	GPIA3	T0TFS	T0RFS	EVNT2	EVNT1	NC	A3	A6	A7	A8	A12	V _{DDM}	GND
Y	GPIA25	GND	GPIA21	GPIA20	GPIA5	GPIA29	GPIA2	GPIA5	T0TD	T0RD	T0RCK	EVNT3	\overline{NMI}	BA1	A4	A0	A1	A9	GND	V _{DDM}

Note: The display is for mask set 1L44X. For mask set 1M88B, A16 is BM3 and B15 is BM2.

Figure 3. MSC7110 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

1.2 Signal List By Ball Location

Table 1 lists the signals sorted by ball number and configuration.

Table 1. MSC7110 Signals by Ball Designator

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
A1		GND				
A2		GND				
A3		DQM1				
A4		DQS2				
A5		CK				
A6		\overline{CK}				
A7		GPIC7		GPOC7	HD15	
A8		GPIC4		GPOC4	HD12	
A9		GPIC2		GPOC2	HD10	
A10		reserved			HD7	
A11		reserved			HD6	
A12		reserved			HD4	
A13		reserved			HD1	
A14		reserved			HD0	
A15		GND				
A16 (1L44X)		NC				
A16 (1M88B)	BM3	GPID8		GPOD7	reserved	
A17		NC				
A18		NC				
A19		NC				
A20		NC				
B1		V_{DDM}				
B2		NC				
B3		$\overline{CS0}$				
B4		DQM2				
B5		DQS3				
B6		DQS0				
B7		CKE				
B8		\overline{WE}				
B9		GPIC6		GPOC6	HD14	
B10		GPIC3		GPOC3	HD11	
B11		GPIC0		GPOC0	HD8	
B12		reserved			HD5	
B13		reserved			HD2	
B14		NC				
B15 (1L44X)		NC				

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
B15 (1M88B)	BM2	GPID7		GPOD7	reserved	
B16		NC				
B17		NC				
B18		NC				
B19		NC				
B20		NC				
C1		D24				
C2		D30				
C3		D25				
C4		$\overline{CS1}$				
C5		DQM3				
C6		DQM0				
C7		DQS1				
C8		\overline{RAS}				
C9		\overline{CAS}				
C10		GPIC5		GPOC5	HD13	
C11		GPIC1		GPOC1	HD9	
C12		reserved			HD3	
C13		NC				
C14		NC				
C15		NC				
C16		NC				
C17		NC				
C18		NC				
C19		NC				
C20		NC				
D1		V_{DDM}				
D2		D28				
D3		D27				
D4		GND				
D5		V_{DDM}				
D6		V_{DDM}				
D7		V_{DDM}				
D8		V_{DDM}				
D9		V_{DDM}				
D10		V_{DDM}				
D11		V_{DDIO}				
D12		V_{DDIO}				

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D13						V _{DDIO}
D14						V _{DDIO}
D15						V _{DDIO}
D16						V _{DDIO}
D17						V _{DDC}
D18						NC
D19						NC
D20						NC
E1						GND
E2						D26
E3						D31
E4						V _{DDM}
E5						V _{DDM}
E6						V _{DDC}
E7						V _{DDC}
E8						V _{DDC}
E9						V _{DDC}
E10						V _{DDM}
E11						V _{DDIO}
E12						V _{DDIO}
E13						V _{DDIO}
E14						V _{DDIO}
E15						V _{DDIO}
E16						V _{DDC}
E17						V _{DDC}
E18						NC
E19						NC
E20						NC
F1						V _{DDM}
F2						D15
F3						D29
F4						V _{DDC}
F5						V _{DDC}
F6						V _{DDC}
F7						GND
F8						GND
F9						GND
F10						V _{DDM}

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
F11						V _{DDM}
F12						GND
F13						GND
F14						GND
F15						V _{DDIO}
F16						V _{DDC}
F17						V _{DDC}
F18						NC
F19						NC
F20						NC
G1						GND
G2						D13
G3						GND
G4						V _{DDM}
G5						V _{DDM}
G6						GND
G7						GND
G8						GND
G9						GND
G10						GND
G11						GND
G12						GND
G13						GND
G14						GND
G15						V _{DDIO}
G16						V _{DDIO}
G17						V _{DDC}
G18						NC
G19						NC
G20						NC
H1						D14
H2						D12
H3						D11
H4						V _{DDM}
H5						V _{DDM}
H6						GND
H7						GND
H8						GND

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
H9						GND
H10						GND
H11						GND
H12						GND
H13						GND
H14						GND
H15						V _{DDIO}
H16						V _{DDIO}
H17						V _{DDC}
H18						NC
H19			reserved			HA2
H20			reserved			HA1
J1						D10
J2						V _{DDM}
J3						D9
J4						V _{DDM}
J5						V _{DDM}
J6						V _{DDM}
J7						GND
J8						GND
J9						GND
J10						GND
J11						GND
J12						GND
J13						GND
J14						GND
J15						GND
J16						V _{DDIO}
J17						V _{DDC}
J18 (1L44X)			reserved			HA3
J18 (1M88B)			GPIC11		GPOC11	HA3
J19			reserved			$\overline{\text{HACK}}/\text{HACK}$ or $\overline{\text{HRRQ}}/\text{HRRQ}$
J20	HDSP		reserved			$\overline{\text{HREQ}}/\text{HREQ}$ or $\overline{\text{HTRQ}}/\text{HTRQ}$
K1						D0
K2						GND
K3						D8
K4						V _{DDC}
K5						V _{DDM}

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
K6						GND
K7						GND
K8						GND
K9						GND
K10						GND
K11						GND
K12						GND
K13						GND
K14						GND
K15						V _{DDIO}
K16						V _{DDIO}
K17						V _{DCC}
K18		reserved				HA0
K19		reserved				HDDS
K20		reserved				$\overline{\text{HDS}}/\text{HDS}$ or $\overline{\text{HWR}}/\text{HWR}$
L1						D1
L2						GND
L3						D3
L4						V _{DCC}
L5						V _{DDM}
L6						GND
L7						GND
L8						GND
L9						GND
L10						GND
L11						GND
L12						GND
L13						GND
L14						V _{DDIO}
L15						V _{DDIO}
L16						V _{DDIO}
L17						V _{DCC}
L18 (1L44X)		reserved				$\overline{\text{HCS2}}/\text{HCS2}$
L18 (1M88B)		GPIB11		GPOB11		$\overline{\text{HCS2}}/\text{HCS2}$
L19		reserved				$\overline{\text{HCS1}}/\text{HCS1}$
L20		reserved				HRW or $\overline{\text{HRD}}/\text{HRD}$
M1						D2
M2						V _{DDM}

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
M3					D5	
M4					V _{DDM}	
M5					V _{DDM}	
M6					GND	
M7					GND	
M8					GND	
M9					GND	
M10					GND	
M11					GND	
M12					GND	
M13					GND	
M14					GND	
M15					GND	
M16					V _{DDC}	
M17					V _{DDC}	
M18		GPIA14	$\overline{\text{IRQ15}}$	GPOA14		SDA
M19		GPIA12	$\overline{\text{IRQ3}}$	GPOA12		UTXD
M20		GPIA13	$\overline{\text{IRQ2}}$	GPOA13		URXD
N1					D4	
N2					D6	
N3					V _{REF}	
N4					V _{DDM}	
N5					V _{DDM}	
N6					V _{DDM}	
N7					GND	
N8					GND	
N9					GND	
N10					GND	
N11					GND	
N12					GND	
N13					GND	
N14					GND	
N15					V _{DDIO}	
N16					V _{DDC}	
N17					V _{DDC}	
N18					CLKIN	
N19		GPIA15	$\overline{\text{IRQ14}}$	GPOA15		SCL
N20					V _{SSPLL}	

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
P1					D7	
P2					D17	
P3					D16	
P4					V _{DDM}	
P5					V _{DDM}	
P6					V _{DDM}	
P7					GND	
P8					GND	
P9					GND	
P10					GND	
P11					GND	
P12					GND	
P13					GND	
P14					GND	
P15					V _{DDIO}	
P16					V _{DDIO}	
P17					V _{DDC}	
P18					$\overline{\text{PORESET}}$	
P19					TPSEL	
P20					V _{DDPLL}	
R1					GND	
R2					D19	
R3					D18	
R4					V _{DDM}	
R5					V _{DDM}	
R6					V _{DDM}	
R7					GND	
R8					V _{DDM}	
R9					GND	
R10					V _{DDM}	
R11					GND	
R12					GND	
R13					V _{DDIO}	
R14					GND	
R15					V _{DDIO}	
R16					V _{DDIO}	
R17					V _{DDC}	
R18					TDO	

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
R19	reserved			EE0/DBREQ		
R20	TEST0					
T1	V _{DDM}					
T2	D20					
T3	D22					
T4	V _{DDM}					
T5	V _{DDM}					
T6	V _{DDC}					
T7	V _{DDM}					
T8	V _{DDM}					
T9	V _{DDC}					
T10	V _{DDM}					
T11	V _{DDM}					
T12	V _{DDIO}					
T13	V _{DDIO}					
T14	V _{DDIO}					
T15	V _{DDIO}					
T16	V _{DDC}					
T17	V _{DDC}					
T18	NC					
T19	TMS					
T20	HRESET					
U1	GND					
U2	D21					
U3	D23					
U4	V _{DDM}					
U5	V _{DDC}					
U6	V _{DDC}					
U7	V _{DDC}					
U8	V _{DDC}					
U9	V _{DDC}					
U10	V _{DDC}					
U11	V _{DDC}					
U12	V _{DDC}					
U13	V _{DDC}					
U14	V _{DDC}					
U15	V _{DDC}					
U16	V _{DDC}					

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
U17	V _{DDC}					
U18	NC					
U19	TCK					
U20	$\overline{\text{TRST}}$					
V1	V _{DDM}					
V2	NC					
V3	A13					
V4	A11					
V5	A10					
V6	A5					
V7	A2					
V8	BA0					
V9	NC					
V10	reserved				EVNT0	
V11	SWTE	GPIA16	$\overline{\text{IRQ12}}$	GPOA16	EVNT4	
V12	GPIA8		$\overline{\text{IRQ6}}$	GPOA8	T0TCK	
V13	GPIA4		$\overline{\text{IRQ1}}$	GPOA4	reserved	
V14	GPIA0		$\overline{\text{IRQ11}}$	GPOA0	reserved	
V15	GPIA28		$\overline{\text{IRQ17}}$	GPOA28	reserved	reserved
V16	GPID6			GPOD6	reserved	reserved
V17	GPIA22		$\overline{\text{IRQ22}}$	GPOA22	reserved	
V18	GPIA24		$\overline{\text{IRQ24}}$	GPOA24	reserved	
V19	NC					
V20	TDI					
W1	GND					
W2	V _{DDM}					
W3	A12					
W4	A8					
W5	A7					
W6	A6					
W7	A3					
W8	NC					
W9	GPIA17		$\overline{\text{IRQ13}}$	GPOA17	EVNT1	CLKO
W10	BM0	GPIC14		GPOC14	EVNT2	
W11	GPIA10		$\overline{\text{IRQ5}}$	GPOA10	T0RFS	
W12	GPIA7		$\overline{\text{IRQ7}}$	GPOA7	T0TFS	
W13	GPIA3		$\overline{\text{IRQ8}}$	GPOA3	reserved	
W14	GPIA1		$\overline{\text{IRQ10}}$	GPOA1	reserved	

Table 1. MSC7110 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
W15	GPID4			GPOD4	reserved	reserved
W16	GPIA27		$\overline{\text{IRQ18}}$	GPOA27	reserved	reserved
W17	GPIA19		$\overline{\text{IRQ19}}$	GPOA19	reserved	
W18	GPIA23		$\overline{\text{IRQ23}}$	GPOA23	reserved	
W19	GPIA26		$\overline{\text{IRQ26}}$	GPOA26	reserved	
W20	H8BIT	reserved				
Y1	V _{DDM}					
Y2	GND					
Y3	A9					
Y4	A1					
Y5	A0					
Y6	A4					
Y7	BA1					
Y8	reserved		$\overline{\text{NMI}}$	reserved		
Y9	BM1	GPIC15		GPOC15	EVNT3	
Y10	GPIA11		$\overline{\text{IRQ4}}$	GPOA11	TORCK	
Y11	GPIA9			GPOA9	TORRD	
Y12	GPIA6			GPOA6	TOTD	
Y13	GPIA5		$\overline{\text{IRQ0}}$	GPOA5	reserved	
Y14	GPIA2		$\overline{\text{IRQ9}}$	GPOA2	reserved	
Y15	GPIA29		$\overline{\text{IRQ16}}$	GPOA29	reserved	reserved
Y16	GPID5			GPOD5	reserved	reserved
Y17	GPIA20		$\overline{\text{IRQ20}}$	GPOA20	reserved	
Y18	GPIA21		$\overline{\text{IRQ21}}$	GPOA21	reserved	
Y19	GND					
Y20	GPIA25		$\overline{\text{IRQ25}}$	GPOA25	reserved	

2 Specifications

This chapter covers power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC711x Reference Manual*.

Note: The MSC7110 electrical specifications are preliminary and many are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after thorough characterization and device qualifications have been completed.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC7110.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.5	V
Memory supply voltage	V_{DDM}	4.0	V
PLL supply voltage	V_{DDPLL}	1.5	V
I/O supply voltage	V_{DDIO}	-0.2 to 4.0	V
Input voltage	V_{IN}	(GND - 0.2) to 4.0	V
Reference voltage	V_{REF}	4.0	V
Maximum operating temperature	T_J	105	°C
Minimum operating temperature	T_A	-40	°C
Storage temperature range	T_{STG}	-55 to +150	°C
Notes: <ol style="list-style-type: none"> Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage. Section 3.1, Thermal Design Considerations includes a formula for computing the chip junction temperature (T_J). 			

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.14 to 1.26	V
Memory supply voltage	V_{DDM}	2.38 to 2.63	V
PLL supply voltage	V_{DDPLL}	1.14 to 1.26	V
I/O supply voltage	V_{DDIO}	3.14 to 3.47	V
Reference voltage	V_{REF}	1.19 to 1.31	V
Operating temperature range	T_J T_A	maximum: 105 minimum: -40	°C °C

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC7110 for the MAP-BGA package.

Table 4. Thermal Characteristics for MAP-BGA Package

Characteristic	Symbol	MAP-BGA 17 × 17 mm ⁵		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient ^{1, 2}	$R_{\theta JA}$	39	31	°C/W
Junction-to-ambient, four-layer board ^{1, 3}	$R_{\theta JA}$	23	20	°C/W
Junction-to-board ⁴	$R_{\theta JB}$	12		°C/W
Junction-to-case ⁵	$R_{\theta JC}$	7		°C/W
Junction-to-package-top ⁶	Ψ_{JT}	2		°C/W
Notes: <ol style="list-style-type: none"> Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal. Per JEDEC JESD51-6 with the board horizontal. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. 				

Section 3.1, *Thermal Design Considerations* explains these characteristics in detail.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC7110.

Note: The leakage current is measured for nominal voltage values must vary in the same direction (for example, both V_{DDIO} and V_{DDC} vary by +2 percent or both vary by -2 percent).

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Core and PLL voltage	V_{DDC} V_{DDPLL}	1.14	1.2	1.26	V
DRAM interface I/O voltage ¹	V_{DDM}	2.375	2.5	2.625	V
I/O voltage	V_{DDIO}	3.135	3.3	3.465	V
DRAM interface I/O reference voltage ²	V_{REF}	$0.49 \times V_{DDM}$	1.25	$0.51 \times V_{DDM}$	V
DRAM interface I/O termination voltage ³	V_{TT}	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Input high CLKIN voltage	V_{IHCLK}	2.4	3.0	3.465	V
DRAM interface input high I/O voltage	V_{IHM}	$V_{REF} + 0.28$	V_{DDM}	$V_{DDM} + 0.3$	V
DRAM interface input low I/O voltage	V_{ILM}	-0.3	GND	$V_{REF} - 0.18$	V
Input leakage current, $V_{IN} = V_{DDIO}$	I_{IN}	-1.0	0.09	1	μ A
V_{REF} input leakage current	I_{VREF}	—	—	5	μ A
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDIO}$	I_{OZ}	-1.0	0.09	1	μ A
Signal low input current, $V_{IL} = 0.4$ V	I_L	-1.0	0.09	1	μ A
Signal high input current, $V_{IH} = 2.0$ V	I_H	-1.0	0.09	1	μ A
Output high voltage, $I_{OH} = -2$ mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, $I_{OL} = 5$ mA	V_{OL}	—	0	0.4	V
Typical core power ⁵ • at 200 MHz • at 266 MHz (mask set 1M88B only)	P_C	— —	222 293	— —	mW mW
Notes: <ol style="list-style-type: none"> The value of V_{DDM} at the MSC7110 device must remain within 50 mV of V_{DDM} at the DRAM device at all times. V_{REF} must be equal to 50% of V_{DDM} and track V_{DDM} variations as measured at the receiver. Peak-to-peak noise must not exceed $\pm 2\%$ of the DC value. V_{TT} is not applied directly to the MSC7110 device. It is the level measured at the far end signal termination. It should be equal to V_{REF}. This rail should track variations in the DC level of V_{REF}. Output leakage for the memory interface is measured with all outputs disabled, $0 \text{ V} \leq V_{OUT} \leq V_{DDM}$. The core power values were measured using a standard EFR pattern at typical conditions (25°C, 200 MHz or 266 MHz, 1.2 V core). 					

Table 6 lists the DDR DRAM capacitance.

Table 6. DDR DRAM Capacitance

Parameter/Condition	Symbol	Max	Unit
Input/output capacitance: DQ, DQS	C_{IO}	30	pF
Delta input/output capacitance: DQ, DQS	C_{DIO}	30	pF
Note: These values were measured under the following conditions: <ul style="list-style-type: none"> $V_{DDM} = 2.5 \text{ V} \pm 0.125 \text{ V}$ $f = 1 \text{ MHz}$ $T_A = 25^\circ\text{C}$ $V_{OUT} = V_{DDM}/2$ V_{OUT} (peak to peak) = 0.2 V 			

2.5 AC Timings

This section presents timing diagrams and specifications for individual signals and parallel I/O outputs and inputs. All AC timings are based on a 30 pF load, except where noted otherwise, and a 50 Ω transmission line. For any additional pF, use the following equations to compute the delay:

- Standard interface: $2.45 + (0.054 \times C_{load})$ ns
- DDR interface: $1.6 + (0.002 \times C_{load})$ ns

2.5.1 Clock and Timing Signals

The following tables describe clock signal characteristics. **Table 7** shows the maximum frequency values for internal (core, reference, and peripherals) and external (CLKO) clocks. You must ensure that maximum frequency values are not exceeded (see for the allowable ranges when using the PLL).

Table 7. Maximum Frequencies

Characteristic	Maximum in MHz	
	Mask Set 1L44X	Mask Set 1M88B
Core clock frequency (CLOCK)	200	266
External output clock frequency (CLKO)	50	67
Memory clock frequency (CK, \overline{CK})	100	133
TDM clock frequency (TxRCK, TxTCK)	50	67

Table 8. Clock Frequencies in MHz

Characteristic	Symbol	Min	Max	
			Mask Set 1L44X	Mask Set 1M88B
CLKIN frequency	F _{CLKIN}	10	100	100
CLOCK frequency	F _{CORE}	—	200	266
CK, \overline{CK} frequency	F _{CK}	—	100	133
TDMxRCK, TDMxTCK frequency	F _{TDMCK}	—	50	50
CLKO frequency	F _{CKO}	—	50	67
AHB/IPBus/APB clock frequency	F _{BCK}	—	100	133

Note: The rise and fall time of external clocks should be 5 ns maximum

Table 9. System Clock Parameters

Characteristic	Min	Max	Unit
CLKIN frequency	10	100	MHz
CLKIN slope	—	5	ns
CLKIN frequency jitter (peak-to-peak)	—	1000	ps
CLKO frequency jitter (peak-to-peak)	—	150	ps

2.5.2 Configuring Clock Frequencies

This section describes important requirements for configuring clock frequencies in the MSC7110 device when using the PLL block. To configure the device clocking, you must program four fields in the Clock Control Register (CLKCTL):

- PLLDVF field. Specifies the PLL division factor. The output of the divider block is the input to the multiplier block.
- PLLMLTF field. Specifies the PLL multiplication factor. The output from the multiplier block is the VCO.
- RNG field. Selects the available PLL frequency range.
- CKSEL field. Selects the source for the core clock.

There are restrictions on the frequency range permitted at the beginning of the multiplication portion of the PLL that affect the allowable values for the PLLDVF and PLLMLTF fields. The following sections define these restrictions and provide guidelines to configure the device clocking when using the PLL. Refer to the Clock and Power Management chapter in the *MSC711x Reference Manual* for details on the clock programming model.

2.5.2.1 PLL Multiplier Restrictions

There are two restrictions for correct usage of the PLL block:

- The input frequency to the PLL multiplier block (that is, the output of the divider) must be in the range 10.5–19.5 MHz.
- The output frequency of the PLL multiplier must be in the range 300–600 MHz.

When programming the PLL for a desired output frequency using the PLLDVF, PLLMLTF, and RNG fields, you must meet these constraints.

2.5.2.2 Division Factors and Corresponding CLKIN Frequency Range

The value of the PLLDVF field determines the allowable CLKIN frequency range, as shown in **Table 10**.

Table 10. CLKIN Frequency Ranges by Divide Factor Value

PLLDVF Field Value	Divide Factor	CLKIN Frequency Range	Comments
0x00	1	10.5 to 19.5 MHz	Pre-Division by 1
0x01	2	21 to 39 MHz	Pre-Division by 2
0x02	3	31.5 to 58.5 MHz	Pre-Division by 3
0x03	4	42 to 78 MHz	Pre-Division by 4
0x04	5	52.5 to 97.5 MHz	Pre-Division by 5
0x05	6	63 to 100 MHz	Pre-Division by 6
0x06	7	73.5 to 100 MHz	Pre-Division by 7
0x07	8	84 to 100 MHz	Pre-Division by 8
0x08	9	94.5 to 100 MHz	Pre-Division by 9

Note: The maximum CLKIN frequency is 100 MHz. Therefore, the PLLDVF value must be in the range from 1–9.

2.5.2.3 Multiplication Factor Range

The multiplier block output frequency ranges depend on the input clock frequency as shown in **Table 11**.

Table 11. PLLMLTF Ranges

Multiplier Block (Loop) Output Range	Minimum PLLMLTF Value	Maximum PLLMLTF Value
$300 \leq [\text{Pre-Divided Clock} \times (\text{PLLMLTF} + 1)] \leq 600 \text{ MHz}$	300/Pre-Divided Clock	600/Pre-Divided Clock

Note: This table results from the allowed range for F_{Loop} . The minimum and maximum multiplication factors are dependent on the frequency of the Pre-Divided Clock.

2.5.2.4 Allowed Core Clock Frequency Range

The frequency delivered to the core, extended core, and peripheral depends on the value of the CLKCTRL[RNG] bit as shown in **Table 12**.

Table 12. F_{VCO} Frequency Ranges

CLKCTRL[RNG] Value	Allowed Range of F_{VCO}
1	$300 \leq F_{\text{VCO}} \leq 600 \text{ MHz}$
0	$150 \leq F_{\text{VCO}} \leq 300 \text{ MHz}$

Note: This table results from the allowed range for F_{VCO} , which is F_{Loop} modified by CLKCTRL[RNG].

This bit along with the CKSEL determines the frequency range of the core clock.

Table 13. Resulting Ranges Permitted for the Core Clock

CLKCTRL[CKSEL]	CLKCTRL[RNG]	Resulting Division Factor	Allowed Range of Core Clock	Comments
11	1	1	Reserved	Reserved
11	0	2	$150 \leq \text{Core_Clk} \leq 200 \text{ MHz}$	Limited by range of PLL
01	1	2	$150 \leq \text{Core_Clk} \leq 200 \text{ MHz}$	Limited by range of PLL
01	0	4	$75 \leq \text{Core_Clk} \leq 150 \text{ MHz}$	Limited by range of PLL

Note: This table results from the allowed range for F_{OUT} , which depends on clock selected via CLKCTRL[CKSEL].

2.5.2.5 Core Clock Frequency Range When Using DDR Memory

The core clock can also be limited by the frequency range of the DDR devices in the system. **Table 14** summarizes this restriction.

Table 14. Core Clock Ranges When Using DDR

DDR Type	Allowed Frequency Range for DDR CK	Corresponding Range for the Core Clock	Comments
DDR 200 (PC-1600)	83–100 MHz	$166 \leq \text{core clock} \leq 200 \text{ MHz}$	Core limited to $2 \times$ maximum DDR frequency
DDR 266 (PC-2100)	83–133 MHz	$166 \leq \text{core clock} \leq 266 \text{ MHz}$	Core limited to $2 \times$ maximum DDR frequency
DDR 333 (PC-2600)	83–150 MHz	$166 \leq \text{core clock} \leq 300 \text{ MHz}$	Core limited to $2 \times$ maximum DDR frequency

2.5.3 Reset Timing

The MSC7110 device has several inputs to the reset logic. All MSC7110 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 15** describes the reset sources.

Table 15. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC7110 and configures various attributes of the MSC7110. On PORESET, the entire MSC7110 device is reset. SPL and DLL states are reset, HRESET is driven, the SC1400 extended core is reset, and system configuration is sampled. The system is configured only when PORESET is asserted.
External Hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC7110. While HRESET is asserted, HRESET is an open-drain output. Upon hard reset, HRESET is driven and the SC1400 extended core is reset.
Software watchdog reset	Internal	When the MSC7110 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC7110 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
JTAG EXTEST, CLAMP, or HIGHZ command	Internal	When a Test Access Port (TAP) executes an EXTEST, CLAMP, or HIGHZ command, the TAP logic asserts an internal reset signal that generates an internal soft reset sequence.

Table 16 summarizes the reset actions that occur as a result of the different reset sources.

Table 16. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)
	External only	External or Internal (Software Watchdog or Bus Monitor)	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (refer to Section 2.5.3.1 for details).	Yes	No	No
PLL and clock synthesis states Reset	Yes	No	No
HRESET Driven	Yes	Yes	No
Software watchdog and bus time-out monitor registers	Yes	Yes	Yes
Clock synthesis modules (STOPCTRL, HLTREQ, and HLTACK) reset	Yes	Yes	Yes
Extended core reset	Yes	Yes	Yes
Peripheral modules reset	Yes	Yes	Yes

2.5.3.1 Power-On Reset (PORESET) Pin

Asserting $\overline{\text{PORESET}}$ initiates the power-on reset flow. $\overline{\text{PORESET}}$ must be asserted externally for at least 16 CLKIN cycles after external power to the MSC7110 reaches at least $2/3 V_{DD}$.

2.5.3.2 Reset Configuration

The MSC7110 has two mechanisms for writing the reset configuration:

- From a host through the host interface (HDI16)
- From memory through the I²C interface

Five signal levels (see **Chapter 1** for signal description details) are sampled on $\overline{\text{PORESET}}$ deassertion to define the boot and operating conditions:

- BM[0–1]
- SWTE
- H8BIT
- HDSP

2.5.3.3 Reset Timing Tables

Table 17 and **Figure 4** describe the reset timing for a reset configuration write.

Table 17. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Unit
1	Required external $\overline{\text{PORESET}}$ duration minimum	$16/F_{\text{CLKIN}}$	clocks
2	Delay from $\overline{\text{PORESET}}$ deassertion to $\overline{\text{HRESET}}$ deassertion	$521/F_{\text{CLKIN}}$	clocks
Note: Timings are not tested, but are guaranteed by design.			

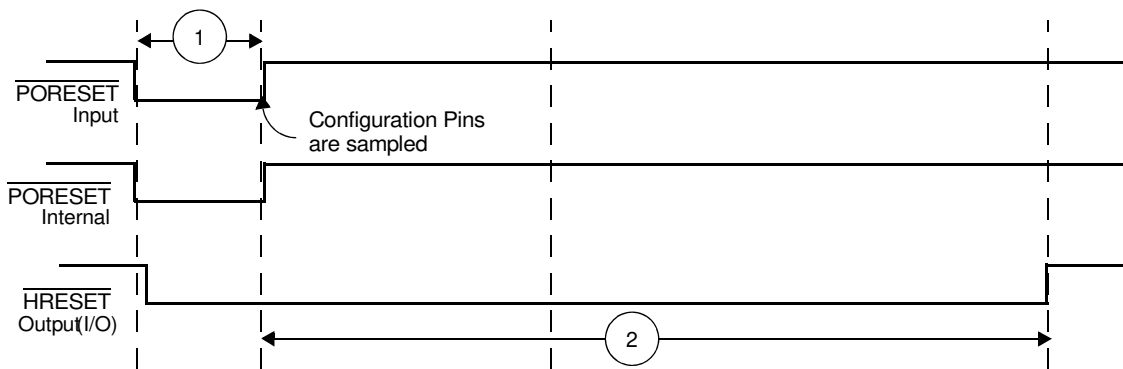


Figure 4. Timing Diagram for a Reset Configuration Write

2.5.4 DDR DRAM Controller Timing

This section provides the AC electrical characteristics for the DDR DRAM interface.

2.5.4.1 DDR DRAM Input AC Timing Specifications

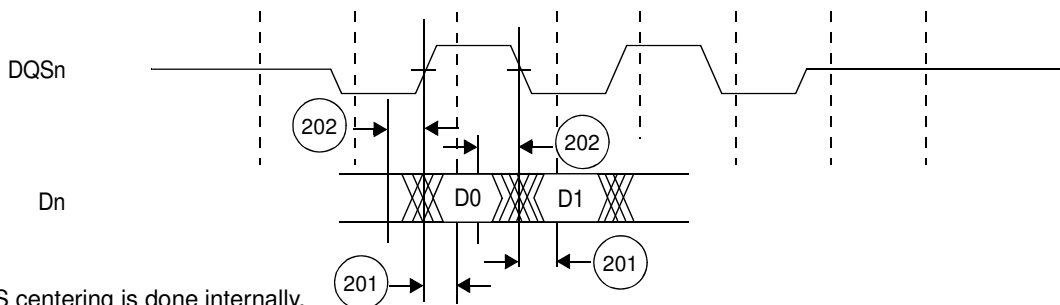
Table 18 provides the input AC timing specifications for the DDR DRAM interface.

Table 18. DDR DRAM Input AC Timing

No.	Parameter	Symbol	Min	Max		Unit
				Mask Set 1L44X	Mask Set 1M88B	
—	AC input low voltage	V_{IL}	—	$V_{REF} - 0.31$	$V_{REF} - 0.31$	V
—	AC input high voltage	V_{IH}	$V_{REF} + 0.31$	$V_{DDM} + 0.3$	$V_{DDM} + 0.3$	V
201	Maximum Dn input setup skew relative to DQSn input	—	—	1026	900	ps
202	Maximum Dn input hold skew relative to DQSn input	—	—	386	900	ps

Notes:

1. Maximum possible skew between a data strobe (DQSn) and any corresponding bit of data (D[8n + {0...7}]) if $0 \leq n \leq 7$.
2. See Table 19 for t_{CK} value.
3. Dn should be driven at the same time as DQSn. This is necessary because the DQSn centering on the DQn data tenure is done internally.



Note: DQS centering is done internally.

Figure 5. DDR DRAM Input Timing Diagram

2.5.4.2 DDR DRAM Output AC Timing Specifications

Table 19 and Table 20 list the output AC timing specifications and measurement conditions for the DDR DRAM interface.

Table 19. DDR DRAM Output AC Timing

No.	Parameter	Symbol	Min		Max	Unit
			Mask Set 1L44X	Mask Set 1M88B		
200	CK cycle time, (CK/ $\overline{\text{CK}}$ crossing) ¹ • 100 MHz (DDR200) • 133 MHz (DDR266)	t_{CK}	10 Not applicable	1.0 7.52	— —	ns ns
204	$\text{An}/\overline{\text{RAS}}/\overline{\text{CAS}}/\overline{\text{WE}}/\text{CKE}$ output setup with respect to CK	t_{DDKHAS}	$0.5 \times t_{\text{CK}} - 2250$	$0.5 \times t_{\text{CK}} - 1000$	—	ps
205	$\text{An}/\overline{\text{RAS}}/\overline{\text{CAS}}/\overline{\text{WE}}/\text{CKE}$ output hold with respect to CK	t_{DDKHAX}	$0.5 \times t_{\text{CK}} - 1250$	$0.5 \times t_{\text{CK}} - 1000$	—	ps
206	$\overline{\text{CSn}}$ output setup with respect to CK	t_{DDKHCS}	$0.5 \times t_{\text{CK}} - 2250$	$0.5 \times t_{\text{CK}} - 1000$	—	ps
207	$\overline{\text{CSn}}$ output hold with respect to CK	t_{DDKHCSX}	$0.5 \times t_{\text{CK}} - 1250$	$0.5 \times t_{\text{CK}} - 1000$	—	ps
208	CK to DQSn ²	t_{DDKMHM}	–600	–600	600	ps
209	Dn/DQMn output setup with respect to DQSn ³	$t_{\text{DDKHDS}},$ t_{DDKLDS}	$0.25 \times t_{\text{MCK}} -$ 1050	$0.25 \times t_{\text{CK}} - 750$	—	ps
210	Dn/DQMn output hold with respect to DQSn ³	$t_{\text{DDKHDX}},$ t_{DDKLDX}	$0.25 \times t_{\text{CK}} - 1050$	$0.25 \times t_{\text{CK}} - 750$	—	ps
211	DQSn preamble start ⁴	t_{DDKHMP}	$-0.25 \times t_{\text{CK}}$	$-0.25 \times t_{\text{CK}}$	—	ps
212	DQSn epilogue end ⁵	t_{DDKHME}	–600	–600	600	ps

Notes:

- All CK/ $\overline{\text{CK}}$ referenced measurements are made from the crossing of the two signals ± 0.1 V.
- t_{DDKMHM} can be modified through the TCFG2[WRDD] DQSS override bits. The DRAM requires that the first write data strobe arrives 75–125% of a DRAM cycle after the write command is issued. Any skew between DQSn and CK must be considered when trying to achieve this 75%–125% goal. The TCFG2[WRDD] bits can be used to shift DQSn by 1/4 DRAM cycle increments. The skew in this case refers to an internal skew existing at the signal connections. By default, the CK/ $\overline{\text{CK}}$ crossing occurs in the middle of the control signal ($\text{An}/\overline{\text{RAS}}/\overline{\text{CAS}}/\overline{\text{WE}}/\text{CKE}$) tenure. Setting TCFG2[ACSM] bit shifts the control signal assertion 1/2 DRAM cycle earlier than the default timing. This means that the signal is asserted no earlier than 410 ps before the CK/ $\overline{\text{CK}}$ crossing and no later than 677 ps after the crossing time; the device uses 1087 ps of the skew budget (the interval from –410 to +677 ps). Timing is verified by referencing the falling edge of CK. See Chapter 10 of the *MSC711x Reference Manual* for details.
- Determined by maximum possible skew between a data strobe (DQS) and any corresponding bit of data. The data strobe should be centered inside of the data eye.
- Please note that this spec is in reference to the DQSn first rising edge. It could also be referenced from CK(r), but due to programmable delay of the write strobes (TCFG2[WRDD]), there pre-amble may be extended for a full DRAM cycle. For this reason, we reference from DQSn.
- All outputs are referenced to the rising edge of CK. Note that this is essentially the CK/DQSn skew in spec 208. In addition there is no real “maximum” time for the epilogue end. JEDEC does not require this is as a device limitation, but simply for the chip to guarantee fast enough write to read turn-around times. This is already guaranteed by the memory controller operation.