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Freescale Semiconductor
Data Sheet:

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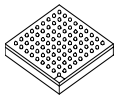
MSC8144E



FC-PBGA–783
29 mm × 29 mm

Quad Core Digital Signal Processor

- Four StarCore® SC3400 DSP subsystems, each with an SC3400 DSP core, 16 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, memory management unit (MMU), extended programmable interrupt controller (EPIC), two general-purpose 32-bit timers, debug and profiling support, and low-power Wait and Stop processing modes.
- Chip-level arbitration and system (CLASS) that provides full fabric non-blocking arbitration between the processing elements and other initiators and the M2 memory, DDR SRAM controller, device configuration control and status registers, and other targets.
- 128 Kbyte L2 shared instruction cache.
- 512 Kbyte M2 memory for critical data and temporary data buffering.
- 10 Mbyte 128-bit wide M3 memory.
- 96 Kbyte boot ROM.
- Three input clocks (shared, global, and differential).
- Four PLLs (system, core, global, and serial RapidIO).
- Security Engine (SEC0 optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP using 4 crypto-channels with multi-command chains, integrated controller for assignment of the six execution units (PKEU, DEU, AESU, AFEU, MDEU, and KEU0) and the random number generator (RNG), and XOR engine to accelerate parity checking for RAID storage applications.
- DDR controller with up to a 200 MHz clock (400 MHz data rate), 16/32 bit data bus, supporting up to 1 Gbyte in up to two banks and support for DDR1 and DDR2.
- DMA controller with 16 bidirectional channels with up to 1024 buffer descriptors, and programmable priority, buffer, and multiplexing configuration.
- Up to eight independent TDM modules with programmable word size (2, 4, 8, or 16-bit), hardware-base A-law/µ-law conversion, up to 128 Mbps data rate for all channels, with glueless interface to E1 or T1 framers, and can interface with H-MVIP/H.110 devices, TSI, and codecs such as AC-97.
- QUICC Engine™ technology subsystem with dual RISC processors, 48 Kbyte multi-master RAM, 48 Kbyte instruction RAM, supporting three communication controllers with one ATM and two Gigabit Ethernet interfaces, to offload scheduling tasks from the DSP cores.
  - The two Ethernet controllers support 10/100/1000 Mbps operations via MII/RMII/SMII/RGMII/SGMII and the SGMII protocol using a 4-pin SerDes interface at 1000 Mbps data rate only.
  - The ATM controller supports UTOPIA level II 8/16 bits at 25/50 MHz in UTOPIA/POS mode with adaptation layer support AAL0, AAL2, and AAL5.
- PCI designed to comply with the PCI specification revision 2.2 at 33 MHz or 66 MHz with access to all PCI address spaces.
- Serial RapidIO® 1x/4x endpoint corresponds to Specification 1.2 of the RapidIO trade association, and supports read, write, messages, doorbells, and maintenance accesses in inbound mode, and messages and doorbells in outbound mode.
- I/O interrupt concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes them to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and the cores.
- UART that permits full-duplex operation with a bit rate of up to 6.25 Mbps.
- Serial peripheral interface (SPI).
- Four timer modules, each with four configurable16-bit timers.
- Four software watchdog timer (SWT) modules.
- Up to 32 general-purpose input/output (GPIO) ports, 16 of which can be configured as maskable interrupt inputs.
- I^2C interface that allows booting from EEPROM devices.
- Eight programmable hardware semaphores.
- Thirty two virtual maskable interrupts and one virtual $\overline{\text{NMI}}$ that can be generated by a simple write access.
- Optional booting via serial RapidIO port, PCI, I^2C, SPI, or Ethernet interfaces.

Note: This document supports mask set M31H.

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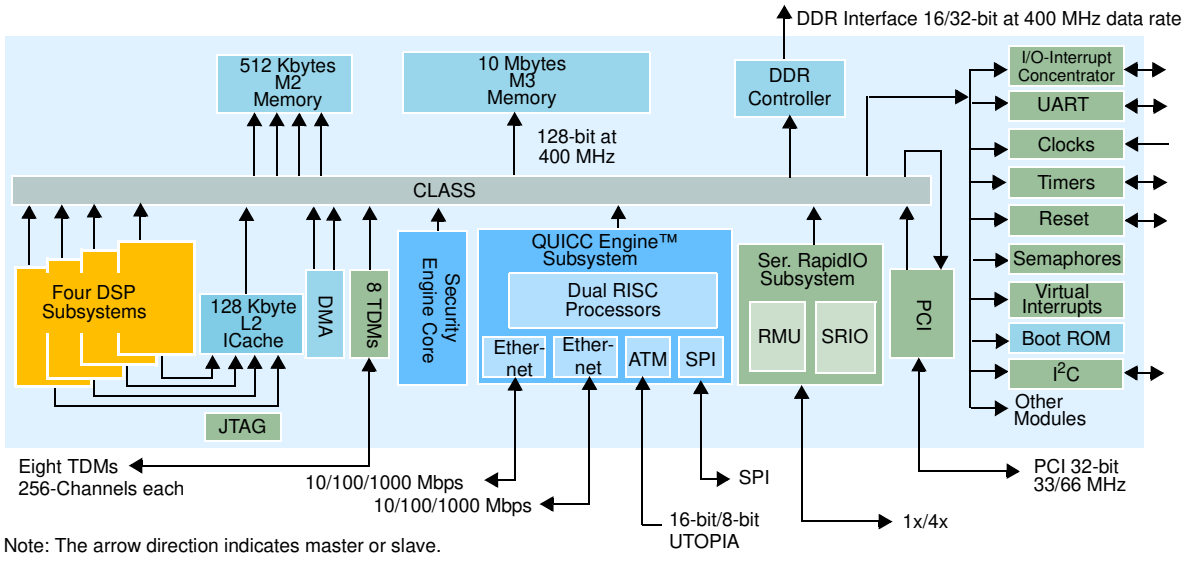

Figure 1. MSC8144E Block Diagram

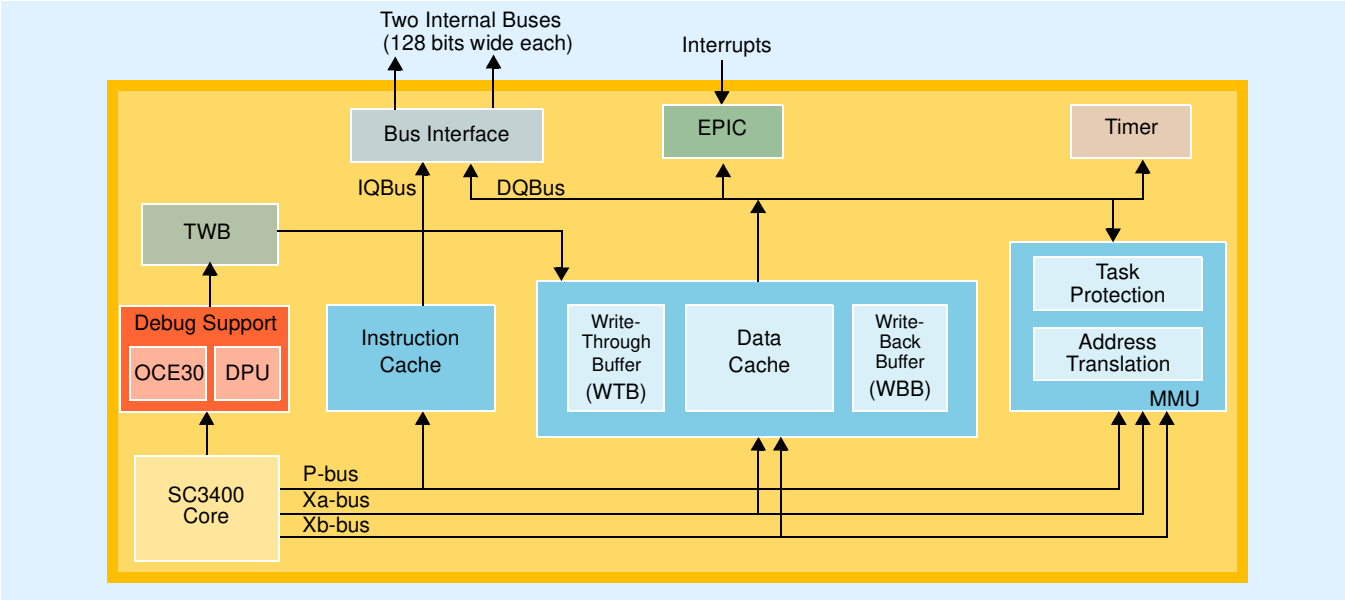

Figure 2. StarCore SC3400 DSP Core Subsystem Block Diagram

1 Pin Assignments and Reset States

This section includes diagrams of the MSC8144E package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in Figure 3 and Figure 4 with their ball location index numbers.

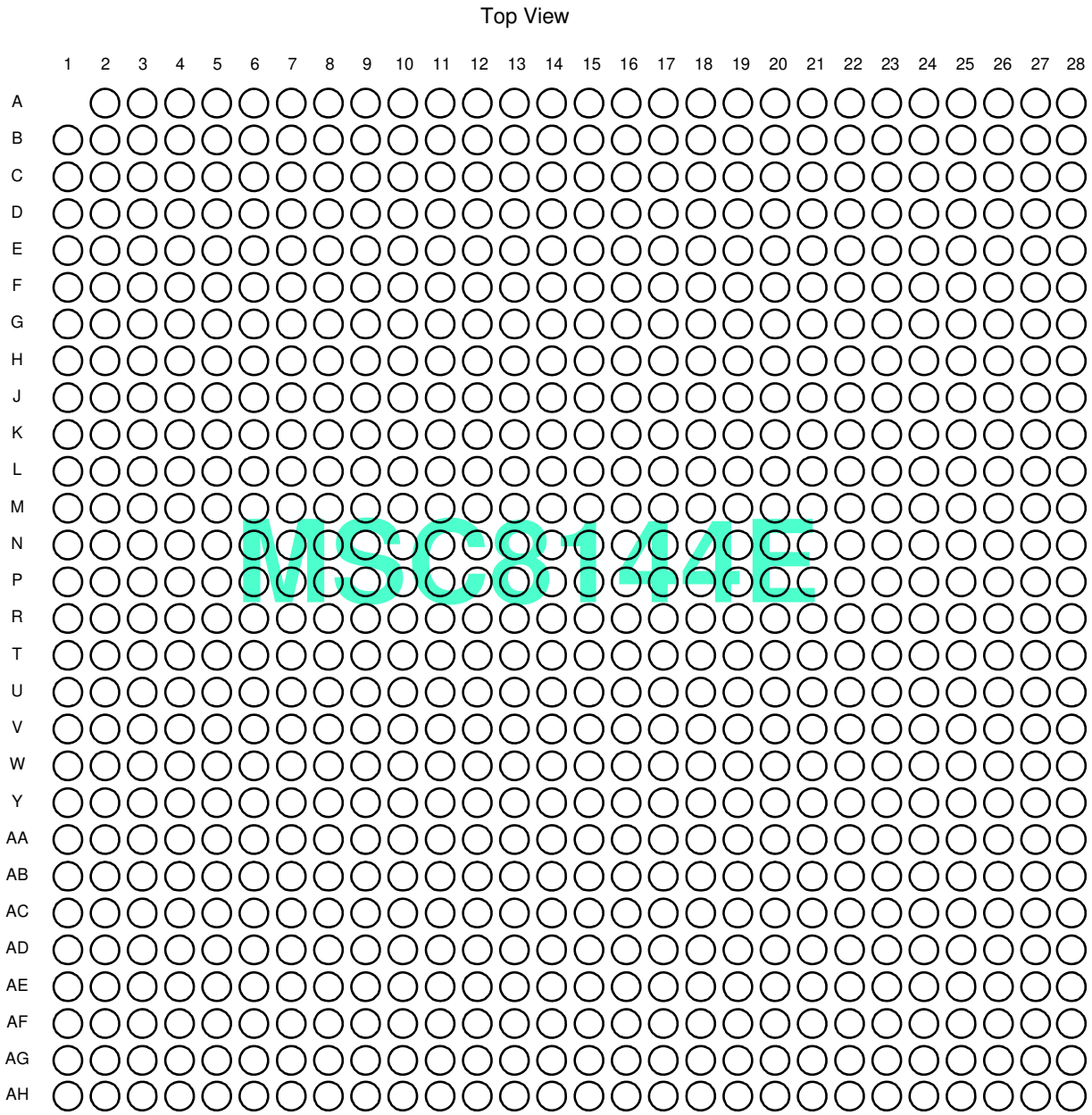

Figure 3. MSC8144E FC-PBGA Package, Top View

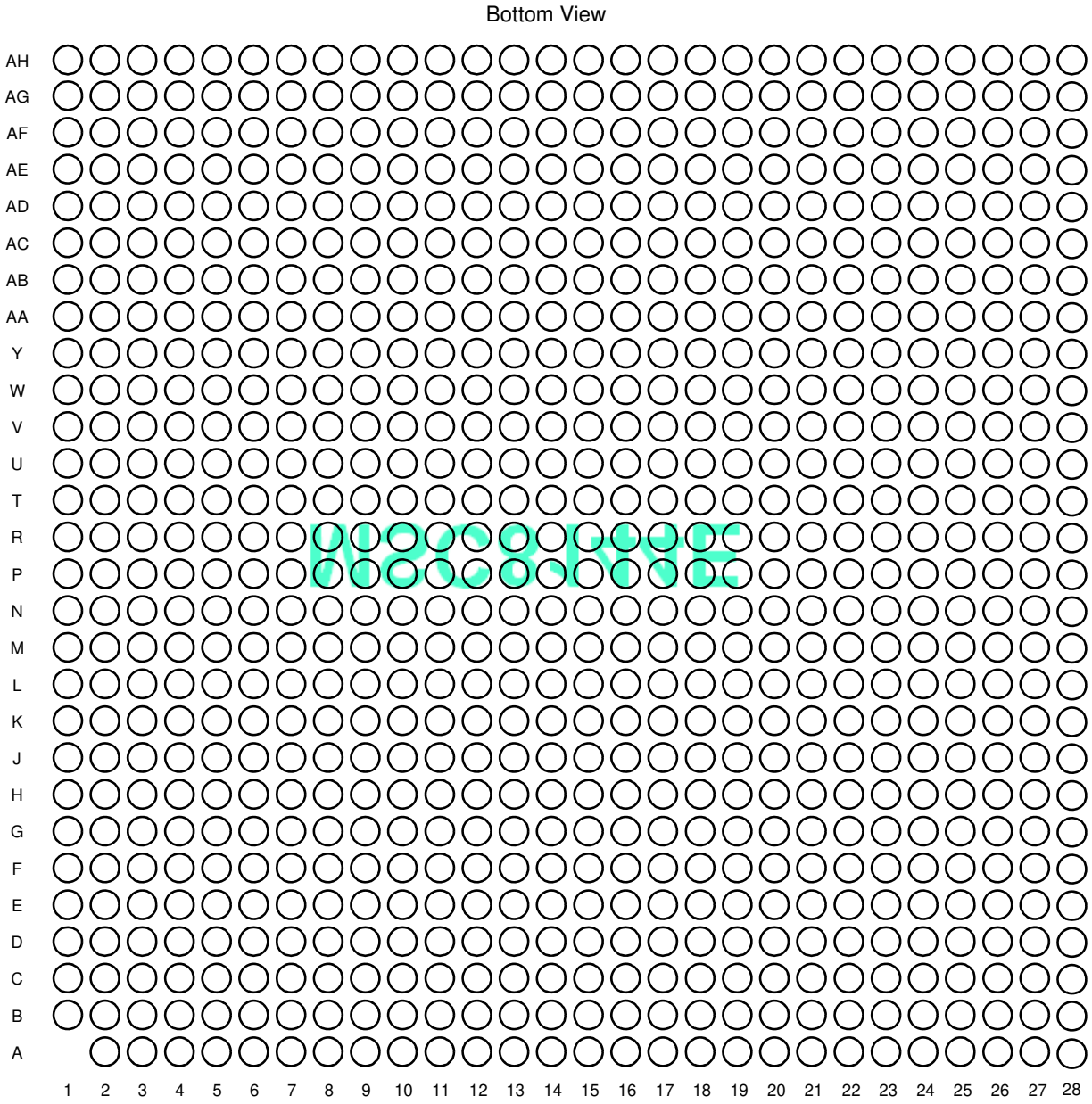

Figure 4. MSC8144E FC-PBGA Package, Bottom View

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A4	V_{DDGE2}										V_{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A6	GE2_TD0/$\overline{\text{PCI\_CBE0}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A7	SRIO_IMP_CAL_RX										V_{DDSXC}
A8	Reserved[1]										—
A9	Reserved[1]										—
A10	Reserved[1]										—
A11	Reserved[1]										—
A12	SRIO_RXD0										V_{DDSXC}
A13	V_{DDSXC}										V_{DDSXC}
A14	SRIO_RXD1										V_{DDSXC}
A15	V_{DDSXC}										V_{DDSXC}
A16	$\overline{\text{SRIO\_REF\_CLK}}$										V_{DDSXC}
A17	$V_{DDRIOPLL}$										GND_{RIOPLL}
A18	GND_{SXC}										GND_{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A20	V_{DDSXC}										V_{DDSXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A22	V_{DDSXC}										V_{DDSXC}
A23	SRIO_IMP_CAL_TX										V_{DDSXP}
A24	MDQ28										V_{DDDDR}
A25	MDQ29										V_{DDDDR}
A26	MDQ30										V_{DDDDR}
A27	MDQ31										V_{DDDDR}
A28	$\overline{\text{MDQS3}}$										V_{DDDDR}
B1	Reserved[1]										—
B2	GE2_TD1/$\overline{\text{PCI\_CBE1}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B3	GE2_TX_EN/$\overline{\text{PCI\_CBE2}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B4	GE_MDIO		Ethernet								V_{DDGE2}
B5	GND										GND
B6	GE_MDC		Ethernet								V_{DDGE2}
B7	GND_{SXC}										GND_{SXC}
B8	Reserved[1]										—
B9	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
B10	Reserved[1]										—
B11	Reserved[1]										—
B12	$\overline{\text{SRIO\_RXD0}}$										V_{DDSXC}
B13	GND_{SXC}										GND_{SXC}
B14	$\overline{\text{SRIO\_RXD1}}$										V_{DDSXC}
B15	GND_{SXC}										GND_{SXC}
B16	SRIO_REF_CLK										V_{DDSXC}
B17	Reserved[1]										—
B18	V_{DDSXC}										V_{DDSXC}
B19	$\overline{\text{SRIO\_RXD2}}$/ $\overline{\text{GE1\_SGMII\_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B20	GND_{SXC}										GND_{SXC}
B21	$\overline{\text{SRIO\_RXD3}}$/ $\overline{\text{GE2\_SGMII\_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B22	GND_{SXC}										GND_{SXC}
B23	GND_{SXP}										GND_{SXP}
B24	MDQ27										V_{DDDDR}
B25	V_{DDDDR}										V_{DDDDR}
B26	GND										GND
B27	V_{DDDDR}										V_{DDDDR}
B28	MDQS3										V_{DDDDR}
C1	Reserved[1]										—
C2	GE2_RX_CLK/PCI_AD29		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C3	V_{DDGE2}										V_{DDGE2}
C4	TDM7RSYN/GE2_TD2/ PCI_AD2/UTP_TER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C5	TDM7RCLK/GE2_RD2/ PCI_AD0/UTP_RVL		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C6	V_{DDGE2}										V_{DDGE2}
C7	GE2_RD0/PCI_AD27		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C8	Reserved[1]										—
C9	Reserved[1]										—
C10	Reserved[1]										—
C11	Reserved[1]										—
C12	V_{DDSXP}										V_{DDSXP}
C13	$\overline{\text{SRIO\_TXD0}}$										V_{DDSXP}
C14	V_{DDSXP}										V_{DDSXP}
C15	$\overline{\text{SRIO\_TXD1}}$										V_{DDSXP}
C16	GND_{SXC}										GND_{SXC}
C17	GND_{RIOPLL}										GND_{RIOPLL}
C18	Reserved[1]										—
C19	V_{DDSXP}										V_{DDSXP}
C20	$\overline{\text{SRIO\_TXD2}}$/$\overline{\text{GE1\_SGMII\_TX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
C21	V_{DDSXP}										V_{DDSXP}
C22	SRIO_TXD3/GE2_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
C23	V_{DDSXP}										V_{DDSXP}
C24	MDQ26										V_{DDDDR}
C25	MDQ25										V_{DDDDR}
C26	MDM3										V_{DDDDR}
C27	GND										GND
C28	MDQ24										V_{DDDDR}
D1	Reserved[1]										—
D2	GE2_RD1/PCI_AD28		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
D3	GND										GND
D4	TDM7TDAT/GE2_TD3/ PCI_AD3/UTP_TMD		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D5	TDM7RDAT/GE2_RD3/ PCI_AD1/UTP_STA		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D6	GE1_RD0/UTP_RD2/ PCI_CBE2		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
D7	TDM7TCLK/GE2_TCK/ PCI_IDS/UTP_RER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D8	Reserved[1]										—
D9	Reserved[1]										—
D10	Reserved[1]										—
D11	Reserved[1]										—
D12	GND_{SXP}										GND_{SXP}
D13	SRIO_TXD0										V_{DDSXP}
D14	GND_{SXP}										GND_{SXP}
D15	SRIO_TXD1										V_{DDSXP}
D16	V_{DDSXC}										V_{DDSXC}
D17	Reserved[1]										—
D18	Reserved[1]										—
D19	GND_{SXP}										GND_{SXP}
D20	SRIO_TXD2/GE1_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D21	GND_{SXP}										GND_{SXP}
D22	SRIO_TXD3/GE2_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D23	GND_{SXP}										GND_{SXP}
D24	MDQ23										V_{DDDDR}
D25	V_{DDDDR}										V_{DDDDR}
D26	MDQ22										V_{DDDDR}
D27	MDQ21										V_{DDDDR}
D28	MDQS2										V_{DDDDR}
E1	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E6	V_{DDGE1}										V_{DDGE1}
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E8	Reserved[1]										—
E9	Reserved[1]										—
E10	GND										GND
E11	V_{DD}										V_{DD}
E12	GND										GND
E13	V_{DD}										V_{DD}
E14	GND										GND
E15	V_{DD}										V_{DD}
E16	GND										GND
E17	V_{DD}										V_{DD}
E18	GND										GND
E19	V_{DD}										V_{DD}
E20	GND										GND
E21	V_{DD}										V_{DD}
E22	GND										GND
E23	V_{DDDDR}										V_{DDDDR}
E24	MDQ20										V_{DDDDR}
E25	GND										GND
E26	V_{DDDDR}										V_{DDDDR}
E27	GND										GND
E28	MDQS2										V_{DDDDR}
F1	Reserved[1]										—
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F3	V_{DDGE1}										V_{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F6	GND										GND
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F8	V_{DDGE1}										V_{DDGE1}
F9	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
F10	V_{DD}										V_{DD}
F11	GND										GND
F12	V_{DD}										V_{DD}
F13	GND										GND
F14	V_{DD}										V_{DD}
F15	GND										GND
F16	V_{DD}										V_{DD}
F17	GND										GND
F18	V_{DD}										V_{DD}
F19	GND										GND
F20	V_{DD}										V_{DD}
F21	Reserved[1]										—
F22	V_{DDDDR}										V_{DDDDR}
F23	GND										GND
F24	MDQ19										V_{DDDDR}
F25	MDQ18										V_{DDDDR}
F26	MDM2										V_{DDDDR}
F27	MDQ17										V_{DDDDR}
F28	MDQ16										V_{DDDDR}
G1	Reserved[1]										—
G2	$\overline{\text{SRESET}}$[4]										V_{DDIO}
G3	GND										GND
G4	$\overline{\text{PORESET}}$[4]										V_{DDIO}
G5	GE1_COL/UTP_RD1		UTOPIA	Ethernet 1		UTOPIA			Ethernet 1	UTOPIA	V_{DDIO}
G6	GE1_TD2/UTP_TD4/ PCI_AD29		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
G7	GE1_RX_DV/UTP_RD7		UTOPIA	Ethernet 1		UTOPIA			Ethernet 1	UTOPIA	V_{DDGE1}
G8	$\overline{\text{GE1\_TX\_ER}}$/UTP_TD7/ $\overline{\text{PCI\_CBE1}}$		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
G9	V_{DD}										V_{DD}
G10	GND										GND
G11	V_{DD}										V_{DD}
G12	GND										GND
G13	V_{DD}										V_{DD}
G14	GND										GND
G15	V_{DD}										V_{DD}
G16	GND										GND
G17	V_{DD}										V_{DD}
G18	GND										GND
G19	V_{DD}										V_{DD}
G20	GND										GND
G21	Reserved[1]	—									—
G22	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
G23	MBA1										V_{DDDDR}
G24	MA3										V_{DDDDR}
G25	MA8										V_{DDDDR}
G26	V_{DDDDR}										V_{DDDDR}
G27	GND										GND
G28	$\overline{\text{MCK0}}$										V_{DDDDR}
H1	Reserved[1]										—
H2	CLKIN										V_{DDIO}
H3	$\overline{\text{HRESET}}$										V_{DDIO}
H4	PCI_CLK_IN										V_{DDIO}
H5	$\overline{\text{NMI}}$										V_{DDIO}
H6	URXD/GPIO14/$\overline{\text{IRQ8}}$/ $\overline{\text{RC\_LDF}}$[3, 6]	$\overline{\text{RC\_LDF}}$	UART/GPIO/IRQ								V_{DDIO}
H7	GE1_RX_ER/PCI_AD6/ GPIO25/$\overline{\text{IRQ15}}$[3, 6]		GPIO/ IRQ	Ethernet 1	PCI			GPIO/ IRQ	Ethernet 1		V_{DDIO}
H8	GE1_CRS/PCI_AD5		PCI	Ethernet 1	PCI				Ethernet 1		V_{DDIO}
H9	GND										GND
H10	V_{DD}										V_{DD}
H11	GND										GND
H12	V_{DD}										V_{DD}
H13	GND										GND
H14	V_{DD}										V_{DD}
H15	V_{DD}										V_{DD}
H16	V_{DD}										V_{DD}
H17	GND										GND
H18	V_{DD}										V_{DD}
H19	GND										GND
H20	V_{DD}										V_{DD}
H21	V_{DD}										V_{DD}
H22	V_{DDDDR}										V_{DDDDR}
H23	MBA0										V_{DDDDR}
H24	MA15										V_{DDDDR}
H25	V_{DDDDR}										V_{DDDDR}
H26	MA9										V_{DDDDR}
H27	MA7										V_{DDDDR}
H28	MCK0										V_{DDDDR}
J1	Reserved[1]										—
J2	GND										GND
J3	V_{DDIO}										V_{DDIO}
J4	STOP_BS										V_{DDIO}
J5	$\overline{\text{NMI\_OUT}}$[4]										V_{DDIO}
J6	$\overline{\text{INT\_OUT}}$[4]										V_{DDIO}
J7	SDA/GPIO27[3, 4, 6]		I2C/GPIO								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
K23	MBA2										V_{DDDDR}
K24	MA10										V_{DDDDR}
K25	MA12										V_{DDDDR}
K26	MA14										V_{DDDDR}
K27	MA4										V_{DDDDR}
K28	MV_{REF}										V_{DDDDR}
L1	Reserved[1]										—
L2	CLKOUT										V_{DDIO}
L3	TMR1/UTP_IR/$\overline{\text{PCI\_CBE3}}$/ GPIO17[3, 6]		UTOPIA		TMR/ GPIO	UTOPIA	PCI	UTOPIA			V_{DDIO}
L4	TMR4/PCI_PAR/GPIO20[3, 6]/ UTP_REOP		TIMER/GPIO				PCI	TIMER/GPIO			V_{DDIO}
L5	GND										GND
L6	TMR2/$\overline{\text{PCI\_FRAME}}$/ GPIO18[3, 6]		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
L7	SCL/GPIO26[3, 4, 6]		I^2C/GPIO								V_{DDIO}
L8	UTXD/GPIO15/$\overline{\text{IRQ9}}$[3, 6]		UART/GPIO/IRQ								V_{DDIO}
L9	GND										GND
L10	V_{DD}										V_{DD}
L11	GND										GND
L12	V_{DD}										V_{DD}
L13	GND										GND
L14	V_{DD}										V_{DD}
L15	Reserved[1]										GND
L16	V_{DD}										V_{DD}
L17	GND										GND
L18	V_{DD}										V_{DD}
L19	GND										GND
L20	V_{DD}										V_{DD}
L21	GND										GND
L22	GND										GND
L23	MCKE1										V_{DDDDR}
L24	MA1										V_{DDDDR}
L25	V_{DDDDR}										V_{DDDDR}
L26	GND										GND
L27	V_{DDDDR}										V_{DDDDR}
L28	$\overline{\text{MCK1}}$										V_{DDDDR}
M1	Reserved[1]										—
M2	$\overline{\text{TRST}}$										V_{DDIO}
M3	EE0										V_{DDIO}
M4	EE1										V_{DDIO}
M5	UTP_RCLK/PCI_AD13		UTOPIA		PCI	UTOPIA					V_{DDIO}
M6	UTP_RADDR0/PCI_AD7		UTOPIA		PCI	UTOPIA					V_{DDIO}
M7	UTP_TD8/PCI_AD30		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
M8	V_{DDIO}										V_{DDIO}
M9	V_{DD}										V_{DD}
M10	GND										GND
M11	V_{DD}										V_{DD}
M12	GND										GND
M13	V_{DD}										V_{DD}
M14	GND										GND
M15	V_{DD}										V_{DD}
M16	GND										GND
M17	V_{DD}										V_{DD}
M18	GND										GND
M19	V_{DD}										V_{DD}
M20	GND										GND
M21	V_{DD}										V_{DD}
M22	V_{DDDDR}										V_{DDDDR}
M23	$\overline{MCS1}$										V_{DDDDR}
M24	MA13										V_{DDDDR}
M25	MA2										V_{DDDDR}
M26	MA0										V_{DDDDR}
M27	GND										GND
M28	MCK1										V_{DDDDR}
N1	Reserved[1]										—
N2	V_{DDIO}										V_{DDIO}
N3	TMS										V_{DDIO}
N4	UTP_RD10/PCI_AD14[5]		UTOPIA		PCI	UTOPIA					V_{DDIO}
N5	V_{DDIO}		Power								V_{DDIO}
N6	UTP_RADDR1/PCI_AD8		UTOPIA		PCI	UTOPIA					V_{DDIO}
N7	UTP_TD9/PCI_AD31		UTOPIA		PCI	UTOPIA					V_{DDIO}
N8	TMR3/$\overline{PCI\_IRDY}$/GPIO19[3,6]/ UTP_TEOP		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
N9	GND										GND
N10	V_{DDM3}										V_{DDM3}
N11	V_{DD}										V_{DD}
N12	V_{DDM3}										V_{DDM3}
N13	V_{DD}										V_{DD}
N14	V_{DDM3}										V_{DDM3}
N15	V_{DD}										V_{DD}
N16	V_{DDM3}										V_{DDM3}
N17	V_{DD}										V_{DD}
N18	V_{DDM3}										V_{DDM3}
N19	V_{DD}										V_{DD}
N20	V_{DDM3}										V_{DDM3}
N21	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
N22	GND										GND
N23	MODT1										V_{DDDDR}
N24	MCKE0										V_{DDDDR}
N25	V_{DDDDR}										V_{DDDDR}
N26	MA5										V_{DDDDR}
N27	MA6										V_{DDDDR}
N28	MA11										V_{DDDDR}
P1	Reserved[1]										—
P2	TDI[5]										V_{DDIO}
P3	UTP_RD11/PCI_AD15		UTOPIA		PCI	UTOPIA					V_{DDIO}
P4	GND										GND
P5	UTP_RADDR3/PCI_AD10		UTOPIA		PCI	UTOPIA					V_{DDIO}
P6	UTP_RADDR2/PCI_AD9		UTOPIA		PCI	UTOPIA					V_{DDIO}
P7	$\overline{\text{PCI\_GNT}}$/GPIO29/$\overline{\text{IRQ7}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
P8	$\overline{\text{PCI\_STOP}}$/GPIO30/$\overline{\text{IRQ2}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
P9	GND										GND
P10	GND										GND
P11	V_{DDM3}										V_{DDM3}
P12	GND										GND
P13	V_{DDM3}										V_{DDM3}
P14	GND										GND
P15	V_{DDM3}										V_{DDM3}
P16	GND										GND
P17	V_{DDM3}										V_{DDM3}
P18	GND										GND
P19	V_{DDM3}										V_{DDM3}
P20	GND										GND
P21	GND										GND
P22	V_{DDDDR}										V_{DDDDR}
P23	$\overline{\text{MCS0}}$										V_{DDDDR}
P24	$\overline{\text{MRAS}}$										V_{DDDDR}
P25	GND										GND
P26	V_{DDDDR}										V_{DDDDR}
P27	GND										GND
P28	$\overline{\text{MCK2}}$										V_{DDDDR}
R1	Reserved[1]										—
R2	TCK										V_{DDIO}
R3	TDO										V_{DDIO}
R4	UTP_RD12/PCI_AD16		UTOPIA		PCI	UTOPIA					V_{DDIO}
R5	UTP_RCLAV_PDRPA/ PCI_AD12		UTOPIA		PCI	UTOPIA					V_{DDIO}
R6	UTP_RADDR4/PCI_AD11		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
R7	V_{DDIO}										V_{DDIO}
R8	$\overline{\text{PCI\_REQ}}$		PCI								V_{DDIO}
R9	GND										GND
R10	GND										GND
R11	GND										GND
R12	GND										GND
R13	GND										GND
R14	GND										GND
R15	GND										GND
R16	GND										GND
R17	GND										GND
R18	GND										GND
R19	GND										GND
R20	GND										GND
R21	GND										GND
R22	GND										GND
R23	MODT0										V_{DDDDR}
R24	MDIC1										V_{DDDDR}
R25	MDIC0										V_{DDDDR}
R26	$\overline{\text{MCAS}}$										V_{DDDDR}
R27	$\overline{\text{MWE}}$										V_{DDDDR}
R28	MCK2										V_{DDDDR}
T1	Reserved[1]										—
T2	UTP_RPRTY/PCI_AD21		UTOPIA		PCI	UTOPIA					V_{DDIO}
T3	UTP_RD13/PCI_AD17		UTOPIA		PCI	UTOPIA					V_{DDIO}
T4	V_{DDIO}										V_{DDIO}
T5	UTP_RD14/PCI_AD18		UTOPIA		PCI	UTOPIA					V_{DDIO}
T6	UTP_RD15/PCI_AD19		UTOPIA		PCI	UTOPIA					V_{DDIO}
T7	$\overline{\text{PCI\_TRDY}}$		PCI								V_{DDIO}
T8	$\overline{\text{PCI\_DEVSEL}}$/GPIO31/ $\overline{\text{IRQ3}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
T9	GND										GND
T10	GND										GND
T11	GND										GND
T12	GND										GND
T13	GND										GND
T14	GND										GND
T15	GND										GND
T16	GND										GND
T17	GND										GND
T18	GND										GND
T19	GND										GND
T20	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
T21	GND										GND
T22	V_{DDDDR}										V_{DDDDR}
T23	GND										GND
T24	V_{DDDDR}										V_{DDDDR}
T25	GND										GND
T26	V_{DDDDR}										V_{DDDDR}
T27	GND										GND
T28	V_{DDDDR}										V_{DDDDR}
U1	Reserved[1]										—
U2	UTP_TCLK/PCI_AD29		UTOPIA		PCI	UTOPIA					V_{DDIO}
U3	UTP_TADDR4/PCI_AD27		UTOPIA		PCI	UTOPIA					V_{DDIO}
U4	UTP_TADDR2		UTOPIA								V_{DDIO}
U5	GND										GND
U6	$\overline{\text{UTP\_REN}}$/PCI_AD20		UTOPIA		PCI	UTOPIA					V_{DDIO}
U7	PCI_AD26		PCI								V_{DDIO}
U8	PCI_AD25		PCI								V_{DDIO}
U9	Reserved[1]										V_{DDIO}
U10	V_{DDM3}										V_{DDM3}
U11	GND										GND
U12	V_{DDM3}										V_{DDM3}
U13	GND										GND
U14	V_{DDM3}										V_{DDM3}
U15	GND										GND
U16	V_{DDM3}										V_{DDM3}
U17	GND										GND
U18	V_{DDM3}										V_{DDM3}
U19	GND										GND
U20	V_{DDM3}										V_{DDM3}
U21	GND										GND
U22	GND										GND
U23	MDQ7										V_{DDDDR}
U24	MDQ3										V_{DDDDR}
U25	MDQ4										V_{DDDDR}
U26	MDQ5										V_{DDDDR}
U27	MDQ1										V_{DDDDR}
U28	MDQ0										V_{DDDDR}
V1	Reserved[1]										—
V2	UTP_TD10/$\overline{\text{PCI\_CBE0}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
V3	UTP_TADDR3		UTOPIA								V_{DDIO}
V4	UTP_TD1/$\overline{\text{PCI\_PERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
V5	UTP_TADDR0/PCI_AD23		UTOPIA		PCI	UTOPIA					V_{DDIO}
V6	UTP_TADDR1/PCI_AD24		UTOPIA		PCI	UTOPIA					V_{DDIO}
V7	UTP_TCLAV/PCI_AD28		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
V8	V_{DDIO}										V_{DDIO}
V9	Reserved[1]										V_{DDIO}
V10	GND										GND
V11	V_{DDM3}										V_{DDM3}
V12	GND										GND
V13	V_{DDM3}										V_{DDM3}
V14	GND										GND
V15	V_{DDM3}										V_{DDM3}
V16	GND										GND
V17	V_{DDM3}										V_{DDM3}
V18	GND										GND
V19	V_{DDM3}										V_{DDM3}
V20	GND										GND
V21	GND										GND
V22	V_{DDDDR}										V_{DDDDR}
V23	MDQ2										V_{DDDDR}
V24	V_{DDDDR}										V_{DDDDR}
V25	MDQ6										V_{DDDDR}
V26	GND										GND
V27	V_{DDDDR}										V_{DDDDR}
V28	MDQS0										V_{DDDDR}
W1	Reserved[1]										—
W2	UTP_TD12/$\overline{\text{PCI\_CBE2}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W3	UTP_TD11/$\overline{\text{PCI\_CBE1}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W4	V_{DDIO}										V_{DDIO}
W5	GND										GND
W6	UTP_TD15/$\overline{\text{PCI\_IRDY}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W7	UTP_TD0/$\overline{\text{PCI\_SERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
W8	UTP_RSOC/PCI_AD22		UTOPIA		PCI	UTOPIA					V_{DDIO}
W9	Reserved[1]										V_{DDIO}
W10	V_{DDM3}										V_{DDM3}
W11	GND										GND
W12	V_{25M3}										V_{25M3}
W13	GND										GND
W14	V_{DDM3}										V_{DDM3}
W15	V_{25M3}										V_{25M3}
W16	V_{DDM3}										V_{DDM3}
W17	GND										GND
W18	V_{25M3}										V_{25M3}
W19	GND										GND
W20	V_{DDM3}										V_{DDM3}
W21	GND										GND
W22	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
W23	MDQ10										V_{DDDDR}
W24	GND										GND
W25	MDQ11										V_{DDDDR}
W26	MDM0										V_{DDDDR}
W27	GND										GND
W28	$\overline{\text{MDQS0}}$										V_{DDDDR}
Y1	Reserved[1]										-
Y2	UTP_TD14/$\overline{\text{PCI\_FRAME}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
Y3	TDM5TSYN/PCI_AD18/ GPIO12[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
Y4	TDM5TCLK/PCI_AD16		TDM			PCI		TDM			V_{DDIO}
Y5	TDM4RCLK/PCI_AD7		TDM			PCI		TDM			V_{DDIO}
Y6	TDM4TSYN/PCI_AD12		TDM			PCI		TDM			V_{DDIO}
Y7	UTP_TPRTY/RC14	RC14	UTOPIA								V_{DDIO}
Y8	$\overline{\text{UTP\_TEN}}$/PCI_PAR		UTOPIA		PCI	UTOPIA					V_{DDIO}
Y9	Reserved[1]										V_{DDIO}
Y10	GND										GND
Y11	V_{DDM3}										V_{DDM3}
Y12	GND										GND
Y13	V_{DDM3}										V_{DDM3}
Y14	GND										GND
Y15	V_{DDM3}										V_{DDM3}
Y16	GND										GND
Y17	V_{DDM3}										V_{DDM3}
Y18	GND										GND
Y19	V_{DDM3}										V_{DDM3}
Y20	GND										GND
Y21	GND										GND
Y22	V_{DDDDR}										V_{DDDDR}
Y23	MDQ13										V_{DDDDR}
Y24	V_{DDDDR}										V_{DDDDR}
Y25	GND										GND
Y26	MDQ9										V_{DDDDR}
Y27	V_{DDDDR}										V_{DDDDR}
Y28	MDQ8										V_{DDDDR}
AA1	Reserved[1]										—
AA2	UTP_TD13/$\overline{\text{PCI\_CBE3}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
AA3	TDM5RSYN/PCI_AD15/ GPIO10[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AA4	TDM5TDAT, AT/PCI_AD17/ GPIO11[6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AA5	TDM5RCLK/PCI_AD13/ GPIO28[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AA6	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AA7	TDM4TCLK/PCI_AD10		TDM			PCI		TDM			V_{DDIO}
AA8	TDM4TDAT/PCI_AD11		TDM			PCI		TDM			V_{DDIO}
AA9	V_{DDIO}										V_{DDIO}
AA10	V_{DDM3}										V_{DDM3}
AA11	GND										GND
AA12	V_{DDM3}										V_{DDM3}
AA13	GND										GND
AA14	V_{DDM3}										V_{DDM3}
AA15	GND										GND
AA16	V_{DDM3}										V_{DDM3}
AA17	GND										GND
AA18	V_{DDM3}										V_{DDM3}
AA19	GND										GND
AA20	V_{DDM3}										V_{DDM3}
AA21	GND										GND
AA22	GND										GND
AA23	MDQ15										V_{DDDDR}
AA24	MDQ14										V_{DDDDR}
AA25	MDM1										V_{DDDDR}
AA26	MDQ12										V_{DDDDR}
AA27	$\overline{\text{MDQS1}}$										V_{DDDDR}
AA28	MDQS1										V_{DDDDR}
AB1	Reserved[1]										-
AB2	UTP_TSOC/RC15	RC15	UTOPIA								V_{DDIO}
AB3	V_{DDIO}										V_{DDIO}
AB4	TDM6RDAT/PCI_AD20/ GPIO5/$\overline{\text{IRQ11}}$[3, 6]		TDM/GPIO/ IRQ			PCI		TDM/GPIO/ IRQ			V_{DDIO}
AB5	TDM5RDAT/PCI_AD14/ GPIO9[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AB6	TDM6TSYN/PCI_AD24/ GPIO8/ $\overline{\text{IRQ14}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB7	TDM6RCLK/PCI_AD19/ GPIO4/$\overline{\text{IRQ10}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB8	TDM4RSYN/PCI_AD9		TDM			PCI		TDM			V_{DDIO}
AB9	TDM4RDAT/PCI_AD8		TDM			PCI		TDM			V_{DDIO}
AB10	GND										GND
AB11	V_{DDM3}										V_{DDM3}
AB12	GND										GND
AB13	V_{DDM3}										V_{DDM3}
AB14	GND										GND
AB15	V_{DDM3}										V_{DDM3}
AB16	GND										GND
AB17	V_{DDM3}										V_{DDM3}
AB18	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AB19	V_{DDM3}										V_{DDM3}
AB20	GND										GND
AB21	GND										GND
AB22	V_{DDDDR}										V_{DDDDR}
AB23	MECC7										V_{DDDDR}
AB24	MECC1										V_{DDDDR}
AB25	MECC4										V_{DDDDR}
AB26	MECC5										V_{DDDDR}
AB27	MECC2										V_{DDDDR}
AB28	ECC_MDQS										V_{DDDDR}
AC1	Reserved[1]										—
AC2	UTP_RD9/RC13	RC13	UTOPIA								V_{DDIO}
AC3	UTP_RD8/RC12	RC12	UTOPIA								V_{DDIO}
AC4	TDM6TCLK/PCI_AD22		TDM			PCI		TDM			V_{DDIO}
AC5	TDM6RSYN/PCI_AD21/ GPIO6/ $\overline{IRQ12}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AC6	V_{DDIO}										V_{DDIO}
AC7	TDM3TSYN/RC11	RC11	TDM								V_{DDIO}
AC8	PCI_AD23/GPIO7/$\overline{IRQ13}$/ TDM6TDAT[3, 6]/UTP_RMOD		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ		UTOPIA	V_{DDIO}
AC9	TDM7TSYN/ PCI_AD4		TDM		PCI			reserved			V_{DDIO}
AC10	V_{DDM3IO}										V_{DDM3IO}
AC11	GND										GND
AC12	V_{DDM3}										V_{DDM3}
AC13	GND										GND
AC14	V_{DDM3}										V_{DDM3}
AC15	GND										GND
AC16	V_{DDM3}										V_{DDM3}
AC17	GND										GND
AC18	V_{DDM3}										V_{DDM3}
AC19	GND										GND
AC20	V_{DDM3IO}										V_{DDM3IO}
AC21	Reserved[1]										—
AC22	MECC6										V_{DDDDR}
AC23	MECC3										V_{DDDDR}
AC24	ECC_MDM										V_{DDDDR}
AC25	V_{DDDDR}										V_{DDDDR}
AC26	MECC0										V_{DDDDR}
AC27	V_{DDDDR}										V_{DDDDR}
AC28	$\overline{ECC\_MDQS}$										V_{DDDDR}
AD1	Reserved[1]										—
AD2	GPIO1[3, 6]		GPIO								V_{DDIO}
AD3	TMR0/GPIO13		TIMER/GPIO								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AD4	GPIO2[3, 6]		GPIO								V_{DDIO}
AD5	GND										GND
AD6	TDM1TCLK		TDM								V_{DDIO}
AD7	TDM3TDAT/RC10	RC10	TDM								V_{DDIO}
AD8	TDM3RSYN/RC9	RC9	TDM								V_{DDIO}
AD9	TDM3RDAT/RC8	RC8	TDM								V_{DDIO}
AD10	GND										GND
AD11	V_{25M3}										V_{25M3}
AD12	GND										GND
AD13	V_{DDM3}										V_{DDM3}
AD14	GND										GND
AD15	V_{25M3}										V_{25M3}
AD16	GND										GND
AD17	V_{DDM3}										V_{DDM3}
AD18	GND										GND
AD19	V_{25M3}										V_{25M3}
AD20	GND										GND
AD21	Reserved[1]										—
AD22	V_{DDDDR}										V_{DDDDR}
AD23	GND										GND
AD24	V_{DDDDR}										V_{DDDDR}
AD25	GND										GND
AD26	V_{DDDDR}										V_{DDDDR}
AD27	GND										GND
AD28	V_{DDDDR}										V_{DDDDR}
AE1	Reserved[1]										—
AE2	GPIO0[3, 6]		GPIO								V_{DDIO}
AE3	GPIO3[3, 6]		GPIO								V_{DDIO}
AE4	TDM1RCLK		TDM								V_{DDIO}
AE5	TDM1TSYN/RC3	RC3	TDM								V_{DDIO}
AE6	TDM1TDAT/RC2	RC2	TDM								V_{DDIO}
AE7	TDM1RSYN/RC1	RC1	TDM								V_{DDIO}
AE8	TDM3RCLK/RC16	RC16	TDM								V_{DDIO}
AE9	TDM3TCLK		TDM								V_{DDIO}
AE10	TDM2TDAT/RC6	RC6	TDM								V_{DDIO}
AE11	GPIO21/$\overline{IRQ1}$[3, 6]/SPICLK		GPIO/IRQ/SPI								V_{DDIO}
AE12	GND										GND
AE13	Reserved[1]										—
AE14	GND										GND
AE15	Reserved[1]										—
AE16	Reserved[1]										—
AE17	Reserved[1]										—
AE18	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AE19	GND										GND
AE20	V_{DDM3IO}										V_{DDM3IO}
AE21	Reserved[1]										—
AE22	GND										GND
AE23	GND										GND
AE24	GND										GND
AE25	V_{DDDDR}										V_{DDDDR}
AE26	GND										GND
AE27	V_{DDDDR}										V_{DDDDR}
AE28	GND										GND
AF1	Reserved[1]										—
AF2	V_{DDIO}										V_{DDIO}
AF3	GND										GND
AF4	TDM0RDAT/ RCFG_CLKIN_RNG	RCFG_ CLKIN_ RNG	TDM								V_{DDIO}
AF5	TDM0TSYN/RCW_SRC2	RCW_ SRC2	TDM								V_{DDIO}
AF6	TDM1RDAT/RC0	RC0	TDM								V_{DDIO}
AF7	V_{DDIO}										V_{DDIO}
AF8	GND										GND
AF9	TDM2RDAT/RC4	RC4	TDM								V_{DDIO}
AF10	TDM2TCLK		TDM								V_{DDIO}
AF11	GPIO22/$\overline{IRQ4}$[3, 6]/SPIMOSI		GPIO/IRQ/SPI								V_{DDIO}
AF12	GND										GND
AF13	GND										GND
AF14	V_{DDM3IO}										V_{DDM3IO}
AF15	GND										GND
AF16	GND										GND
AF17	Reserved[1]										—
AF18	V_{DDM3IO}										V_{DDM3IO}
AF19	GND										GND
AF20	Reserved[1]										—
AF21	Reserved[1]										—
AF22	$\overline{M3\_RESET}$										V_{DDM3IO}
AF23	GND										GND
AF24	V_{DDDDR}										V_{DDDDR}
AF25	GND										GND
AF26	V_{DDDDR}										V_{DDDDR}
AF27	GND										GND
AF28	V_{DDDDR}										V_{DDDDR}
AG1	Reserved[1]										—
AG2	GPIO16/$\overline{IRQ0}$[3, 6]		GPIO/IRQ								V_{DDIO}
AG3	TDM0TCLK		TDM								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AG4	TDM0RSYN/RCW_SRC0	RCW_SRC0	TDM								V_{DDIO}
AG5	TDM0RCLK		TDM								V_{DDIO}
AG6	TDM0TDAT/RCW_SRC1	RCW_SRC1	TDM								V_{DDIO}
AG7	TDM2TSYN/RC7	RC7	TDM								V_{DDIO}
AG8	TDM2RCLK		TDM								V_{DDIO}
AG9	TDM2RSYN/RC5	RC5	TDM								V_{DDIO}
AG10	GPIO24/$\overline{\text{IRQ6}}$[3, 6]/$\overline{\text{SPISEL}}$		GPIO/IRQ/SPI								V_{DDIO}
AG11	GPIO23/$\overline{\text{IRQ5}}$[3, 6]/SPIMISO		GPIO/IRQ/SPI								V_{DDIO}
AG12	Reserved[1]										—
AG13	GND										GND
AG14	GND										GND
AG15	GND										GND
AG16	GND										GND
AG17	Reserved[1]										—
AG18	Reserved[1]										—
AG19	GND										GND
AG20	GND										GND
AG21	V_{DDM3IO}										V_{DDM3IO}
AG22	GND										GND
AG23	GND										GND
AG24	GND										GND
AG25	V_{DDDDR}										V_{DDDDR}
AG26	GND										GND
AG27	V_{DDDDR}										V_{DDDDR}
AG28	GND										GND
AH1	Reserved[1]										—
AH2	Reserved[1]										—
AH3	Reserved[1]										—
AH4	Reserved[1]										—
AH5	Reserved[1]										—
AH6	Reserved[1]										—
AH7	Reserved[1]										—
AH8	Reserved[1]										—
AH9	Reserved[1]										—
AH10	Reserved[1]										—
AH11	Reserved[1]										—
AH12	Reserved[1]										—
AH13	Reserved[1]										—
AH14	Reserved[1]										—
AH15	Reserved[1]										—
AH16	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AH17	Reserved[1]										—
AH18	Reserved[1]										—
AH19	Reserved[1]										—
AH20	Reserved[1]										—
AH21	Reserved[1]										—
AH22	Reserved[1]										—
AH23	Reserved[1]										—
AH24	Reserved[1]										—
AH25	Reserved[1]										—
AH26	Reserved[1]										—
AH27	Reserved[1]										—
AH28	Reserved[1]										—

Notes:
1. Reserved signals should be disconnected for compatibility with future revisions of the device.
2. For signals with same functionality in all modes the appropriate cells are empty.
3. The choice between GPIO function and other function is by GPIO registers setup. For configuration details, see **Chapter 23,** *GPIO* in the *MSC8144E Reference Manual*.
4. Open-drain signal.
5. Internal 20 KΩ pull-up resistor.
6. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See **Chapter 23**, *GPIO* of the *MSC8144E Reference Manual* for configuration details.