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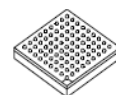
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MSC8157 Six-Core Digital Signal Processor

MSC8157



FC-PBGA-783
29 mm x 29 mm

- Six StarCore SC3850 DSP subsystems, each with an SC3850 DSP core, 32 KB L1 instruction cache, 32 KB L1 data cache, unified 512 KB L2 cache configurable as M2 memory in 64 KB increments, memory management unit (MMU), extended programmable interrupt controller (EPIC), two general-purpose 32-bit timers, debug and profiling support, low-power Wait, Stop, and power-down processing modes, and ECC/EDC support.
- Chip-level arbitration and switching system (CLASS) that provides full fabric non-blocking arbitration between the cores and other initiators and the M2 memory, shared M3 memory, DDR SRAM controller, device configuration control and status registers, MAPLE-B, and other targets.
- 3072 KB 128-bit wide M3 memory, 2048 KBs of which can be turned off to save power.
- 96 KB boot ROM.
- Three input clocks (one global and two differential).
- Six PLLs (three global, two Serial RapidIO, one DDR PLLs).
- Second generation Multi-Accelerator Platform Engine for Baseband (MAPLE-B2) with a second generation programmable system interface (PSIF2); Turbo encoding and decoding; Viterbi decoding; FFT/iFFT and DFT/iDFT processing; downlink chip rate processing; CRC processing and insertion; equalization processing and matrix inversion; uplink batch and fast processing. Some MAPLE-B2 processors can be disabled when not required to reduce overall power consumption.
- One DDR controllers with up to a 667 MHz clock (1333 MHz data rate), 64/32 bit data bus, supporting up to a total 2 Gbyte in up to four banks (two per controller) and support for DDR3.
- DMA controller with 32 unidirectional channels supporting 16 memory-to-memory channels with up to 1024 buffer descriptors per channel, and programmable priority, buffer, and multiplexing configuration. It is optimized for DDR SDRAM.
- High-speed serial interface with a 10-lane SerDes PHY that supports two Serial RapidIO interfaces, one PCI Express interface, six CPRI lanes, and two SGMII interfaces (multiplexed). The Serial RapidIO interfaces support x1/x2/x4 operation up to 5 Gbaud with an enhanced messaging unit (eMSG) and two DMA units. The PCI Express controller supports 32- and 64-bit addressing, x1/x2/x4 link. The six CPRI controllers can support six lanes up to 6.144 Gbaud.
- QUICC Engine technology subsystem with dual RISC processors, 48 KB multi-master RAM, 48 KB instruction RAM, supporting two communication controllers for two Gigabit Ethernet interfaces (RGMII or SGMII), to offload scheduling tasks from the DSP cores, and an SPI.
- I/O Interrupt Concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes then to INT_OUT/CP_TX_INT, NMI_OUT/CP_RX_INT, and the cores.
- UART that permits full-duplex operation with a bit rate of up to 6.25 Mbps.
- Two general-purpose 32-bit timers for RTOS support per SC3850 core, four timer modules with four 16-bit fully programmable timers, two timer modules with four 32-bit fully programmable timers; and eight software watchdog timers (SWT).
- Eight programmable hardware semaphores.
- Up to 32 virtual interrupts and a virtual NMI asserted by simple write access.
- I²C interface.
- Up to 32 GPIO ports, sixteen of which can be configured as external interrupts.
- Boot interface options include Ethernet, Serial RapidIO interface, I²C, and SPI.
- Supports IEEE Std. 1149.6 JTAG interface
- Low power CMOS design, with low-power standby and power-down modes, and optimized power-management circuitry.
- 45 nm SOI CMOS technology.

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

Table of Contents

1	Block Diagram	3	3.5	DC Electrical Characteristics	54
2	Pin Assignment	4	3.6	AC Timing Characteristics	69
	2.1	FC-PBGA Ball Layout Diagram	4	Hardware Design Considerations	92
	2.2	Signal Lists	5	Ordering Information	92
3	Electrical Characteristics	52	6	Package Information	93
	3.1	Maximum Ratings	7	Product Documentation	94
	3.2	Recommended Operating Conditions	8	Revision History	95
	3.3	Thermal Characteristics			
	3.4	CLKIN/MCLKIN Requirements			

1 Block Diagram

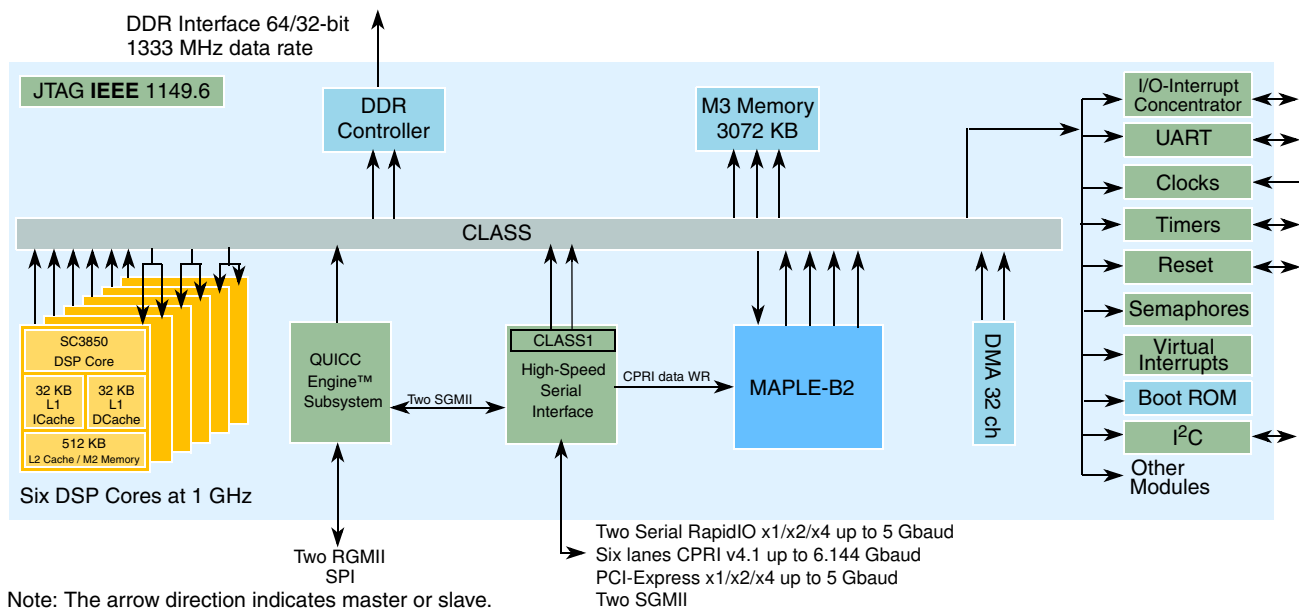


Figure 1. MSC8157 Block Diagram

2 Pin Assignment

This section includes a MSC8157 package ball grid array layout and table listing the signal allocation by ball location.

2.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in [Figure 2](#) with the ball location index numbers. Only the first multiplexed signal is shown. See [Table 1](#) for a complete signal list by ball location.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28			
A		VSS	MDQ57	GVDD	VSS	MDQ63	GVDD	NC	NC	NC	NC	CLKOUT	EEO	VSS	MCLKIN (optional)	VSS	CLKIN	VSS	GPI029	GPI031	GE1_TX_CTL	GE1_TX_CLK	GE1_TX_CLK	GE1_TX_CLK	GE1_TX_CLK	GE1_TX_CLK	GE1_TX_CLK	A			
B	MDQ60	MDQ59	MDQ57	MDQ57	MDQ62	MDQ58	MDQ56	NC	VSS	NC	VSS	NC	VSS	TDO	TMS	VSS	VSS	VSS	VSS	GE2_TX_CLK	VSS	VSS	VSS	GPI025	VSS	GE_MDC	VSS	GPI018	B		
C	VSS	GVDD	MDQ61	VSS	GVDD	MDM7	VSS	NC	NC	NC	NC	NC	NC	EE1	NC	DFT_TEST	PORRESET	VSS	GPI015	GE2_TX_CLK	GE2_TX_CLK	GE2_TX_CTL	GE2_TX_CLK	GE2_TX_CLK	GPI030	GPI020	GE_MDI0	GPI021	C		
D	MDQ49	MDQ48	MDQ56	MDQ56	MDQ50	MDQ51	MDQ52	NC	VSS	NC	VSS	NC	VSS	NC	NMI	VSS	HRESET_IN	VSS	VSS	GPI013	NVDD	GE2_TX_CLK	GE2_TX_CLK	VSS	GPI05	NVDD	GPI016	VSS	GPI010	D	
E	MDQ53	VSS	MDQ55	GVDD	VSS	MDQ54	GVDD	VSS	NC	NC	NC	NC	NC	NC	INT_OUT	HRESET	TCK	VSS	NVDD	GE2_RD3	VSS	VSS	NVDD	GPI027	VSS	GPI00	GPI017	GPI01	E		
F	MDQ40	MDQ41	MDQ55	MDQ55	MDQ43	MDQ47	MDM6	VDD	VSS	VDD	NC	NC	VSS	NC	NMI_OUT	VSS	TDI	VSS	GE2_RD2	GE2_RX_CTL	GE2_RX_CLK	GE2_RX_CLK	GE2_RD1	GPI026	GPI06	GPI022	GPI023	GPI08	F		
G	VSS	GVDD	MDM5	VSS	GVDD	MDQ46	VDD	VSS	VDD	VSS	NC	NC	NC	NC	QVDD	STOP_BS	TRST	VSS	GPI028	GE1_RD3	GE1_RD2	GE1_RX_CLK	VSS	GE1_RX_CTL	NVDD	GPI019	VSS	GPI011	G		
H	MDQ38	MDQ54	MDQ54	MDQ44	MDQ45	MDQ42	VSS	VDD	VSS	VDD	VSS	VSS	NC	QVDD	VSS	VDD	VSS	VDD	VSS	NVDD	VSS	GE1_RD0	NVDD	GE1_RD1	VSS	GPI014	NVDD	GPI012	H		
J	MDQ37	VSS	MDQ35	GVDD	MDQ33	MDQ36	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	GPI024	GPI09	RCW_LSEL3	RCW_LSEL2	RCW_LSEL1	RC21	GPI03	J	
K	MCAS	MC50	MC51	MDQ39	MDQ32	MDQ34	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	GPI04	VSS	RCW_LSEL1	NVDD	GPI07	VSS	GPI02	K		
L	VSS	GVDD	NC	VSS	GVDD	MDM4	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NVDD	NC	NC	VSS	VSS	VSS	SXCVSS	SXCVDD	L		
M	MCK0	MCK0	MA13	MWE	NC	NC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NC	NC	SD_A_TX	SD_A_TX	SXPVDD	SXPVSS	SD_A_RX	SD_A_RX	M	
N	MRA5	VSS	NC	GVDD	VSS	MDT1	CRPEVDD	VSS	CRPEVDD	VSS	CRPEVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NC	NC	SXPVDD	SXPVSS	SD_B_TX	SD_B_TX	SXCVSS	SXCVDD	N
P	MCK2	MA10	NC	MA4	NC	MDT0	VSS	CRPEVDD	VSS	CRPEVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NC	NC	SD_IMP_CAL_RX	NC	NC	SXPVDD	SXPVSS	SD_B_RX	SD_B_RX	P
R	MCK2	GVDD	MA0	VSS	GVDD	MBA0	GVDD	VSS	VDD	VSS	CRPEVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NC	NC	NC	NC	SD_C_TX	SD_C_TX	SXCVSS	SXCVDD	R
T	VSS	VSS	MCK1	MA1	MA3	MAPAR_OUT	VSS	GVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	NC	NC	NC	NC	SXPVDD	SXPVSS	SD_C_RX	SD_C_RX	T
U	MAVDD	VSS	MCK1	GVDD	VSS	MBA1	GVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NC	NC	NC	NC	SD_D_TX	SD_D_TX	SXCVSS	SXCVDD	U
V	MVREF	VSS	MA8	MA2	MA6	MCKE1	VSS	GVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	NC	NC	NC	NC	NC	NC	SD_D_RX	SD_D_RX	V
W	VSS	VSS	MA5	VSS	GVDD	MMD1C1	GVDD	VSS	VDD	VSS	M3VDD	VSS	M3VDD	VSS	M3VDD	VSS	CPRIVDD	VSS	VDD	VSS	VDD	VSS	NC	NC	NC	SD_PLL1_AVDD	SD_PLL1_AVDD	NC	SXCVSS	SXCVDD	W
Y	MA11	MA9	MA12	MA7	NC	MMD1C0	VSS	GVDD	VSS	VDD	VSS	M3VDD	VSS	M3VDD	VSS	CPRIVDD	VSS	CPRIVDD	VSS	VDD	VSS	NC	NC	NC	NC	NC	NC	NC	SD_REF_CLK1	SD_REF_CLK1	Y
AA	MDQ58	VSS	MA14	GVDD	VSS	MA15	MCKE0	VSS	GVDD	VSS	M3VDD	VSS	M3VDD	VSS	CPRIVDD	VSS	CPRIVDD	VSS	CPRIVDD	NC	SD_IMP_CAL_TX	NC	NC	NC	SD_E_TX	SD_E_TX	SXCVSS	SXCVDD	AA		
AB	MDQ58	MDM8	MECC2	MECC1	NC	MAPAR_IN	MBA2	MDQ2	MDQ1	MDQ0	VSS	M3VDD	VSS	M3VDD	VSS	CPRIVDD	VSS	CPRIVDD	NC	NC	NC	NC	NC	NC	NC	SXPVDD	SXPVSS	SD_E_RX	SD_E_RX	AB	
AC	VSS	GVDD	MECC4	VSS	GVDD	MDQ25	VSS	GVDD	MDQ3	VSS	GVDD	VSS	M3VDD	VSS	CPRIVDD	VSS	NC	NC	NC	NC	NC	NC	NC	NC	NC	SD_F_TX	SD_F_TX	SXCVSS	SXCVDD	AC	
AD	MECC7	MECC6	MECC0	MECC5	MECC3	MDQ24	MDM0	MDQ50	MDQ50	MDQ4	MDQ6	VSS	VSS	VSS	VSS	VSS	NC	SD_PLL2_AVDD	NC	NC	NC	NC	NC	NC	NC	SXPVDD	SXPVSS	SD_F_RX	SD_F_RX	AD	
AE	MDQ52	VSS	MDQ18	GVDD	VSS	MDQ29	GVDD	VSS	MDQ5	GVDD	VSS	MDQ9	VSS	VSS	VSS	VSS	NC	SD_PLL2_AGND	NC	SD_I_TX	SXPVDD	SD_I_TX	SXPVDD	NC	SD_G_TX	SD_G_TX	SXCVSS	SXCVDD	AE		
AF	MDQ52	MDQ17	MDQ21	MDQ16	MDQ30	MDQ27	MDQ28	MDQ7	MDQ14	MDQ11	MDQ8	MDQ10	VSS	VSS	VSS	VSS	NC	NC	NC	SD_I_TX	SXPVSS	SD_I_TX	SXPVSS	NC	SXPVDD	SXPVSS	SD_G_RX	SD_G_RX	AF		
AG	VSS	GVDD	MDQ22	VSS	GVDD	MDQ26	VSS	GVDD	MDQ13	VSS	GVDD	MDQ12	VSS	VSS	VSS	VSS	NC	SXCVSS	SD_REF_CLK2	SXCVSS	SD_I_RX	SXCVSS	SD_I_RX	SXCVSS	SD_H_TX	SD_H_TX	SXCVSS	SXCVDD	AG		
AH	MDQ20	MDQ19	MDQ23	MDM2	MDQ53	MDM3	MDQ31	MDQ51	MDQ15	MDM1	VSS	PLLO_AVDD	PLL1_AVDD	PLL2_AVDD	NC	SXCVDD	SD_REF_CLK2	SXCVDD	SD_I_RX	SXCVDD	SD_I_RX	SXCVDD	SXPVDD	SXPVSS	SD_H_RX	SD_H_RX	AH				
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28			

Figure 2. MSC8157 FC-PBGA Package, Top View

NOTE

See [Figure 31](#) as a reference for correct ball grid layout.

2.2 Signal Lists

[Table 1](#) presents the signal list sorted by ball number. [Table 2](#) presents the signal list by signal name. When designing a board, make sure that the power rail for each signal is appropriately considered. The specified power rail must be tied to the voltage level specified in this document if any of the related signal functions are used (active)

NOTE

The information in [Table 1](#) distinguishes among three concepts. First, the power pins are the balls of the device package used to supply specific power levels for different device subsystems (as opposed to signals). Second, the power rails are the electrical lines on the board that transfer power from the voltage regulators to the device. They are indicated here as the reference power rails for signal lines; therefore, the actual power inputs are listed as N/A with regard to the power rails. Third, symbols used in these tables are the names for the voltage levels (absolute, recommended, and so on) and not the power supplies themselves.

Table 1. Signal List by Ball Number

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
A2	VSS	Ground	N/A
A3	MDQ57	I/O	GVDD
A4	GVDD	Power	N/A
A5	VSS	Ground	N/A
A6	MDQ63	I/O	GVDD
A7	GVDD	Power	N/A
A8	NC	Non-user	N/A
A9	NC	Non-user	N/A
A10	NC	Non-user	N/A
A11	NC	Non-user	N/A
A12	NC	Non-user	N/A
A13	CLKOUT	O	QVDD
A14	EE0	I	QVDD
A15	VSS	Ground	N/A
A16	MCLKIN (optional)	I	QVDD
A17	VSS	Ground	N/A
A18	CLKIN	I	QVDD
A19	VSS	Ground	N/A
A20	GPIO29/UART_TXD/CP_LOS2	I/O	NVDD
A21	GPIO31/I2C_SDA	I/O	NVDD
A22	GE1_TX_CTL	O	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
A23	GE1_GTX_CLK	O	NVDD
A24	GE1_TD0	O	NVDD
A25	GE1_TX_CLK	I	NVDD
A26	GE1_TD2	O	NVDD
A27	GE1_TD1	O	NVDD
A28	GE1_TD3	O	NVDD
B1	MDQ60	I/O	GVDD
B2	MDQ59	I/O	GVDD
B3	MDQS7	I/O	GVDD
B4	MDQS7	I/O	GVDD
B5	MDQ62	I/O	GVDD
B6	MDQ58	I/O	GVDD
B7	MDQ56	I/O	GVDD
B8	NC	Non-user	N/A
B9	VSS	Ground	N/A
B10	NC	Non-user	N/A
B11	VSS	Ground	N/A
B12	NC	Non-user	N/A
B13	VSS	Ground	N/A
B14	TDO	O	QVDD
B15	TMS	I	QVDD
B16	VSS	Ground	N/A
B17	VSS	Ground	N/A
B18	VSS	Ground	N/A
B19	VSS	Ground	N/A
B20	GE2_TX_CLK	I	NVDD
B21	VSS	Ground	N/A
B22	VSS	Non-user	N/A
B23	VSS	Ground	N/A
B24	GPIO25/TMR2/RCW_SRC1	I/O	NVDD
B25	VSS	Ground	N/A
B26	GE_MDC	O	NVDD
B27	VSS	Ground	N/A
B28	GPIO18/SPI_MOSI/CP_LOS4	I/O	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
C1	VSS	Ground	N/A
C2	GVDD	Power	N/A
C3	MDQ61	I/O	GVDD
C4	VSS	Ground	N/A
C5	GVDD	Power	N/A
C6	MDM7	O	GVDD
C7	VSS	Ground	N/A
C8	NC	Non-user	N/A
C9	NC	Non-user	N/A
C10	NC	Non-user	N/A
C11	NC	Non-user	N/A
C12	NC	Non-user	N/A
C13	NC	Non-user	N/A
C14	EE1	O	QVDD
C15	NC	Non-user	N/A
C16	DFT_TEST	I	QVDD
C17	$\overline{\text{PORESET}}$	I	QVDD
C18	VSS	Ground	N/A
C19	GPIO15/DDN0/IRQ15/RC15	I/O	NVDD
C20	GE2_TD2/CP_LOS3	I/O	NVDD
C21	GE2_GTX_CLK/CP_LOS4	I/O	NVDD
C22	GE2_TX_CTL	O	NVDD
C23	GE2_TD1	O	NVDD
C24	GE2_TD0	O	NVDD
C25	GPIO30/I2C_SCL	I/O	NVDD
C26	GPIO20/SPI_SL/CP_LOS6	I/O	NVDD
C27	GE_MDIO	I/O	NVDD
C28	GPIO21/TMR6	I/O	NVDD
D1	MDQ49	I/O	GVDD
D2	MDQ48	I/O	GVDD
D3	$\overline{\text{MDQS6}}$	I/O	GVDD
D4	MDQS6	I/O	GVDD
D5	MDQ50	I/O	GVDD
D6	MDQ51	I/O	GVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
D7	MDQ52	I/O	GVDD
D8	NC	Non-user	N/A
D9	VSS	Ground	N/A
D10	NC	Non-user	N/A
D11	VSS	Ground	N/A
D12	NC	Non-user	N/A
D13	VSS	Ground	N/A
D14	NC	Non-user	N/A
D15	NMI	I	QVDD
D16	VSS	Ground	N/A
D17	HRESET_IN	I	QVDD
D18	VSS	Ground	N/A
D19	VSS	Non-user	N/A
D20	GPIO13/IRQ13/RC13	I/O	NVDD
D21	NVDD	Power	N/A
D22	GE2_TD3/CP_LOS5	I/O	NVDD
D23	VSS	Ground	N/A
D24	GPIO5/IRQ5/RC5/CP_SYNC4	I/O	NVDD
D25	NVDD	Power	N/A
D26	GPIO16/TMR5/RC16	I/O	NVDD
D27	VSS'	Ground	N/A
D28	GPIO10/IRQ10/RC10	I/O	NVDD
E1	MDQ53	I/O	GVDD
E2	VSS	Ground	N/A
E3	MDQ55	I/O	GVDD
E4	GVDD	Power	N/A
E5	VSS	Ground	N/A
E6	MDQ54	I/O	GVDD
E7	GVDD	Power	N/A
E8	VSS	Ground	N/A
E9	NC	Non-user	N/A
E10	NC	Non-user	N/A
E11	NC	Non-user	N/A
E12	NC	Non-user	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
E13	NC	Non-user	N/A
E14	NC	Non-user	N/A
E15	INT_OUT/CP_TX_INT	O	QVDD
E16	HRESET	I/O	QVDD
E17	TCK	I	QVDD
E18	VSS	Ground	N/A
E19	NVDD	Power	N/A
E20	GE2_RD3/CP_LOS2	I	NVDD
E21	VSS	Ground	N/A
E22	VSS	Non-user	N/A
E23	NVDD	Power	N/A
E24	GPIO27/TMR4/RCW_SRC0	I/O	NVDD
E25	VSS	Ground	N/A
E26	GPIO0/IRQ0/RC0/CP_SYNC1	I/O	NVDD
E27	GPIO17/SPI_SCK/CP_LOS3	I/O	NVDD
E28	GPIO1/IRQ1/RC1/CP_SYNC2	I/O	NVDD
F1	MDQ40	I/O	GVDD
F2	MDQ41	I/O	GVDD
F3	MDQS5	I/O	GVDD
F4	MDQS5	I/O	GVDD
F5	MDQ43	I/O	GVDD
F6	MDQ47	I/O	GVDD
F7	MDM6	O	GVDD
F8	VDD	Power	N/A
F9	VSS	Ground	N/A
F10	VDD	Power	N/A
F11	NC	Non-user	N/A
F12	NC	Non-user	N/A
F13	VSS	Ground	N/A
F14	NC	Non-user	N/A
F15	NMI_OUT/CP_RX_INT	O	QVDD
F16	VSS	Ground	N/A
F17	TDI	I	QVDD
F18	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
F19	GE2_RD2/CP_LOS1	I	NVDD
F20	GE2_RX_CTL	I	NVDD
F21	GE2_RD0/CP_LOS6	I	NVDD
F22	GE2_RX_CLK	I	NVDD
F23	GE2_RD1	I	NVDD
F24	GPIO26/TMR3	I/O	NVDD
F25	GPIO6/IRQ6/RC6/CP_SYNC5	I/O	NVDD
F26	GPIO22	I/O	NVDD
F27	GPIO23/TMR0/BOOT_SPI_SL	I/O	NVDD
F28	GPIO8/IRQ8/RC8	I/O	NVDD
G1	VSS	Ground	N/A
G2	GVDD	Power	N/A
G3	MDM5	O	GVDD
G4	VSS	Ground	N/A
G5	GVDD	Power	N/A
G6	MDQ46	I/O	GVDD
G7	VDD	Power	N/A
G8	VSS	Ground	N/A
G9	VDD	Power	N/A
G10	VSS	Ground	N/A
G11	NC	Non-user	N/A
G12	NC	Non-user	N/A
G13	NC	Non-user	N/A
G14	NC	Non-user	N/A
G15	QVDD	Power	N/A
G16	STOP_BS	I	QVDD
G17	TRST	I	QVDD
G18	VSS	Ground	N/A
G19	GPIO28/UART_RXD/CP_LOS1	I/O	NVDD
G20	GE1_RD3	I	NVDD
G21	GE1_RD2	I	NVDD
G22	GE1_RX_CLK	I	NVDD
G23	VSS	Ground	N/A
G24	GE1_RX_CTL	I	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
G25	NVDD	Power	N/A
G26	GPIO19/SPI_MISO/CP_LOS5	I/O	NVDD
G27	VSS	Ground	N/A
G28	GPIO11/ $\overline{\text{IRQ11}}$ /RC11	I/O	NVDD
H1	MDQ38	I/O	GVDD
H2	$\overline{\text{MDQS4}}$	I/O	GVDD
H3	MDQS4	I/O	GVDD
H4	MDQ44	I/O	GVDD
H5	MDQ45	I/O	GVDD
H6	MDQ42	I/O	GVDD
H7	VSS	Ground	N/A
H8	VDD	Power	N/A
H9	VSS	Ground	N/A
H10	VDD	Power	N/A
H11	VSS	Ground	N/A
H12	VSS	Non-user	N/A
H13	NC	Non-user	N/A
H14	QVDD	Power	N/A
H15	VSS	Ground	N/A
H16	VDD	Power	N/A
H17	VSS	Ground	N/A
H18	VDD	Power	N/A
H19	VSS	Ground	N/A
H20	NVDD	Power	N/A
H21	VSS	Ground	N/A
H22	GE1_RD0	I	NVDD
H23	NVDD	Power	N/A
H24	GE1_RD1	I	NVDD
H25	VSS	Ground	N/A
H26	GPIO14/DRQ0/ $\overline{\text{IRQ14}}$ /RC14	I/O	NVDD
H27	NVDD	Power	N/A
H28	GPIO12/ $\overline{\text{IRQ12}}$ /RC12	I/O	NVDD
J1	MDQ37	I/O	GVDD
J2	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
J3	MDQ35	I/O	GVDD
J4	GVDD	Power	N/A
J5	MDQ33	I/O	GVDD
J6	MDQ36	I/O	GVDD
J7	VDD	Power	N/A
J8	VSS	Ground	N/A
J9	VDD	Power	N/A
J10	VSS	Ground	N/A
J11	VDD	Power	N/A
J12	VSS	Ground	N/A
J13	VDD	Power	N/A
J14	VSS	Ground	N/A
J15	VDD	Power	N/A
J16	VSS	Ground	N/A
J17	VDD	Power	N/A
J18	VSS	Ground	N/A
J19	VDD	Power	N/A
J20	VSS	Ground	N/A
J21	NVDD	Power	N/A
J22	GPIO24/TMR1/RCW_SRC2	I/O	NVDD
J23	GPIO9/IRQ9/RC9	I/O	NVDD
J24	RCW_LSEL0/RC17	I/O	NVDD
J25	RCW_LSEL3/RC20	I/O	NVDD
J26	RCW_LSEL2/RC19	I/O	NVDD
J27	RC21	I	NVDD
J28	GPIO3/DRQ1/IRQ3/RC3	I/O	NVDD
K1	MCAS	O	GVDD
K2	MCS0	O	GVDD
K3	MCS1	O	GVDD
K4	MDQ39	I/O	GVDD
K5	MDQ32	I/O	GVDD
K6	MDQ34	I/O	GVDD
K7	VSS	Ground	N/A
K8	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
K9	VSS	Ground	N/A
K10	VDD	Power	N/A
K11	VSS	Ground	N/A
K12	VDD	Power	N/A
K13	VSS	Ground	N/A
K14	VDD	Power	N/A
K15	VSS	Ground	N/A
K16	VDD	Power	N/A
K17	VSS	Ground	N/A
K18	VDD	Power	N/A
K19	VSS	Ground	N/A
K20	VDD	Power	N/A
K21	VSS	Ground	N/A
K22	GPIO4/DDN1/IRQ4/RC4	I/O	NVDD
K23	VSS	Ground	N/A
K24	RCW_LSEL1/RC18	I/O	NVDD
K25	NVDD	Power	N/A
K26	GPIO7/IRQ7/RC7/CP_SYNC6	I/O	NVDD
K27	VSS	Ground	N/A
K28	GPIO2/IRQ2/RC2/CP_SYNC3	I/O	NVDD
L1	VSS	Ground	N/A
L2	GVDD	Power	N/A
L3	NC	Non-user	N/A
L4	VSS	Ground	N/A
L5	GVDD	Power	N/A
L6	MDM4	O	GVDD
L7	VDD	Power	N/A
L8	VSS	Ground	N/A
L9	VDD	Power	N/A
L10	VSS	Ground	N/A
L11	VDD	Power	N/A
L12	VSS	Ground	N/A
L13	VDD	Power	N/A
L14	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
L15	VDD	Power	N/A
L16	VSS	Ground	N/A
L17	VDD	Power	N/A
L18	VSS	Ground	N/A
L19	VDD	Power	N/A
L20	VSS	Ground	N/A
L21	NVDD	Power	N/A
L22	NC	NC	N/A
L23	NC	NC	N/A
L24	VSS	Non-user	N/A
L25	VSS	Non-user	N/A
L26	VSS	Non-user	N/A
L27	SXCVSS	Ground	N/A
L28	SXCVDD	Power	N/A
M1	$\overline{\text{MCK0}}$	O	GVDD
M2	MCK0	O	GVDD
M3	MA13	O	GVDD
M4	$\overline{\text{MWE}}$	O	GVDD
M5	NC	Non-user	N/A
M6	NC	Non-user	N/A
M7	VSS	Ground	N/A
M8	VDD	Power	N/A
M9	VSS	Ground	N/A
M10	VDD	Power	N/A
M11	VSS	Ground	N/A
M12	VDD	Power	N/A
M13	VSS	Ground	N/A
M14	VDD	Power	N/A
M15	VSS	Ground	N/A
M16	VDD	Power	N/A
M17	VSS	Ground	N/A
M18	VDD	Power	N/A
M19	VSS	Ground	N/A
M20	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
M21	NC	NC	N/A
M22	NC	NC	N/A
M23	SD_A_TX	O	SXPVDD
M24	$\overline{\text{SD_A_TX}}$	O	SXPVDD
M25	SXPVDD	Power	N/A
M26	SXPVSS	Ground	N/A
M27	$\overline{\text{SD_A_RX}}$	I	SXCVDD
M28	SD_A_RX	I	SXCVDD
N1	MRAS	O	GVDD
N2	VSS	Ground	N/A
N3	NC	Non-user	N/A
N4	GVDD	Power	N/A
N5	VSS	Ground	N/A
N6	MODT1	O	GVDD
N7	CRPEVDD	Power	N/A
N8	VSS	Ground	N/A
N9	CRPEVDD	Power	N/A
N10	VSS	Ground	N/A
N11	CRPEVDD	Power	N/A
N12	VSS	Ground	N/A
N13	VDD	Power	N/A
N14	VSS	Ground	N/A
N15	VDD	Power	N/A
N16	VSS	Ground	N/A
N17	VDD	Power	N/A
N18	VSS	Ground	N/A
N19	VDD	Power	N/A
N20	VSS	Ground	N/A
N21	NC	NC	N/A
N22	NC	NC	N/A
N23	SXPVDD	Power	N/A
N24	SXPVSS	Ground	N/A
N25	SD_B_TX	O	SXPVDD
N26	$\overline{\text{SD_B_TX}}$	O	SXPVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
N27	SXCVSS	Ground	N/A
N28	SXCVDD	Power	N/A
P1	MCK2	O	GVDD
P2	MA10	O	GVDD
P3	NC	Non-user	N/A
P4	MA4	O	GVDD
P5	NC	Non-user	N/A
P6	MODT0	O	GVDD
P7	VSS	Ground	N/A
P8	CRPEVDD	Power	N/A
P9	VSS	Ground	N/A
P10	CRPEVDD	Power	N/A
P11	VSS	Ground	N/A
P12	VDD	Power	N/A
P13	VSS	Ground	N/A
P14	VDD	Power	N/A
P15	VSS	Ground	N/A
P16	VDD	Power	N/A
P17	VSS	Ground	N/A
P18	VDD	Power	N/A
P19	VSS	Ground	N/A
P20	VDD	Power	N/A
P21	NC	NC	N/A
P22	SD_IMP_CAL_RX	I	SXCVDD
P23	NC	NC	N/A
P24	NC	NC	N/A
P25	SXPVDD	Power	N/A
P26	SXPVSS	Ground	N/A
P27	SD_B_RX	I	SXCVDD
P28	SD_B_RX	I	SXCVDD
R1	MCK2	O	GVDD
R2	GVDD	Power	N/A
R3	MA0	O	GVDD
R4	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
R5	GVDD	Power	N/A
R6	MBA0	O	GVDD
R7	GVDD	Power	N/A
R8	VSS	Ground	N/A
R9	VDD	Power	N/A
R10	VSS	Ground	N/A
R11	CRPEVDD	Power	N/A
R12	VSS	Ground	N/A
R13	VDD	Power	N/A
R14	VSS	Ground	N/A
R15	VDD	Power	N/A
R16	VSS	Ground	N/A
R17	VDD	Power	N/A
R18	VSS	Ground	N/A
R19	VDD	Power	N/A
R20	VSS	Ground	N/A
R21	NC	NC	N/A
R22	NC	NC	N/A
R23	NC	NC	N/A
R24	NC	NC	N/A
R25	SD_C_TX	O	SXPVDD
R26	$\overline{\text{SD_C_TX}}$	O	SXPVDD
R27	SXCVSS	Ground	N/A
R28	SXCVDD	Power	N/A
T1	VSS	Ground	N/A
T2	VSS	Ground	N/A
T3	$\overline{\text{MCK1}}$	O	GVDD
T4	MA1	O	GVDD
T5	MA3	O	GVDD
T6	MAPAR_OUT	O	GVDD
T7	VSS	Ground	N/A
T8	GVDD	Power	N/A
T9	VSS	Ground	N/A
T10	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
T11	VSS	Ground	N/A
T12	VDD	Power	N/A
T13	VSS	Ground	N/A
T14	VDD	Power	N/A
T15	VSS	Ground	N/A
T16	VDD	Power	N/A
T17	VSS	Ground	N/A
T18	VDD	Power	N/A
T19	VSS	Ground	N/A
T20	VDD	Power	N/A
T21	NC	NC	N/A
T22	NC	Non-user	N/A
T23	NC	Non-user	N/A
T24	NC	NC	N/A
T25	SXPVDD	Power	N/A
T26	SXPVSS	Ground	N/A
T27	$\overline{\text{SD_C_RX}}$	I	SXCVDD
T28	SD_C_RX	I	SXCVDD
U1	MAVDD	Power	N/A
U2	VSS	Ground	N/A
U3	MCK1	O	GVDD
U4	GVDD	Power	N/A
U5	VSS	Ground	N/A
U6	MBA1	O	GVDD
U7	GVDD	Power	N/A
U8	VSS	Ground	N/A
U9	VDD	Power	N/A
U10	VSS	Ground	N/A
U11	VDD	Power	N/A
U12	VSS	Ground	N/A
U13	VDD	Power	N/A
U14	VSS	Ground	N/A
U15	VDD	Power	N/A
U16	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
U17	VDD	Power	N/A
U18	VSS	Ground	N/A
U19	VDD	Power	N/A
U20	VSS	Ground	N/A
U21	NC	NC	N/A
U22	NC	NC	N/A
U23	NC	NC	N/A
U24	NC	NC	N/A
U25	SD_D_TX	O	SXPVDD
U26	$\overline{\text{SD_D_TX}}$	O	SXPVDD
U27	SXCVSS	Ground	N/A
U28	SXCVDD	Power	N/A
V1	MVREF	Power	N/A
V2	VSS	Ground	N/A
V3	MA8	O	GVDD
V4	MA2	O	GVDD
V5	MA6	O	GVDD
V6	MCKE1	O	GVDD
V7	VSS	Ground	N/A
V8	GVDD	Power	N/A
V9	VSS	Ground	N/A
V10	VDD	Power	N/A
V11	VSS	Ground	N/A
V12	VDD	Power	N/A
V13	VSS	Ground	N/A
V14	VDD	Power	N/A
V15	VSS	Ground	N/A
V16	VDD	Power	N/A
V17	VSS	Ground	N/A
V18	VDD	Power	N/A
V19	VSS	Ground	N/A
V20	VDD	Power	N/A
V21	NC	NC	N/A
V22	NC	NC	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
V23	NC	NC	N/A
V24	NC	NC	N/A
V25	NC	NC	N/A
V26	NC	NC	N/A
V27	$\overline{\text{SD_D_RX}}$	I	SXCVDD
V28	SD_D_RX	I	SXCVDD
W1	VSS	Ground	N/A
W2	VSS	Ground	N/A
W3	MA5	O	GVDD
W4	VSS	Ground	N/A
W5	GVDD	Power	N/A
W6	MMDIC1	I/O	GVDD
W7	GVDD	Power	N/A
W8	VSS	Ground	N/A
W9	VDD	Power	N/A
W10	VSS	Ground	N/A
W11	M3VDD	Power	N/A
W12	VSS	Ground	N/A
W13	M3VDD	Power	N/A
W14	VSS	Ground	N/A
W15	M3VDD	Power	N/A
W16	VSS	Ground	N/A
W17	CPRIVDD	Power	N/A
W18	VSS	Ground	N/A
W19	VDD	Power	N/A
W20	VSS	Ground	N/A
W21	NC	NC	N/A
W22	NC	NC	N/A
W23	NC	NC	N/A
W24	SD_PLL1_AVDD	Power	N/A
W25	SD_PLL1_AGND	Ground	N/A
W26	NC	NC	N/A
W27	SXCVSS	Ground	N/A
W28	SXCVDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
Y1	MA11	O	GVDD
Y2	MA9	O	GVDD
Y3	MA12	O	GVDD
Y4	MA7	O	GVDD
Y5	NC	Non-user	N/A
Y6	MMDIC0	I/O	GVDD
Y7	VSS	Ground	N/A
Y8	GVDD	Power	N/A
Y9	VSS	Ground	N/A
Y10	VDD	Power	N/A
Y11	VSS	Ground	N/A
Y12	M3VDD	Power	N/A
Y13	VSS	Ground	N/A
Y14	M3VDD	Power	N/A
Y15	VSS	Ground	N/A
Y16	CPRIVDD	Power	N/A
Y17	VSS	Ground	N/A
Y18	CPRIVDD	Power	N/A
Y19	VSS	Ground	N/A
Y20	VDD	Power	N/A
Y21	NC	NC	N/A
Y22	NC	NC	N/A
Y23	NC	NC	N/A
Y24	NC	NC	N/A
Y25	NC	NC	N/A
Y26	NC	NC	N/A
Y27	SD_REF_CLK1	I	SXCVDD
Y28	SD_REF_CLK1	I	SXCVDD
AA1	MDQS8	I/O	GVDD
AA2	VSS	Ground	N/A
AA3	MA14	O	GVDD
AA4	GVDD	Power	N/A
AA5	VSS	Ground	N/A
AA6	MA15	O	GVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
AA7	MCKE0	O	GVDD
AA8	VSS	Ground	N/A
AA9	GVDD	Power	N/A
AA10	VSS	Ground	N/A
AA11	M3VDD	Power	N/A
AA12	VSS	Ground	N/A
AA13	M3VDD	Power	N/A
AA14	VSS	Ground	N/A
AA15	CPRIVDD	Power	N/A
AA16	VSS	Ground	N/A
AA17	CPRIVDD	Power	N/A
AA18	VSS	Ground	N/A
AA19	CPRIVDD	Power	N/A
AA20	NC	NC	N/A
AA21	SD_IMP_CAL_TX	I	SXPVDD
AA22	NC	NC	N/A
AA23	NC	NC	N/A
AA24	NC	NC	N/A
AA25	SD_E_TX	O	SXPVDD
AA26	$\overline{\text{SD_E_TX}}$	O	SXPVDD
AA27	SXCVSS	Ground	N/A
AA28	SXCVDD	Power	N/A
AB1	$\overline{\text{MDQS8}}$	I/O	GVDD
AB2	MDM8	O	GVDD
AB3	MECC2	I/O	GVDD
AB4	MECC1	I/O	GVDD
AB5	NC	Non-user	N/A
AB6	MAPAR_IN	I	GVDD
AB7	MBA2	O	GVDD
AB8	MDQ2	I/O	GVDD
AB9	MDQ1	I/O	GVDD
AB10	MDQ0	I/O	GVDD
AB11	VSS	Ground	N/A
AB12	M3VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
AB13	VSS	Ground	N/A
AB14	M3VDD	Power	N/A
AB15	VSS	Ground	N/A
AB16	CPRIVDD	Power	N/A
AB17	VSS	Ground	N/A
AB18	CPRIVDD	Power	N/A
AB19	NC	NC	N/A
AB20	NC	Non-user	N/A
AB21	NC	NC	N/A
AB22	NC	NC	N/A
AB23	NC	NC	N/A
AB24	NC	NC	N/A
AB25	SXPVDD	Power	N/A
AB26	SXPVSS	Ground	N/A
AB27	SD_E_RX	I	SXCVDD
AB28	SD_E_RX	I	SXCVDD
AC1	VSS	Ground	N/A
AC2	GVDD	Power	N/A
AC3	MECC4	I/O	GVDD
AC4	VSS	Ground	N/A
AC5	GVDD	Power	N/A
AC6	MDQ25	I/O	GVDD
AC7	VSS	Ground	N/A
AC8	GVDD	Power	N/A
AC9	MDQ3	I/O	GVDD
AC10	VSS	Ground	N/A
AC11	GVDD	Power	N/A
AC12	VSS	Ground	N/A
AC13	M3VDD	Power	N/A
AC14	VSS	Ground	N/A
AC15	CPRIVDD	Power	N/A
AC16	VSS	Ground	N/A
AC17	NC	NC	N/A
AC18	NC	NC	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
AC19	NC	NC	N/A
AC20	NC	Non-user	N/A
AC21	NC	NC	N/A
AC22	NC	NC	N/A
AC23	NC	NC	N/A
AC24	NC	NC	N/A
AC25	SD_F_TX	O	SXPVDD
AC26	$\overline{\text{SD_F_TX}}$	O	SXPVDD
AC27	SXCVSS	Ground	N/A
AC28	SXCVDD	Power	N/A
AD1	MECC7	I/O	GVDD
AD2	MECC6	I/O	GVDD
AD3	MECC0	I/O	GVDD
AD4	MECC5	I/O	GVDD
AD5	MECC3	I/O	GVDD
AD6	MDQ24	I/O	GVDD
AD7	MDM0	O	GVDD
AD8	$\overline{\text{MDQS0}}$	I/O	GVDD
AD9	MDQS0	I/O	GVDD
AD10	MDQ4	I/O	GVDD
AD11	MDQ6	I/O	GVDD
AD12	VSS	Non-user	N/A
AD13	VSS	Non-user	N/A
AD14	VSS	Non-user	N/A
AD15	VSS	Ground	N/A
AD16	VSS	Ground	N/A
AD17	NC	NC	N/A
AD18	SD_PLL2_AVDD	Power	N/A
AD19	NC	NC	N/A
AD20	NC	NC	N/A
AD21	NC	NC	N/A
AD22	NC	NC	N/A
AD23	NC	NC	N/A
AD24	NC	NC	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ³	Power Rail Name
AD25	SXPVDD	Power	N/A
AD26	SXPVSS	Ground	N/A
AD27	SD_F_RX	I	SXCVDD
AD28	SD_F_RX	I	SXCVDD
AE1	MDQS2	I/O	GVDD
AE2	VSS	Ground	N/A
AE3	MDQ18	I/O	GVDD
AE4	GVDD	Power	N/A
AE5	VSS	Ground	N/A
AE6	MDQ29	I/O	GVDD
AE7	GVDD	Power	N/A
AE8	VSS	Ground	N/A
AE9	MDQ5	I/O	GVDD
AE10	GVDD	Power	N/A
AE11	VSS	Ground	N/A
AE12	MDQ9	I/O	GVDD
AE13	VSS	Non-user	N/A
AE14	VSS	Ground	N/A
AE15	VSS	Ground	N/A
AE16	VSS	Ground	N/A
AE17	NC	NC	N/A
AE18	SD_PLL2_AGND	Ground	N/A
AE19	NC	NC	N/A
AE20	SD_J_TX	O	SXPVDD
AE21	SXPVDD	Power	N/A
AE22	SD_I_TX	O	SXPVDD
AE23	SXPVDD	Power	N/A
AE24	NC	NC	N/A
AE25	SD_G_TX	O	SXPVDD
AE26	SD_G_TX	O	SXPVDD
AE27	SXCVSS	Ground	N/A
AE28	SXCVDD	Power	N/A
AF1	MDQS2	I/O	GVDD
AF2	MDQ17	I/O	GVDD