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# SYNCHRONOUS DRAM MODULE

**MT8LSDT1664A – 128MB**  
**MT16LSDT3264A – 256MB**

For the latest data sheet, please refer to the Micron® Web site: [www.micron.com/products/modules](http://www.micron.com/products/modules)

## Features

- 168-pin, dual in-line memory module (DIMM)
- PC100- and PC133-compliant
- Utilizes 125 MHz and 133 MHz SDRAM components
- Unbuffered
- 128MB (16 Meg x 64) and 256MB (32 Meg x 64)
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE and Auto Refresh Modes
- Self Refresh Mode: 64ms, 4,096-cycle refresh (15.625µs refresh interval)
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)
- Gold edge contacts

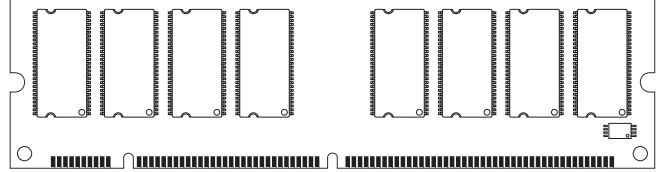
**Table 1: Timing Parameters**

CL = CAS (READ) latency

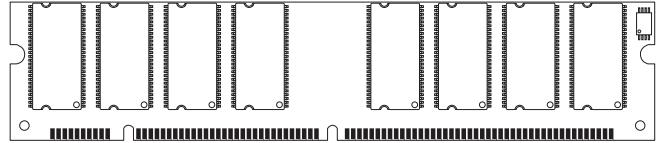
| MODULE MARKING | CLOCK FREQUENCY | ACCESS TIME |        | SETUP TIME | HOLD TIME |
|----------------|-----------------|-------------|--------|------------|-----------|
|                |                 | CL = 2      | CL = 3 |            |           |
| -13E           | 133 MHz         | 5.4ns       | –      | 1.5        | 0.8       |
| -133           | 133 MHz         | –           | 5.4ns  | 1.5        | 0.8       |
| -10E           | 100 MHz         | 9ns         | 7.5ns  | 2ns        | 1ns       |

**Figure 1: 168-Pin DIMM (MO-161)**

Standard 1.375in. (34.93mm)



Low Profile 1.125in. (28.58mm)



## Options

## Marking

- Frequency/ CAS Latency
  - 133 MHz/ CL = 2 -13E
  - 133 MHz/ CL = 3 -133
  - 100 MHz/ CL = 2 -10E
- PCB
  - Standard 1.375in. (34.93mm)
  - Low-Profile 1.125in. (28.58mm)<sup>1</sup>

NOTE: 1. Contact Micron for product availability.

**Table 2: Address Table**

|                      | 128MB              | 256MB                  |
|----------------------|--------------------|------------------------|
| Refresh Count        | 4K                 | 4K                     |
| Device Banks         | 4 (BA0, BA1)       | 4 (BA0, BA1)           |
| Device Configuration | 128Mb (16 Meg x 8) | 128Mb (16 Meg x 8)     |
| Row Addressing       | 4K (A0–A11)        | 4K (A0–A11)            |
| Column Addressing    | 1K (A0–A9)         | 1K (A0–A9)             |
| Module Banks         | 1 (S0#, S2#)       | 2 (S0#, S2#; S1#, S3#) |



**Table 3: Part Numbers**

| PART NUMBER         | MODULE DENSITY | CONFIGURATION | SYSTEM BUS SPEED |
|---------------------|----------------|---------------|------------------|
| MT8LSDT1664AG-13E_  | 128MB          | 16 Meg x 64   | 133 MHz          |
| MT8LSDT1664AY-13E_  | 128MB          | 16 Meg x 64   | 133 MHz          |
| MT8LSDT1664AG-133_  | 128MB          | 16 Meg x 64   | 133 MHz          |
| MT8LSDT1664AY-133_  | 128MB          | 16 Meg x 64   | 133 MHz          |
| MT8LSDT1664AG-10E_  | 128MB          | 16 Meg x 64   | 100 MHz          |
| MT8LSDT1664AY-10E_  | 128MB          | 16 Meg x 64   | 100 MHz          |
| MT16LSDT3264AG-13E_ | 256MB          | 32 Meg x 64   | 133 MHz          |
| MT16LSDT3264AY-13E_ | 256MB          | 32 Meg x 64   | 133 MHz          |
| MT16LSDT3264AG-133_ | 256MB          | 32 Meg x 64   | 133 MHz          |
| MT16LSDT3264AY-133_ | 256MB          | 32 Meg x 64   | 133 MHz          |
| MT16LSDT3264AG-10E_ | 256MB          | 32 Meg x 64   | 100 MHz          |
| MT16LSDT3264AY-10E_ | 256MB          | 32 Meg x 64   | 100 MHz          |

**NOTE:**

The designators for component and PCB revision are the last two characters of each part number. Consult factory for current revision codes. Example: MT16LSDT3264AG-133B1.

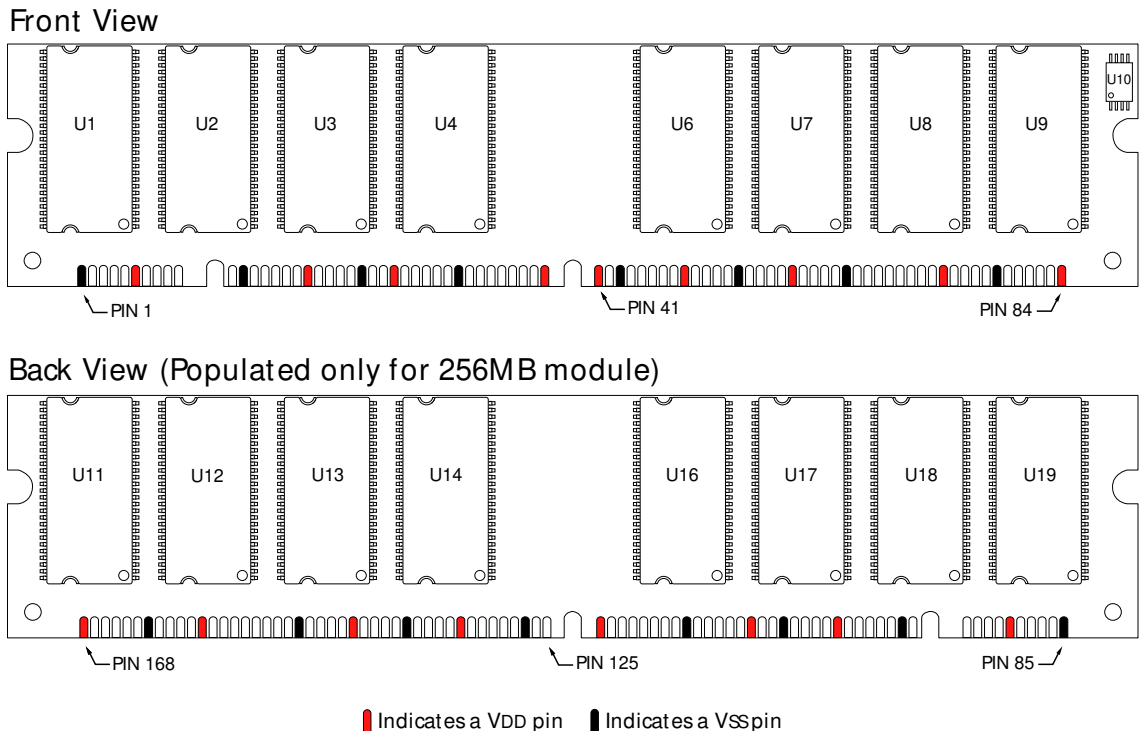
**Table 4: Pin Assignment  
(168-Pin DIMM Front)**

| PIN | SYMBOL          | PIN | SYMBOL           | PIN | SYMBOL           | PIN | SYMBOL          |
|-----|-----------------|-----|------------------|-----|------------------|-----|-----------------|
|     | V <sub>SS</sub> | 22  | NC               | 43  | V <sub>SS</sub>  | 64  | V <sub>SS</sub> |
| 2   | DQ0             | 23  | V <sub>SS</sub>  | 44  | NC               | 65  | DQ21            |
| 3   | DQ1             | 24  | NC               | 45  | S <sub>2</sub> # | 66  | DQ22            |
| 4   | DQ2             | 25  | NC               | 46  | DQMB2            | 67  | DQ23            |
| 5   | DQ3             | 26  | V <sub>DD</sub>  | 47  | DQMB3            | 68  | V <sub>SS</sub> |
| 6   | V <sub>DD</sub> | 27  | WE#              | 48  | NC               | 69  | DQ24            |
| 7   | DQ4             | 28  | DQMB0            | 49  | V <sub>DD</sub>  | 70  | DQ25            |
| 8   | DQ5             | 29  | DQMB1            | 50  | NC               | 71  | DQ26            |
| 9   | DQ6             | 30  | S <sub>0</sub> # | 51  | NC               | 72  | DQ27            |
| 10  | DQ7             | 31  | NC               | 52  | NC               | 73  | V <sub>DD</sub> |
| 11  | DQ8             | 32  | V <sub>SS</sub>  | 53  | NC               | 74  | DQ28            |
| 12  | V <sub>SS</sub> | 33  | A0               | 54  | V <sub>SS</sub>  | 75  | DQ29            |
| 13  | DQ9             | 34  | A2               | 55  | DQ16             | 76  | DQ30            |
| 14  | DQ10            | 35  | A4               | 56  | DQ17             | 77  | DQ31            |
| 15  | DQ11            | 36  | A6               | 57  | DQ18             | 78  | V <sub>SS</sub> |
| 16  | DQ12            | 37  | A8               | 58  | DQ19             | 79  | CK2             |
| 17  | DQ13            | 38  | A10              | 59  | V <sub>DD</sub>  | 80  | NC              |
| 18  | V <sub>DD</sub> | 39  | BA1              | 60  | DQ20             | 81  | WP              |
| 19  | DQ14            | 40  | V <sub>DD</sub>  | 61  | NC               | 82  | SDA             |
| 20  | DQ15            | 41  | V <sub>DD</sub>  | 62  | NC               | 83  | SCL             |
| 21  | NC              | 42  | CK0              | 63  | CKE1             | 84  | V <sub>DD</sub> |

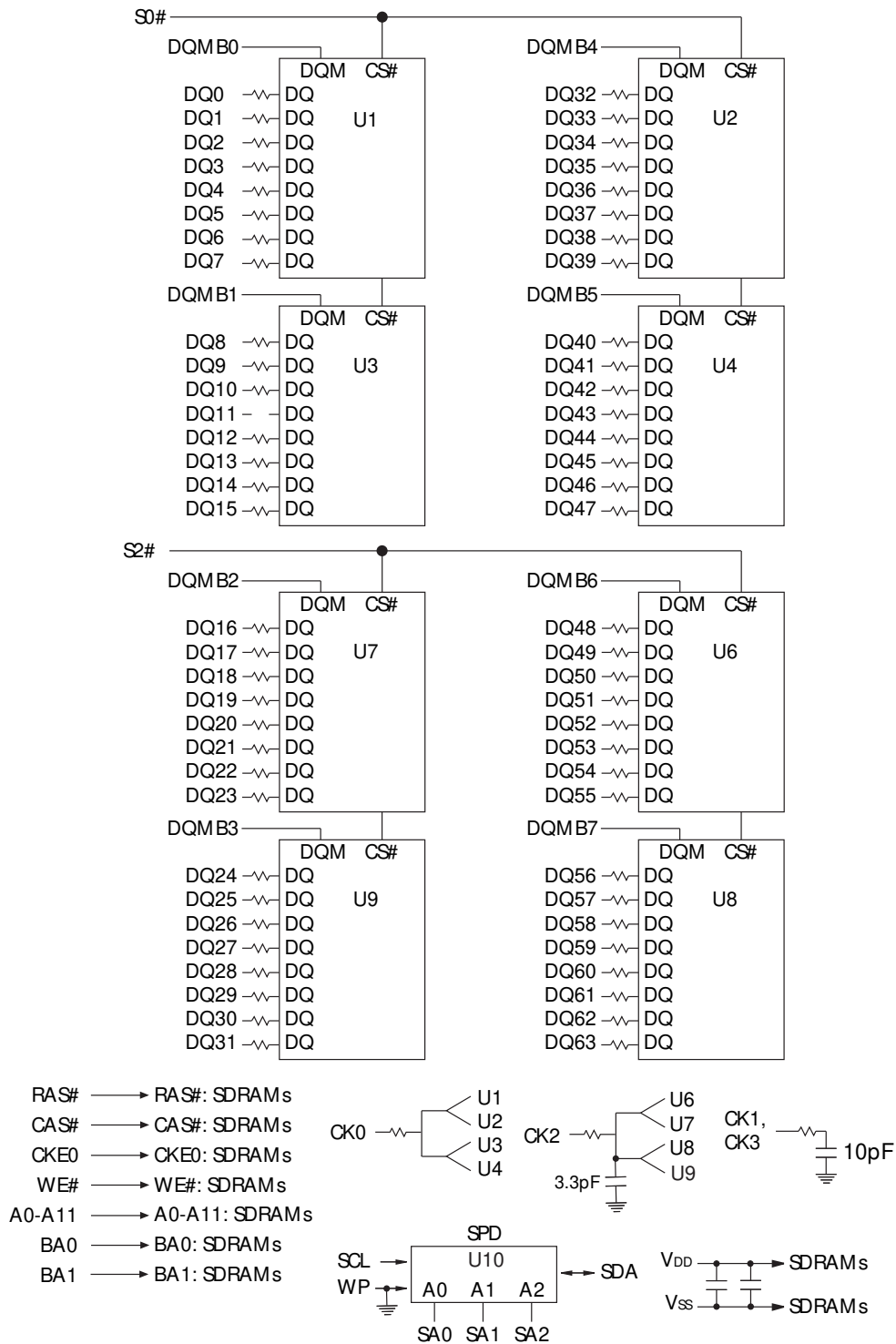
**Table 5: Pin Assignment  
(168-Pin DIMM Back)**

| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|-----|--------|-----|--------|-----|--------|-----|--------|
|     |        |     |        |     |        |     |        |
|     |        |     |        |     |        |     |        |
|     |        |     |        |     |        |     |        |
|     |        |     |        |     |        |     |        |
|     |        |     |        |     |        |     |        |
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|     |        |     |        |     |        |     |        |
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|     |        |     |        |     |        |     |        |
|     |        |     |        |     |        |     |        |
|     |        |     |        |     |        |     |        |
|     |        |     |        |     |        |     |        |

**Figure 2: 168-Pin DIMM Pin Locations**



### Functional Block Diagram – 128MB

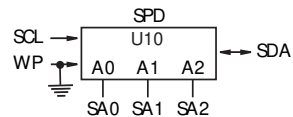
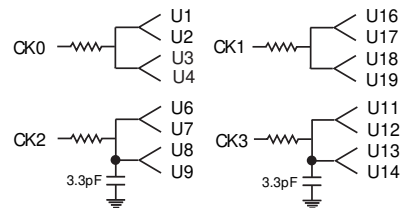
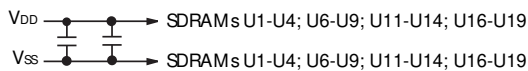
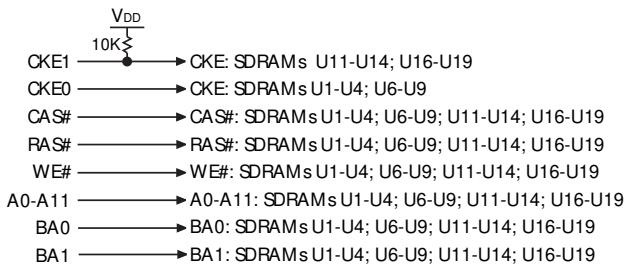
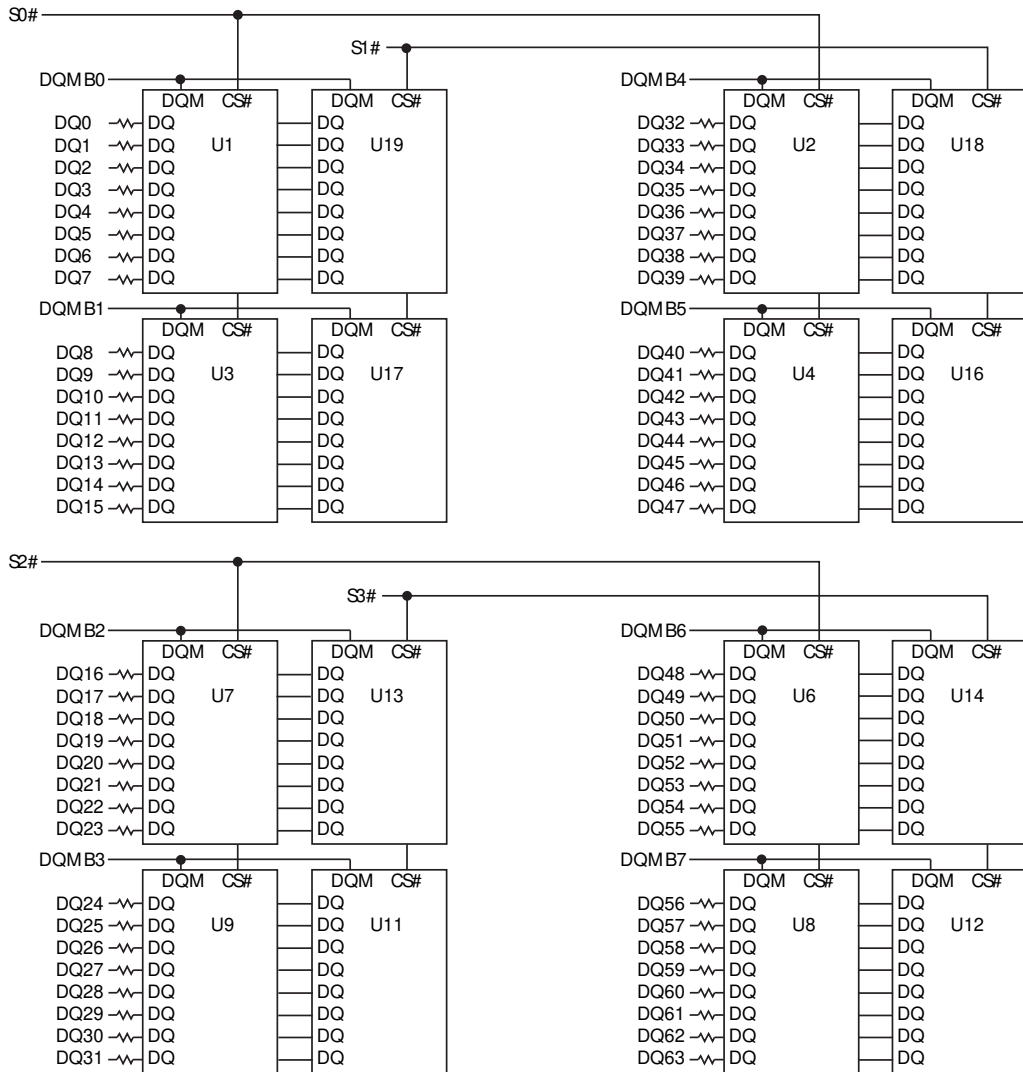


**NOTE:**

1. All resistor values are 10Ω unless otherwise specified.
2. Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part numbering guide at [www.micron.com/numberguide](http://www.micron.com/numberguide).

Standard modules use the following SDRAM devices:  
MT48LC16M8A2TG

Lead-free modules use the following SDRAM devices:  
MT48LC16M8A2P



**NOTE:**

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Standard modules use the following SDRAM devices:  
 MT48LC16M8A2TG

Lead-free modules use the following SDRAM devices:  
 MT48LC16M8A2P



Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 3 for more information

|   |                 |              |  |
|---|-----------------|--------------|--|
| 27, 115, 111  | RAS#, CAS#, WE# | Input        | Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.  |
| 42, 79, 125, 163  | CK0-CK3         | Input        | Clock: CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.  |
| 63, 128   | CKE0, CKE1      | Input        | Clock Enable: CKE0 activate (HIGH) and deactivate (LOW) the CK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all device banks idle), ACTIVE POWER-DOWN (row ACTIVE in any device bank) or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power. |
| 30, 45, 114, 129  | S0#-S3#         | Input        | Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.  |
| 28-29, 46-47, 112-113, 130-131  | DQMB0-DQMB7     | Input        | Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.  |
| 39, 122   | BA0, BA1        | Input        | Bank Address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.  |
| 33, 34, 35, 36, 37, 38, 117, 118, 119, 120, 121, 123  | A0-A11          | Input        | Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to once device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command.  |
| 83  | SCL             | Input        | Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.   |
| 165-167   | SA0-SA2         | Input        | Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.   |
| 2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161 | DQ0-DQ63        | Input/Output | Data I/O: Data bus.  |
| 82  | SDA             | Input/Output | Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.  |
| 6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168  | VDD             | Supply       | Power Supply: +3.3V ±0.3V.   |

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 3 for more information

|   |     |        |   |
|---|-----|--------|---|
| 1, 12, 23, 32, 43,<br>54, 64, 68, 78, 85,<br>96, 107, 116, 127,<br>138, 148, 152, 162                                 | Vss | Supply | Ground.   |
| 21, 22, 24, 25, 31,<br>44, 48, 50–53, 61,<br>62, 80, 81, 105,<br>106, 108, 109, 126,<br>132, 134–137,<br>145–147, 164 | NC  | –      | Not Connected: These pins are not connected on this module. |



## General Description

signals CK).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank, A0–A11 select the device row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

SDRAM modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing one of the other three device banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

SDRAM modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb SDRAM component data sheets.

## Serial Presence-Detect Operation

SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses.

## Initialization

DD and VDDQ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100 $\mu$ s delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100 $\mu$ s period and continuing at least through the end of this period, Command Inhibit or NOP commands should be applied.

Once the 100 $\mu$ s delay has been satisfied with at least one Command Inhibit or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO refresh cycles must be performed. After the AUTO refresh cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

## Mode Register Definition

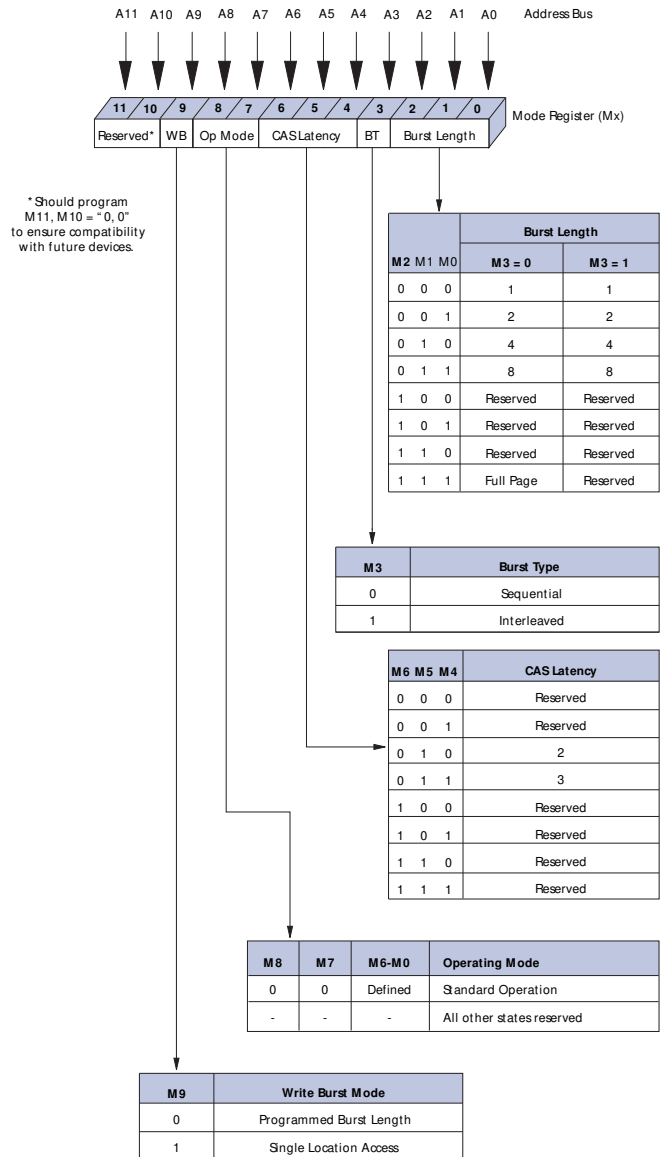
## Burst Length

in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in the Burst Definition Table. The block is uniquely selected by A1–A9 when the burst length is set to two; by A2–A9 when the burst length is set to four; and by A3–A9 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in the Table 7.

## Burst Type



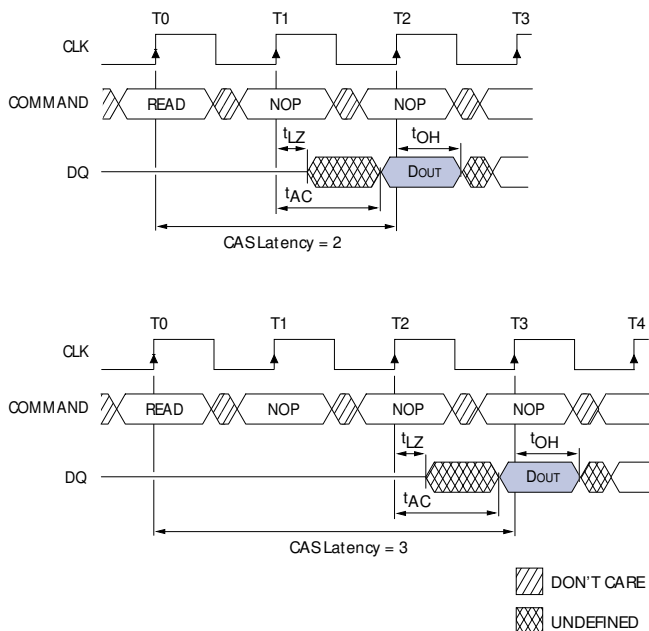
**Table 7: Burst Definition**

| BURST LENGTH | STARTING COLUMN | ORDER OF ACCESSES WITHIN A BURST ADDRESS |                    |
|--------------|-----------------|--|--------------------|
|              |                 | TYPE = SEQUENTIAL                        | TYPE = INTERLEAVED |
|              | A0              |  |                    |
|              |                 |  |                    |
|              |                 |  |                    |
|              | A1 A0           |  |                    |
|              |                 |  |                    |
|              |                 |  |                    |
|              | A2 A1 A0        |  |                    |
|              |                 |  |                    |
|              |                 |  |                    |
|              |                 |  |                    |
|              |                 |  |                    |
|              |                 |  |                    |
|              |                 |  |                    |
|              |                 |  | Not Supported      |
|              |                 | ...Cn - 1, Cn...                         |                    |

**NOTE:**

1. For full-page accesses:  $y = 1,024$ .
2. For a burst length of two, A1–A9 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2–A9 select the block-of-four burst; A0–A1 select the starting column within the block.
4. For a burst length of eight, A3–A9 select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A9 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0–A9 select the unique column to be accessed, and mode register bit M3 is ignored.

**CAS Latency Diagram**



**CAS Latency**

**Operating Mode**



**Write Burst Mode**

|  | CLOCK FREQUENCY (MHZ) |                 |
|--|-----------------------|-----------------|
|  | CAS LATENCY = 2       | CAS LATENCY = 3 |
|  | ≤                     | ≤               |
|  | ≤                     | ≤               |
|  | ≤                     | ≤               |

**Table 9: SDRAM Commands and DQMB Operation Truth Table**

| NAME (FUNCTION)  | CS# | RAS# | CAS# | WE# | DQMB | ADDR     | DQ     | NOTES |
|--|-----|------|------|-----|------|----------|--------|-------|
|  |     | X    | X    | X   | X    | X        | X      |       |
| NO OPERATION (NOP)                                     | L   | H    | H    | H   | X    | X        | X      |       |
| ACTIVE (Select bank and activate row)                  | L   | L    | H    | H   | X    | Bank/Row | X      | 1     |
| READ (Select bank and column, and start READ burst)    | L   | H    | L    | H   | L/H8 | Bank/Col | X      | 2     |
| WRITE (Select bank and column, and start WRITE burst)  | L   | H    | L    | L   | L/H8 | Bank/Col | Valid  | 2     |
| BURST TERMINATE  | L   | H    | H    | L   | X    | X        | Active |       |
| PRECHARGE (Deactivate row in bank or banks)            | L   | L    | H    | L   | X    | Code     | X      | 3     |
| AUTO refresh or Self Refresh (Enter self refresh mode) | L   | L    | L    | H   | X    | X        | X      | 4, 5  |
| LOAD MODE REGISTER                                     | L   | L    | L    | L   | X    | Op-code  | X      | 6     |
| Write Enable/Output Enable                             | –   | –    | –    | –   | L    | –        | Active | 7     |

**NOTE:**

1. A0–A11 provide device row address, and BA0, BA1 determine which device bank is made active.
2. A0–A9 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which device bank is being read from or written to.
3. A10 LOW: BA0, BA1 determine which device bank is being precharged. A10 HIGH: all device banks are precharged and BA0, BA1 are “Don’t Care.”
4. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
5. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
6. A0–A11 define the op-code written to the mode register.
7. Activates or deactivates the DQs during WRITES (zero-clock delay) and READs (two-clock delay).



**Absolute Maximum Ratings**

|                                   |   |
|-----------------------------------|---|
| SS.....-1V to +4.6V               | Operating Temperature                                     |
| Voltage on Inputs, NC or I/O Pins | T <sub>OPR</sub> (Commercial - ambient) .....0°C to +65°C |
| Relative to VSS .....-1V to +4.6V | Storage Temperature (plastic) .....-55°C to +150°C        |

**Table 10: DC Electrical Characteristics and Operating Conditions – 128MB**

| PARAMETER/CONDITION  | SYMBOL                          | MIN             | MAX                   | UNITS | NOTES |    |
|--|---------------------------------|-----------------|-----------------------|-------|-------|----|
|  | I <sub>H</sub>                  | 2               | V <sub>DD</sub> + 0.3 | V     | 22    |    |
| INPUT LOW VOLTAGE: Logic 0; All inputs   | V <sub>IL</sub>                 | -0.3            | 0.8                   | V     | 22    |    |
| INPUT LEAKAGE CURRENT:<br>Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub><br>(All other pins not under test = 0V) | Command and Address Inputs, CKE | -40             | 40                    | μA    | 33    |    |
|  | CK, S#                          | -20             | 20                    | μA    |       |    |
|  | DQMB                            | -5              | 5                     | μA    |       |    |
| OUTPUT LEAKAGE CURRENT: DQ pins are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>                             | DQ                              | I <sub>OZ</sub> | -5                    | 5     | μA    | 33 |
| OUTPUT LEVELS:<br>Output High Voltage (I <sub>OUT</sub> = -4mA)<br>Output Low Voltage (I <sub>OUT</sub> = 4mA)     | V <sub>OH</sub>                 | 2.4             | –                     | V     |       |    |
|  | V <sub>OL</sub>                 | –               | 0.4                   | V     |       |    |

Notes: 1, 5, 6; notes appear on page 18; V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±0.3V

| PARAMETER/CONDITION  | SYMBOL                             | MIN             | MAX                   | UNITS | NOTES |    |
|--|------------------------------------|-----------------|-----------------------|-------|-------|----|
| SUPPLY VOLTAGE   | V <sub>DD</sub> , V <sub>DDQ</sub> | 3               | 3.6                   | V     |       |    |
| INPUT HIGH VOLTAGE: Logic 1; All inputs  | V <sub>IH</sub>                    | 2               | V <sub>DD</sub> + 0.3 | V     | 22    |    |
| INPUT LOW VOLTAGE: Logic 0; All inputs   | V <sub>IL</sub>                    | -0.3            | 0.8                   | V     | 22    |    |
| INPUT LEAKAGE CURRENT:<br>Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub><br>(All other pins not under test = 0V) | Command and Address Inputs, CKE    | I <sub>I</sub>  | -80                   | 80    | μA    | 33 |
|  | CK, S#                             | -20             | 20                    | μA    |       |    |
|  | DQMB                               | -10             | 10                    | μA    |       |    |
| OUTPUT LEAKAGE CURRENT: DQ pins are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>                             | DQ                                 | I <sub>OZ</sub> | -10                   | 10    | μA    | 33 |
| OUTPUT LEVELS:<br>Output High Voltage (I <sub>OUT</sub> = -4mA)<br>Output Low Voltage (I <sub>OUT</sub> = 4mA)     | V <sub>OH</sub>                    | 2.4             | –                     | V     |       |    |
|  | V <sub>OL</sub>                    | –               | 0.4                   | V     |       |    |



## DD Specifications and Conditions – 128MB

| PARAMETER/CONDITION  | SYMBOL                    | MAX   |       |       | UNITS | NOTES         |                       |
|--|---------------------------|-------|-------|-------|-------|---------------|-----------------------|
|  |                           | -13E  | -133  | -10E  |       |               |                       |
| $t_{RC} = t_{RC} (MIN)$  | IDD1                      | 1,280 | 1,200 | 1,120 | mA    | 3, 18, 19, 30 |                       |
| STANDBY CURRENT: Power-Down Mode;<br>All device device banks idle; CKE = LOW   | IDD2                      | 16    | 16    | 16    | mA    | 30            |                       |
| STANDBY CURRENT: Active Mode;<br>CKE = HIGH; CS# = HIGH; All device banks active after $t_{RCD}$ met;<br>No accesses in progress | IDD3                      | 400   | 400   | 320   | mA    | 3, 12, 19, 30 |                       |
| OPERATING CURRENT: Burst Mode;<br>Continuous burst; READ or WRITE; All device banks active                                       | IDD4                      | 1,320 | 1,280 | 1,200 | mA    | 3, 18, 19, 30 |                       |
| AUTO REFRESH CURRENT<br>CKE = HIGH; CS# = HIGH   | $t_{RFC} = t_{RFC} (MIN)$ | IDD5  | 2,640 | 2,480 | 2,160 | mA            | 3, 12, 18, 19, 30, 31 |
|  | $t_{RFC} = 15.625\mu s$   | IDD6  | 24    | 24    | 24    | mA            |                       |
| SELF REFRESH CURRENT: CKE $\leq$ 0.2V  | IDD7                      | 16    | 16    | 16    | mA    | 4             |                       |

Notes: 1, 5, 6, 11, 13; notes appear on page 18; VDD, VDDQ = +3.3V  $\pm$ 0.3V; SDRAM components only

| PARAMETER/CONDITION  | SYMBOL                    | MAX               |       |       | UNITS | NOTES         |                       |
|--|---------------------------|-------------------|-------|-------|-------|---------------|-----------------------|
|  |                           | -13E              | -133  | -10E  |       |               |                       |
| OPERATING CURRENT: Active Mode;<br>Burst = 2; READ or WRITE; $t_{RC} = t_{RC} (MIN)$   | IDD1 <sup>a</sup>         | 1,296             | 1,216 | 1,136 | mA    | 3, 18, 19, 30 |                       |
| STANDBY CURRENT: Power-Down Mode;<br>All device banks idle; CKE = LOW  | IDD2 <sup>b</sup>         | 32                | 32    | 32    | mA    | 30            |                       |
| STANDBY CURRENT: Active Mode;<br>CKE = HIGH; CS# = HIGH; All device banks active after $t_{RCD}$ met;<br>No accesses in progress | IDD3 <sup>a</sup>         | 416               | 416   | 336   | mA    | 3, 12, 19, 30 |                       |
| OPERATING CURRENT: Burst Mode;<br>Continuous burst; READ or WRITE; All device banks active                                       | IDD4 <sup>a</sup>         | 1,336             | 1,216 | 1,136 | mA    | 3, 18, 19, 30 |                       |
| AUTO REFRESH CURRENT<br>CS# = HIGH; CKE = HIGH   | $t_{RFC} = t_{RFC} (MIN)$ | IDD5 <sup>b</sup> | 5,280 | 4,960 | 4,320 | mA            | 3, 12, 18, 19, 30, 31 |
|  | $t_{RFC} = 15.625\mu s$   | IDD6 <sup>b</sup> | 48    | 48    | 48    | mA            |                       |
| SELF REFRESH CURRENT: CKE $\leq$ 0.2V  | IDD7 <sup>b</sup>         | 32                | 32    | 32    | mA    | 4             |                       |

a - Value calculated as one module rank in this operating condition, and all other ranks in Power-Down Mode.

b - Value calculated reflects all module ranks in this operating condition.

| Input Capacitance: Command and Address | Cl1 | 20   | 30.4 | pF |
|--|-----|------|------|----|
| Input Capacitance: CK                  | Cl2 | 13.3 | 17.3 | pF |
| Input Capacitance: S#                  | Cl3 | 10   | 15.2 | pF |
| Input Capacitance: CKE                 | Cl4 | 20   | 30.4 | pF |
| Input Capacitance: DQMB                | Cl5 | 2.5  | 3.8  | pF |
| Input/Output Capacitance: DQ           | ClO | 4    | 6    | pF |

| Input Capacitance: Command and Address | Cl1 | 40   | 60.8 | pF |
|--|-----|------|------|----|
| Input Capacitance: CK                  | Cl2 | 13.3 | 17.3 | pF |
| Input Capacitance: S#                  | Cl3 | 10   | 15.2 | pF |
| Input Capacitance: CKE                 | Cl4 | 20   | 30.4 | pF |
| Input Capacitance: DQMB                | Cl5 | 5    | 7.6  | pF |
| Input/Output Capacitance: DQ           | ClO | 8    | 12   | pF |





Notes: 5–9, 11, 32; notes appear on page 18; module AC timing parameters comply with PC100 and PC133 design specs, based on component parameters

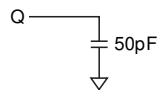
| Access time from CLK (pos. edge)       | CL = 3 | $t_{AC(3)}$ |             | 5.4     |               | 5.4     |             | 6       | ns | 27 |
|--|--------|-------------|-------------|---------|---------------|---------|-------------|---------|----|----|
|  | CL = 2 | $t_{AC(2)}$ |             | 5.4     |               | 6       |             | 6       | ns |    |
| Address hold time                      |        | $t_{AH}$    | 0.8         |         | 0.8           |         | 1           |         | ns |    |
| Address setup time                     |        | $t_{AS}$    | 1.5         |         | 1.5           |         | 2           |         | ns |    |
| CLK high-level width                   |        | $t_{CH}$    | 2.5         |         | 2.5           |         | 3           |         | ns |    |
| CLK low-level width                    |        | $t_{CL}$    | 2.5         |         | 2.5           |         | 3           |         | ns |    |
| Clock cycle time                       | CL = 3 | $t_{CK(3)}$ | 7           |         | 7.5           |         | 8           |         | ns | 23 |
|  | CL = 2 | $t_{CK(2)}$ | 7.5         |         | 10            |         | 10          |         | ns | 23 |
| CKE hold time                          |        | $t_{CKH}$   | 0.8         |         | 0.8           |         | 1           |         | ns |    |
| CKE setup time                         |        | $t_{CKS}$   | 1.5         |         | 1.5           |         | 2           |         | ns |    |
| CS#, RAS#, CAS#, WE#, DQM hold time    |        | $t_{CMH}$   | 0.8         |         | 0.8           |         | 1           |         | ns |    |
| CS#, RAS#, CAS#, WE#, DQM setup time   |        | $t_{CMS}$   | 1.5         |         | 1.5           |         | 2           |         | ns |    |
| Data-in hold time                      |        | $t_{DH}$    | 0.8         |         | 0.8           |         | 1           |         | ns |    |
| Data-in setup time                     |        | $t_{DS}$    | 1.5         |         | 1.5           |         | 2           |         | ns |    |
| Data-out high-impedance time           | CL = 3 | $t_{HZ(3)}$ |             | 5.4     |               | 5.4     |             | 6       | ns | 10 |
|  | CL = 2 | $t_{HZ(2)}$ |             | 5.4     |               | 6       |             | 6       | ns | 10 |
| Data-out low-impedance time            |        | $t_{LZ}$    | 1           |         | 1             |         | 1           |         | ns |    |
| Data-out hold time (load)              |        | $t_{OH}$    | 3           |         | 3             |         | 3           |         | ns |    |
| Data-out hold time (no load)           |        | $t_{OHN}$   | 1.8         |         | 1.8           |         | 1.8         |         | ns | 28 |
| ACTIVE to PRECHARGE command            |        | $t_{RAS}$   | 37          | 120,000 | 44            | 120,000 | 50          | 120,000 | ns | .  |
| ACTIVE to ACTIVE command period        |        | $t_{RC}$    | 60          |         | 66            |         | 70          |         | ns |    |
| ACTIVE to READ or WRITE delay          |        | $t_{RCD}$   | 15          |         | 20            |         | 20          |         | ns |    |
| Refresh period (8,192 rows)            |        | $t_{REF}$   |             | 64      |               | 64      |             | 64      | ms |    |
| AUTO REFRESH period                    |        | $t_{RFC}$   | 66          |         | 66            |         | 70          |         | ns |    |
| PRECHARGE command period               |        | $t_{RP}$    | 15          |         | 20            |         | 20          |         | ns |    |
| ACTIVE bank a to ACTIVE bank b command |        | $t_{RRD}$   | 14          |         | 15            |         | 20          |         | ns |    |
| Transition time                        |        | $t_T$       | 0.3         | 1.2     | 0.3           | 1.2     | 0.3         | 1.2     | ns | 7  |
| Write recovery time                    |        | $t_{WR}$    | 1 CLK + 7ns |         | 1 CLK + 7.5ns |         | 1 CLK + 7ns |         | ns | 24 |
|  |        |             | 14          |         | 15            |         | 15          |         | ns | 25 |
| Exit self refresh to ACTIVE command    |        | $t_{XSR}$   | 67          |         | 75            |         | 80          |         | ns | 20 |



(Notes: 5, 6, 7, 8, 9, 11, 32; notes appear following parameter tables)

|   |            |              |   |   |          |          |    |
|---|------------|--------------|---|---|----------|----------|----|
| READ/WRITE command to READ/WRITE command                | $t_{CCD}$  | 1            | 1 | 1 | $t_{CK}$ | 17       |    |
| CKE to clock disable or power-down entry mode           | $t_{CKED}$ | 1            | 1 | 1 | $t_{CK}$ | 14       |    |
| CKE to clock enable or power-down exit setup mode       | $t_{PED}$  | 1            | 1 | 1 | $t_{CK}$ | 14       |    |
| DQM to input data delay                                 | $t_{DQD}$  | 0            | 0 | 0 | $t_{CK}$ | 17       |    |
| DQM to data mask during WRITES                          | $t_{DQM}$  | 0            | 0 | 0 | $t_{CK}$ | 17       |    |
| DQM to data high-impedance during READs                 | $t_{DQZ}$  | 2            | 2 | 2 | $t_{CK}$ | 17       |    |
| WRITE command to input data delay                       | $t_{DWD}$  | 0            | 0 | 0 | $t_{CK}$ | 17       |    |
| Data-in to ACTIVE command                               | $t_{DAL}$  | 4            | 5 | 4 | $t_{CK}$ | 15, 21   |    |
| Data-in to precharge command                            | $t_{DPL}$  | 2            | 2 | 2 | $t_{CK}$ | 16, 21   |    |
| Last data-in to burst stop command                      | $t_{BDL}$  | 1            | 1 | 1 | $t_{CK}$ | 17       |    |
| Last data-in to new READ/WRITE command                  | $t_{CDL}$  | 1            | 1 | 1 | $t_{CK}$ | 17       |    |
| Last data-in to precharge command                       | $t_{RDL}$  | 2            | 2 | 2 | $t_{CK}$ | 16, 21   |    |
| LOAD MODE REGISTER command to ACTIVE or REFRESH command | $t_{MRD}$  | 2            | 2 | 2 | $t_{CK}$ | 26       |    |
| Data-out to high-impedance from precharge command       | CL = 3     | $t_{ROH(3)}$ | 3 | 3 | 3        | $t_{CK}$ | 17 |
|   | CL = 2     | $t_{ROH(2)}$ | 2 | 2 | 2        | $t_{CK}$ | 17 |

1. All voltages referenced to Vss.
2. This parameter is sampled. VDD, VDDQ = +3.3V; f = 1 MHz, TA = 25°C; pin under test biased at 1.4V.
3. Idd is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured (0°C ≤ TA ≤ +70°C).
6. An initial pause of 100μs is required after power-up, followed by two AUTO Refresh commands, before proper device operation is ensured. (VDD and VDDQ must be powered up simultaneously. Vss and VssQ must be at same potential.) The two AUTO Refresh command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
7. AC characteristics assume tT = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The last valid data element will meet tOH before going High-Z.
11. AC timing and Idd tests have VIL = 0V and VIH = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1 ns, then the timing is referenced at VIL (MAX) and VIH (MIN) and no longer at the 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
13. IDD specifications are tested after the device is properly initialized.
14. Timing actually specified by tCKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by tWR plus tRP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by tWR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on tCK = 10ns for -10E, and tCK = 7.5ns for -133 and -13E.
22. VIH overshoot: VIH (MAX) = VDDQ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. VIL undershoot: VIL (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (tRP) begins 7ns for -13E; 7.5ns for -133 and 7ns for -10E after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. tAC for -133/-13E at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. For -10E, CL = 2 and tCK = 10ns; for -133, CL = 3 and tCK = 7.5ns; for -13E, CL = 2 and tCK = 7.5ns.
30. CKE is HIGH during refresh command period tRFC (MIN) else CKE is LOW. The Idd6 limit is actually a nominal value and does not result in a fail value.
31. The value of tRAS used in -13E speed grade module SPDs is calculated from tRC - tRP = 45ns.
32. Refer to device data sheet for timing waveforms.
33. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.

## SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 7, Data Validity, and Figure 8, Definition of Start and Stop).

### SPD Start Condition

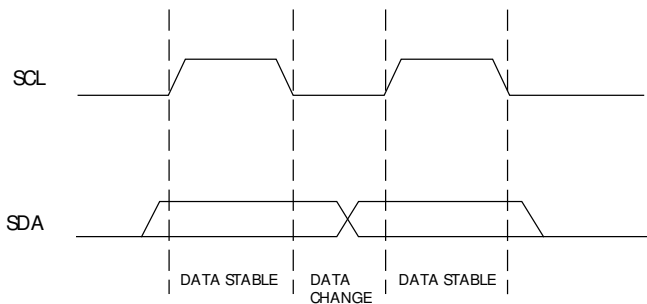
All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

### SPD Stop Condition

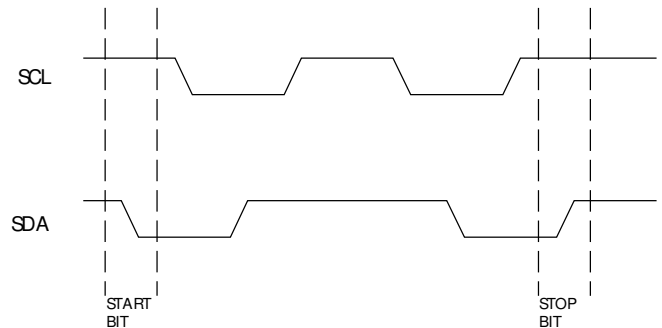
All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

## SPD Acknowledge

**Figure 7: Data Validity**



**Figure 8: Definition of Start and Stop**



**Figure 9: Acknowledge Response From Receiver**

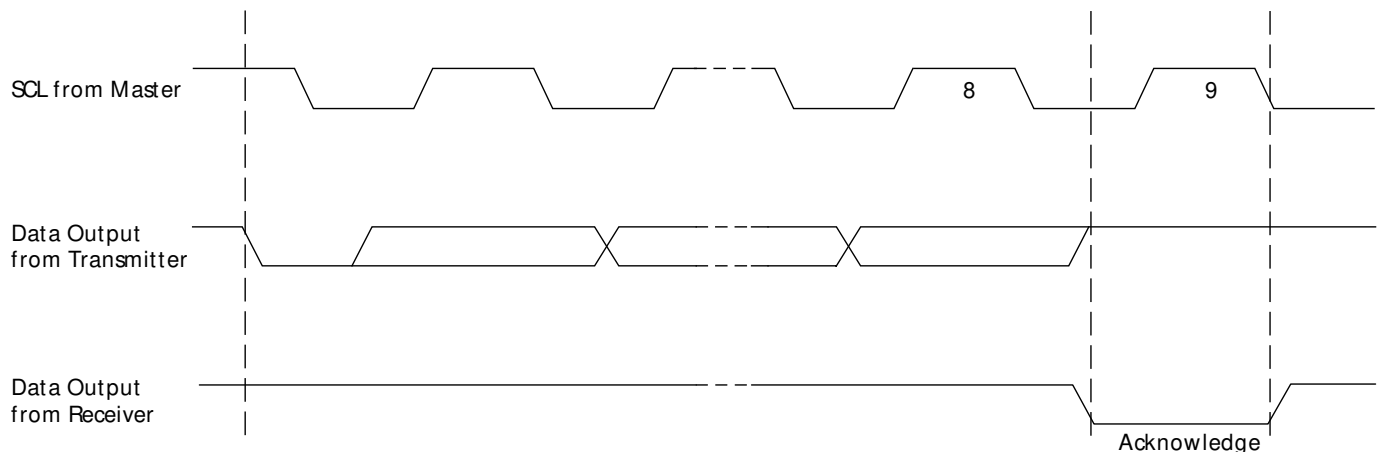


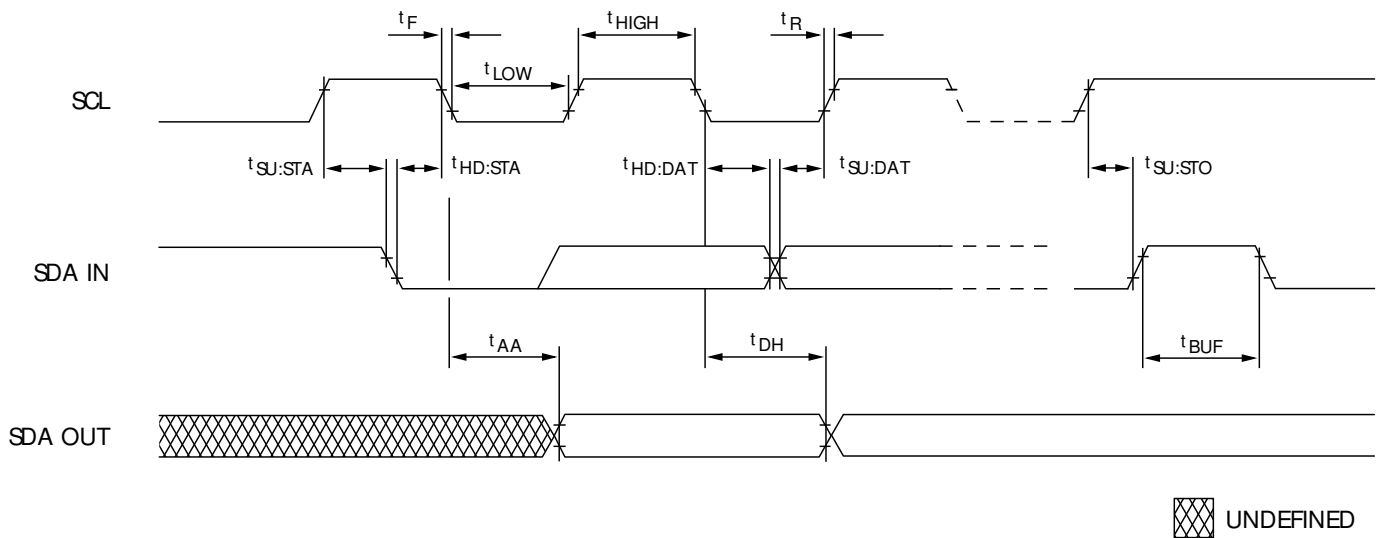
Table 18: EEPROM Device Select Code

| SELECT CODE | DEVICE TYPE IDENTIFIER |    |    |    | CHIP ENABLE |    |    | R $\bar{W}$ |
|-------------|------------------------|----|----|----|-------------|----|----|-------------|
|             | b7                     | b6 | b5 | b4 | b3          | b2 | b1 | b0          |
|             |                        |    |    |    |             |    |    | —           |
|             |                        |    |    |    |             |    |    | —           |

Table 19: EEPROM Operating Modes

| MODE | R $\bar{W}$ BIT | WC | BYTES | INITIAL SEQUENCE |
|------|-----------------|----|-------|------------------|
|      |                 |    |       | —                |
|      |                 |    |       | —                |
|      |                 |    | ≥     | —                |
|      |                 |    | ≤     | —                |

Figure 10: SPD EEPROM Timing Diagram





All voltages referenced to VSS; VDDSPD = +2.3V to +3.6V

| SUPPLY VOLTAGE   | VDDSPD | 2.3                 | 3.6                 | V       |
|--|--------|---------------------|---------------------|---------|
| INPUT HIGH VOLTAGE: Logic 1; All inputs                                | Vih    | $VDDSPD \times 0.7$ | $VDDSPD + 0.5$      | V       |
| INPUT LOW VOLTAGE: Logic 0; All inputs                                 | VIL    | -1                  | $VDDSPD \times 0.3$ | V       |
| OUTPUT LOW VOLTAGE: IOUT = 3mA   | VOL    | -                   | 0.4                 | V       |
| INPUT LEAKAGE CURRENT: VIN = GND to VDD                                | II     | -                   | 10                  | $\mu A$ |
| OUTPUT LEAKAGE CURRENT: VOUT = GND to VDD                              | ILO    | -                   | 10                  | $\mu A$ |
| STANDBY CURRENT: SCL = SDA = VDD - 0.3V; All other inputs = VDD or VSS | ISB    | -                   | 30                  | $\mu A$ |
| POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz                    | ICC    | -                   | 2                   | mA      |

All voltages referenced to VSS; VDDSPD = +2.3V to +3.6V

| SCL LOW to SDA data-out valid                               | $t_{AA}$     | 0.2 | 0.9 | $\mu s$ | 1 |
|---|--------------|-----|-----|---------|---|
| Time the bus must be free before a new transition can start | $t_{BUF}$    | 1.3 |     | $\mu s$ |   |
| Data-out hold time  | $t_{DH}$     | 200 |     | ns      |   |
| SDA and SCL fall time                                       | $t_F$        |     | 300 | ns      | 2 |
| Data-in hold time   | $t_{HD:DAT}$ | 0   |     | $\mu s$ |   |
| Start condition hold time                                   | $t_{HD:STA}$ | 0.6 |     | $\mu s$ |   |
| Clock HIGH period   | $t_{HIGH}$   | 0.6 |     | $\mu s$ |   |
| Noise suppression time constant at SCL, SDA inputs          | $t_I$        |     | 50  | ns      |   |
| Clock LOW period  | $t_{LOW}$    | 1.3 |     | $\mu s$ |   |
| SDA and SCL rise time                                       | $t_R$        |     | 0.3 | $\mu s$ | 2 |
| SCL clock frequency   | $f_{SCL}$    |     | 400 | KHz     |   |
| Data-in setup time  | $t_{SU:DAT}$ | 100 |     | ns      |   |
| Start condition setup time                                  | $t_{SU:STA}$ | 0.6 |     | $\mu s$ | 3 |
| Stop condition setup time                                   | $t_{SU:STO}$ | 0.6 |     | $\mu s$ |   |
| WRITE cycle time  | $t_{WRC}$    |     | 10  | ms      | 4 |

NOTE:

1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time ( $t_{WRC}$ ) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.



“1” / “0” : Serial Data, “driven to HIGH” / “driven to LOW”

|    |  |                                     |                |                |
|----|--|-------------------------------------|----------------|----------------|
| 0  | Number of Bytes Used by Micron                             | 128                                 | 80             | 80             |
| 1  | Total Number of SPD Memory Bytes                           | 256                                 | 08             | 08             |
| 2  | Memory Type  | SDRAM                               | 04             | 04             |
| 3  | Number of Row Addresses                                    | 12                                  | 0C             | 0C             |
| 4  | Number of Column Addresses                                 | 10                                  | 0A             | 0A             |
| 5  | Number of Module Ranks                                     | 1 or 2                              | 01             | 02             |
| 6  | Module Data Width  | 64                                  | 40             | 40             |
| 7  | Module Data Width (Continued)                              | 0                                   | 00             | 00             |
| 8  | Module Voltage Interface Levels                            | LVTTL                               | 01             | 01             |
| 9  | SDRAM Cycle Time, <sup>t</sup> CK, (CASLatency = 3)        | 7 (-13E)<br>7.5 (-133)<br>8 (-10E)  | 70<br>75<br>80 | 70<br>75<br>80 |
| 10 | SDRAM Access From Clock, <sup>t</sup> AC, (CASLatency = 3) | 5.4 (-13E/-133)<br>6 (-10E)         | 54<br>60       | 54<br>60       |
| 11 | Module Configuration Type                                  | NONPARITY                           | 00             | 00             |
| 12 | Refresh Rate/type  | 15.625μs/SELF                       | 80             | 80             |
| 13 | SDRAM Width (Primary SDRAM)                                | 8                                   | 08             | 08             |
| 14 | Error-Checking SDRAM Data Width                            | NONE                                | 00             | 00             |
| 15 | Minimum Clock Delay, <sup>t</sup> CCD                      | 1                                   | 01             | 01             |
| 16 | Burst Lengths Supported                                    | 1, 2, 4, 8, PAGE                    | 8F             | 8F             |
| 17 | Number of Banks on SDRAM Device                            | 4                                   | 04             | 04             |
| 18 | CAS Latencies Supported                                    | 2, 3                                | 06             | 06             |
| 19 | CS Latency   | 0                                   | 01             | 01             |
| 20 | WE Latency   | 0                                   | 01             | 01             |
| 21 | SDRAM Module Attributes                                    | UNBUFFERED                          | 00             | 00             |
| 22 | SDRAM Device Attributes: General                           | 0E                                  | 0E             | 0E             |
| 23 | SDRAM Cycle Time, <sup>t</sup> CK, (CASLatency = 2)        | 7.5 (13E)<br>10 (-133/-10E)         | 75<br>A0       | 75<br>A0       |
| 24 | SDRAM Access From Clock, <sup>t</sup> AC, (CASLatency = 2) | 54 (-13E)<br>6 (-133/-10E)          | 54<br>60       | 54<br>60       |
| 25 | SDRAM Cycle Time, <sup>t</sup> CK, (CASLatency = 1)        |                                     | 00             | 00             |
| 26 | SDRAM Access From Clock, <sup>t</sup> AC, (CASLatency = 1) |                                     | 00             | 00             |
| 27 | Minimum Row Precharge Time, <sup>t</sup> RP                | 15 (-13E)<br>20 (-133/-10E)         | 0F<br>14       | 0F<br>14       |
| 28 | Minimum Row Active to Row Active, <sup>t</sup> RRD         | 14 (-13E)<br>15 (-133)<br>20 (-10E) | 0E<br>0F<br>14 | 0E<br>0F<br>14 |
| 29 | Minimum RAS# to CAS# Delay, <sup>t</sup> RCD               | 15 (-13E)<br>20 (-133/-10E)         | 0F<br>14       | 0F<br>14       |
| 30 | Minimum RAS# Pulse Width, <sup>t</sup> RAS (See note 1)    | 45 (-13E)<br>44 (-133)<br>50 (-10E) | 2D<br>2C<br>32 | 2D<br>2C<br>32 |
| 31 | Module Rank Density  | 128MB                               | 20             | 20             |
| 32 | Command Address Setup, <sup>t</sup> AS                     | 1.5 (-13E/-133)<br>2 (-10E)         | 15<br>20       | 15<br>20       |



“1” / “0” : Serial Data, “driven to HIGH” / “driven to LOW”

|        |  |   |                |                |
|--------|--|---|----------------|----------------|
| 33     | Command Address Hold, <sup>t</sup> AH                    | 0.8 (-13E/-133)<br>1 (-10E)               | 08<br>10       | 08<br>10       |
| 34     | Data Signal Input Setup, <sup>t</sup> DS                 | 1.5 (-13E/-133)<br>2 (-10E)               | 15<br>20       | 15<br>20       |
| 35     | Data Signal Input Hold, <sup>t</sup> DH                  | 0.8 (-13E/-133)<br>1 (-10E)               | 08<br>10       | 08<br>10       |
| 36–40  | Reserved Bytes   |   | 00             | 00             |
| 41     | Device Minimum Active/Auto-Refresh Time, <sup>t</sup> RC | 60ns (-13E)<br>66ns (-133)<br>70ns (-10E) | 3C<br>42<br>46 | 3C<br>42<br>46 |
| 42–61  | Reserved Bytes   |   | 00             | 00             |
| 62     | SPD Revision   | REV.2.0                                   | 02             | 12             |
| 63     | Checksum For Bytes 0-62                                  | (-13E)<br>(-133)<br>(-10E)                | 94<br>E0<br>2C | 95<br>E1<br>2D |
| 64     | Manufacturer's JEDEC ID Code                             | MICRON                                    | 2C             | 2C             |
| 65-71  | Manufacturer's JEDEC Code (Cont.)                        |   | FF             | FF             |
| 72     | Manufacturing Location                                   | 00–12                                     | 00–0C          | 00–0C          |
| 73–90  | Module Part Number (ASCII)                               |   | Variable Data  | Variable Data  |
| 91     | PCB Identification Code                                  |   | Variable Data  | Variable Data  |
| 92     | Identification Code (Continued)                          | 0   | 00             | 00             |
| 93     | Year of Manufacture in BCD                               |   | Variable Data  | Variable Data  |
| 94     | Week of Manufacture in BCD                               |   | Variable Data  | Variable Data  |
| 95–98  | Module Serial Number                                     |   | Variable Data  | Variable Data  |
| 99–125 | Manufacturer-Specific Data (RSVD)                        |   |                |                |
| 126    | System Frequency   | 100 MHz<br>(-13E/-133, -10E)              | 64             | 64             |
| 127    | Year of Manufacture in BCD                               |   | AF             | FF             |

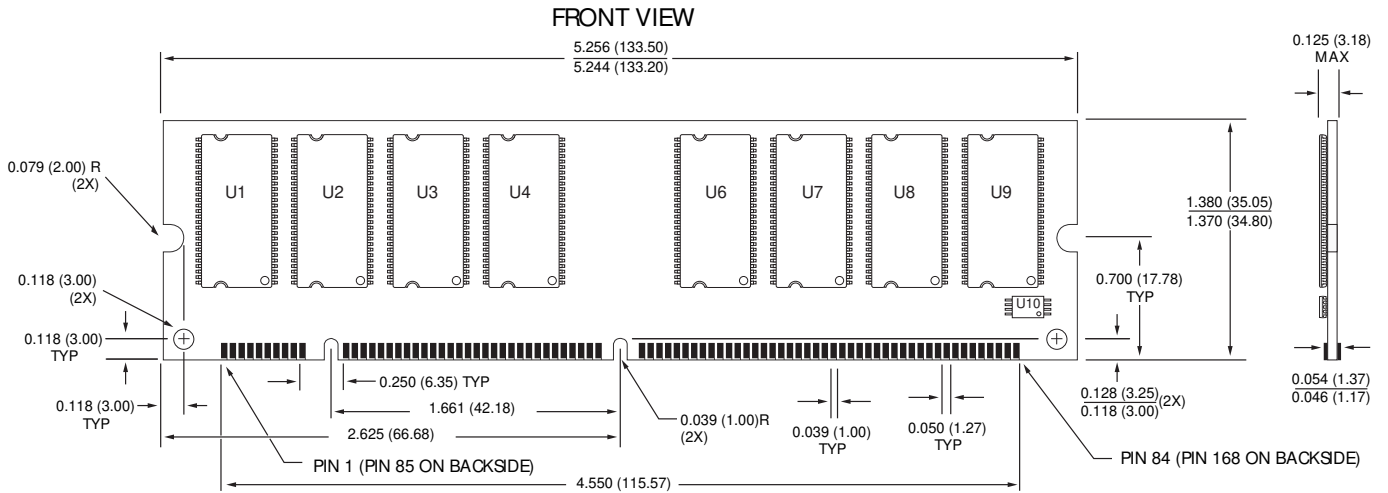
NOTE:

1. The value of <sup>t</sup>RAS used for the -13E module is calculated from <sup>t</sup>RC - <sup>t</sup>RP. Actual device spec. value is 37ns.

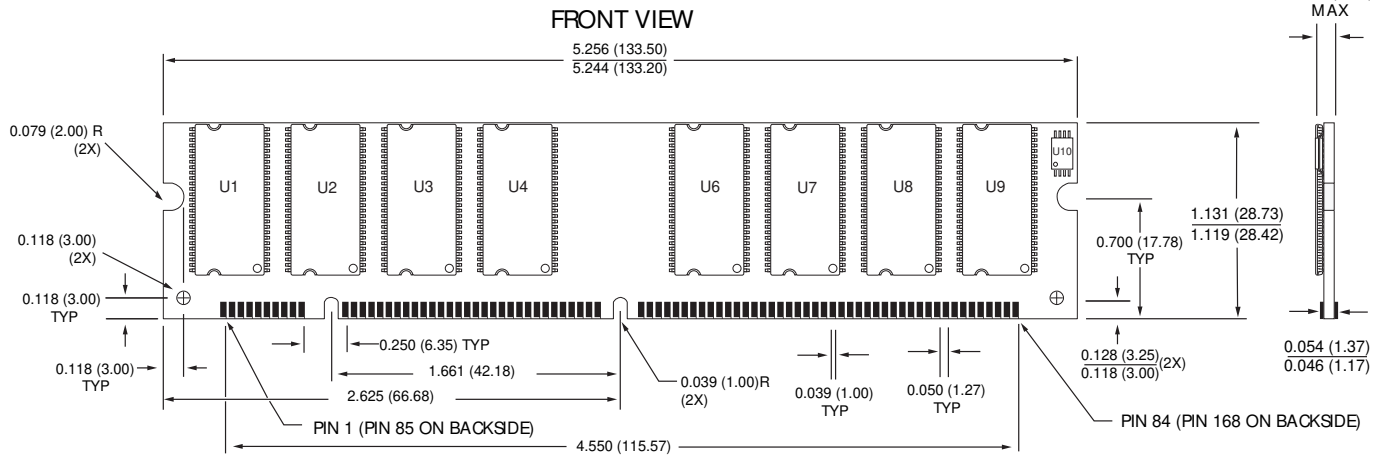


**Figure 11: 168-Pin DIMM Dimensions – 128M B**

**STANDARD PCB**



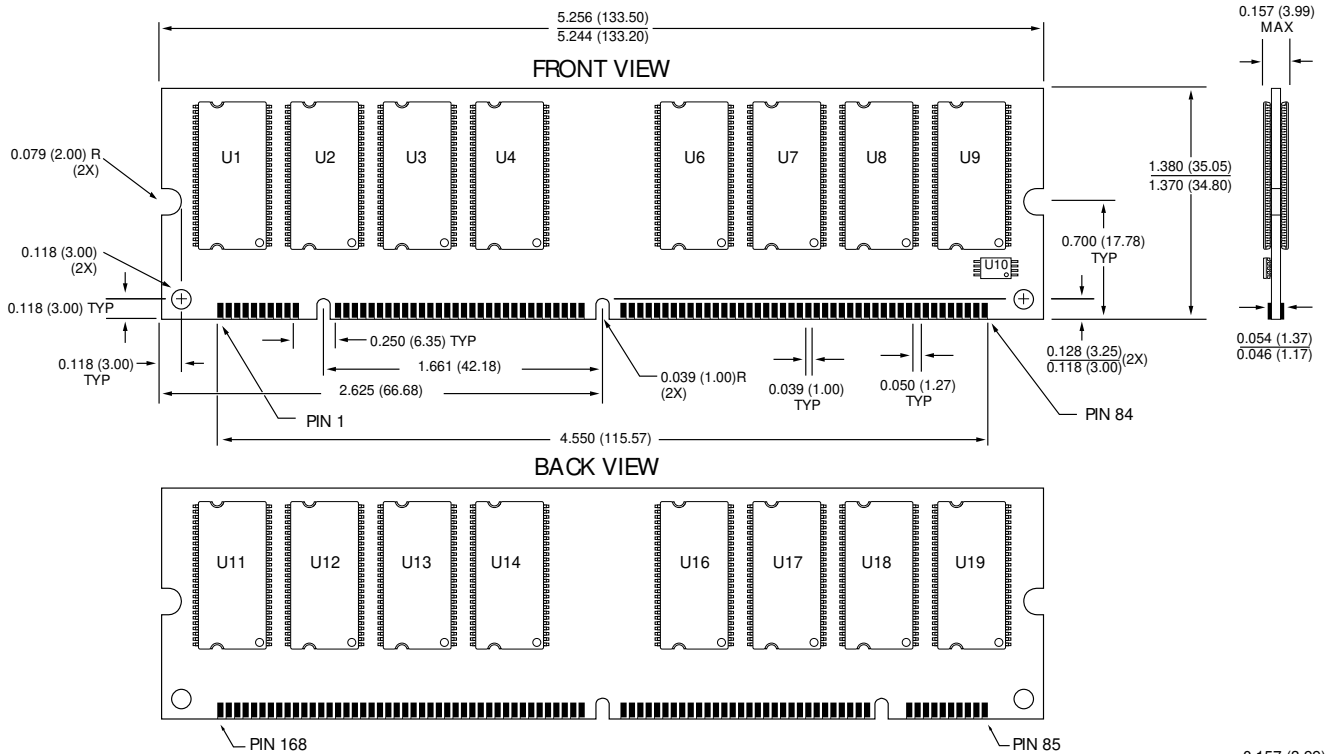
**LOW PROFILE PCB**



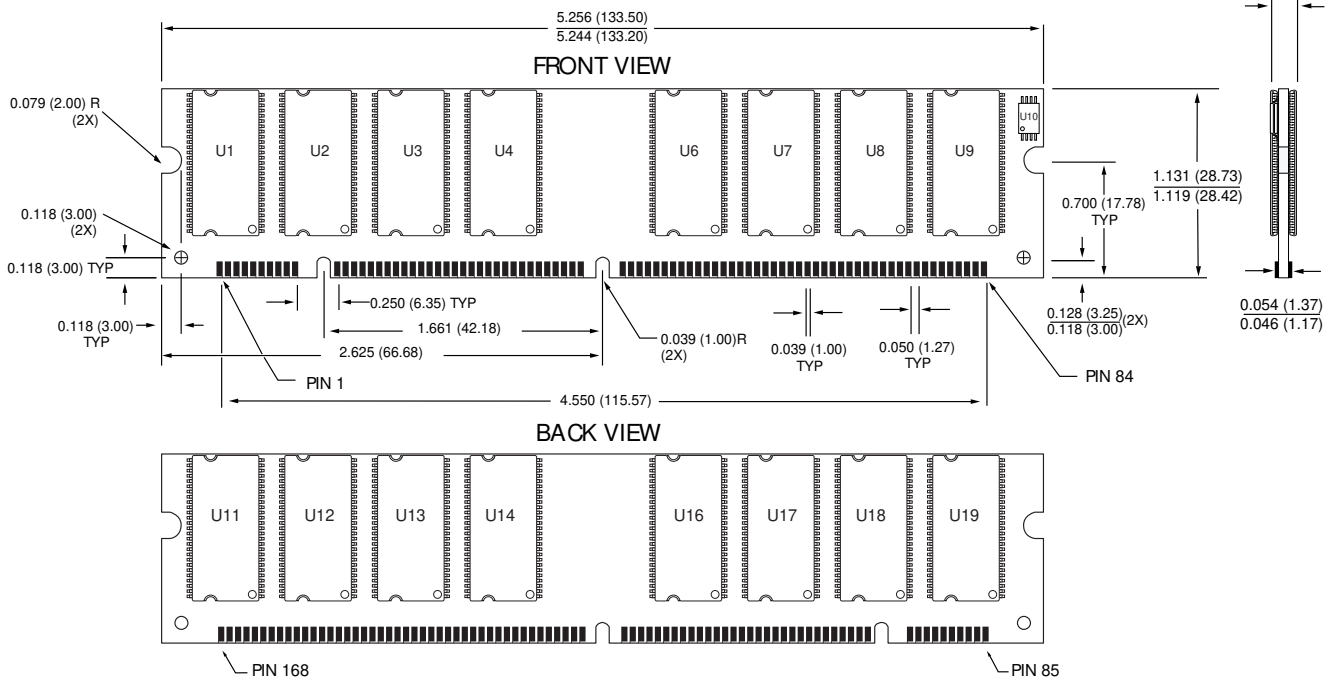
NOTE:

All dimensions in inches (millimeters);  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.

### STANDARD PCB



### LOW PROFILE PCB



**NOTE:**

All dimensions in inches (millimeters);  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.