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DDR SDRAM REGISTERED DIMM

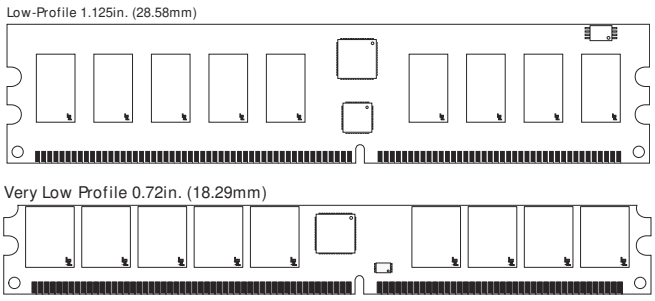
MT18VDDF6472 – 512MB
MT18VDDF12872 – 1GB

For the latest data sheet, please refer to the Micron® Web site: www.micron.com/products/modules

Features

- 184-pin, dual in-line memory module (DIMM)
- Fast data transfer rates: PC3200
- Utilizes 400 MT/s DDR SDRAM components
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Supports ECC error detection and correction
- 512MB (64 Meg x 72) and 1GB (128 Meg x 72)
- $V_{DD} = V_{DD}Q = +2.6V$
- $V_{DDSPD} = +2.3V$ to $+3.6V$
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs CK and CK#
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh modes
- 7.8125µs maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency
- Gold edge contacts

Figure 1: 184-Pin DIMM (MO-206)



OPTIONS	MARKING
• Operating Temperature Range	
Commercial ($0°C \le T_A \le +70°C$)	none
• Package	
184-pin DIMM (standard)	G
184-pin DIMM (lead-free)[1]	Y
• Memory Clock, Speed, CAS Latency[2]	
5ns (200 MHz), 400 MT/s, CL = 3	-40B
• PCB	
1.125in (28.58mm)	

NOTE: 1. Contact Micron for availability of products.
2. CL = CAS latency; registered Mode adds one clock cycle to CL.

Table 1: Address Table

	512MB	1GB
Refresh Count	8K	8K
Row Addressing	8K (A0–A12)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	256Mb (64 Meg x 4)	512Mb (128 Meg x 4)
Column Addressing	2K (A0–A9, A11)	4K (A0–A9, A11, A12)
Module Rank Addressing	1 (S0#)	1 (S0#)

Table 2: Part Numbers and Timing Parameters

PART NUMBER	MODULE DENSITY	CONFIGURATION	MODULE BANDWIDTH	MEMORY CLOCK/ DATA RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT18VDDF6472G-40B__	512MB	64 Meg x 72	3.2 GB/s	5ns/400 MT/s	3-3-3
MT18VDDF6472Y-40B__	512MB	64 Meg x 72	3.2 GB/s	5ns/400 MT/s	3-3-3
MT18VDDF12872G-40B__	1GB	128 Meg x 72	3.2 GB/s	5ns/400 MT/s	3-3-3
MT18VDDF12872Y-40B__	1GB	128 Meg x 72	3.2 GB/s	5ns/400 MT/s	3-3-3

NOTE:

All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18VDDF6472G-40BB1.

Table 3: Pin Assignment (184-Pin DIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	24	DQ17	47	DQS8	70	VDD
2	DQ0	25	DQS2	48	A0	71	NC
3	VSS	26	VSS	49	CB2	72	DQ48
4	DQ1	27	A9	50	VSS	73	DQ49
5	DQS0	28	DQ18	51	CB3	74	VSS
6	DQ2	29	A7	52	BA1	75	NC
7	VDD	30	VDDQ	53	DQ32	76	NC
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ
9	NC	32	A5	55	DQ33	78	DQS6
10	RESET#	33	DQ24	56	DQS4	79	DQ50
11	VSS	34	VSS	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	VSS	81	VSS
13	DQ9	36	DQS3	59	BA0	82	NC
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDDQ	38	VDD	61	DQ40	84	DQ57
16	NC	39	DQ26	62	VDDQ	85	VDD
17	NC	40	DQ27	63	WE#	86	DQS7
18	VSS	41	A2	64	DQ41	87	DQ58
19	DQ10	42	VSS	65	CAS#	88	DQ59
20	DQ11	43	A1	66	VSS	89	VSS
21	CKE0	44	CB0	67	DQS5	90	NC
22	VDDQ	45	CB1	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

Table 4: Pin Assignment (184-Pin DIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
93	VSS	116	VSS	139	VSS	162	DQ47
94	DQ4	117	DQ21	140	DQS17	163	NC
95	DQ5	118	A11	141	A10	164	VDDQ
96	VDDQ	119	DQS11	142	CB6	165	DQ52
97	DQS9	120	VDD	143	VDDQ	166	DQ53
98	DQ6	121	DQ22	144	CB7	167	NC
99	DQ7	122	A8	145	VSS	168	VDD
100	VSS	123	DQ23	146	DQ36	169	DQS15
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	NC	126	DQ28	149	DQS13	172	VDDQ
104	VDDQ	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDDQ	151	DQ39	174	DQ60
106	DQ13	129	DQS12	152	VSS	175	DQ61
107	DQS10	130	A3	153	DQ44	176	VSS
108	VDD	131	DQ30	154	RAS#	177	DQS16
109	DQ14	132	VSS	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDDQ	179	DQ63
111	NC	134	CB4	157	S0#	180	VDDQ
112	VDDQ	135	CB5	158	NC	181	SA0
113	NC	136	VDDQ	159	DQS14	182	SA1
114	DQ20	137	CK0	160	VSS	183	SA2
115	A12	138	CK0#	161	DQ46	184	VDDSPD

Figure 2: Pin Locations

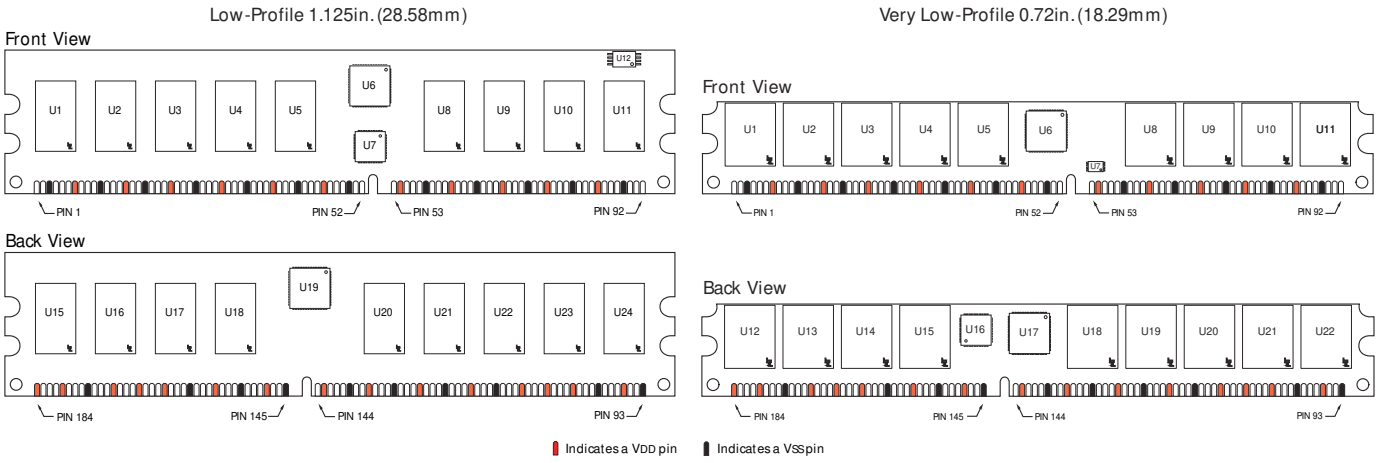


Table 5: Pin Descriptions

Pin numbers may not correlate with symbol; refer to Pin Assignment Tables for pin number and symbol information.

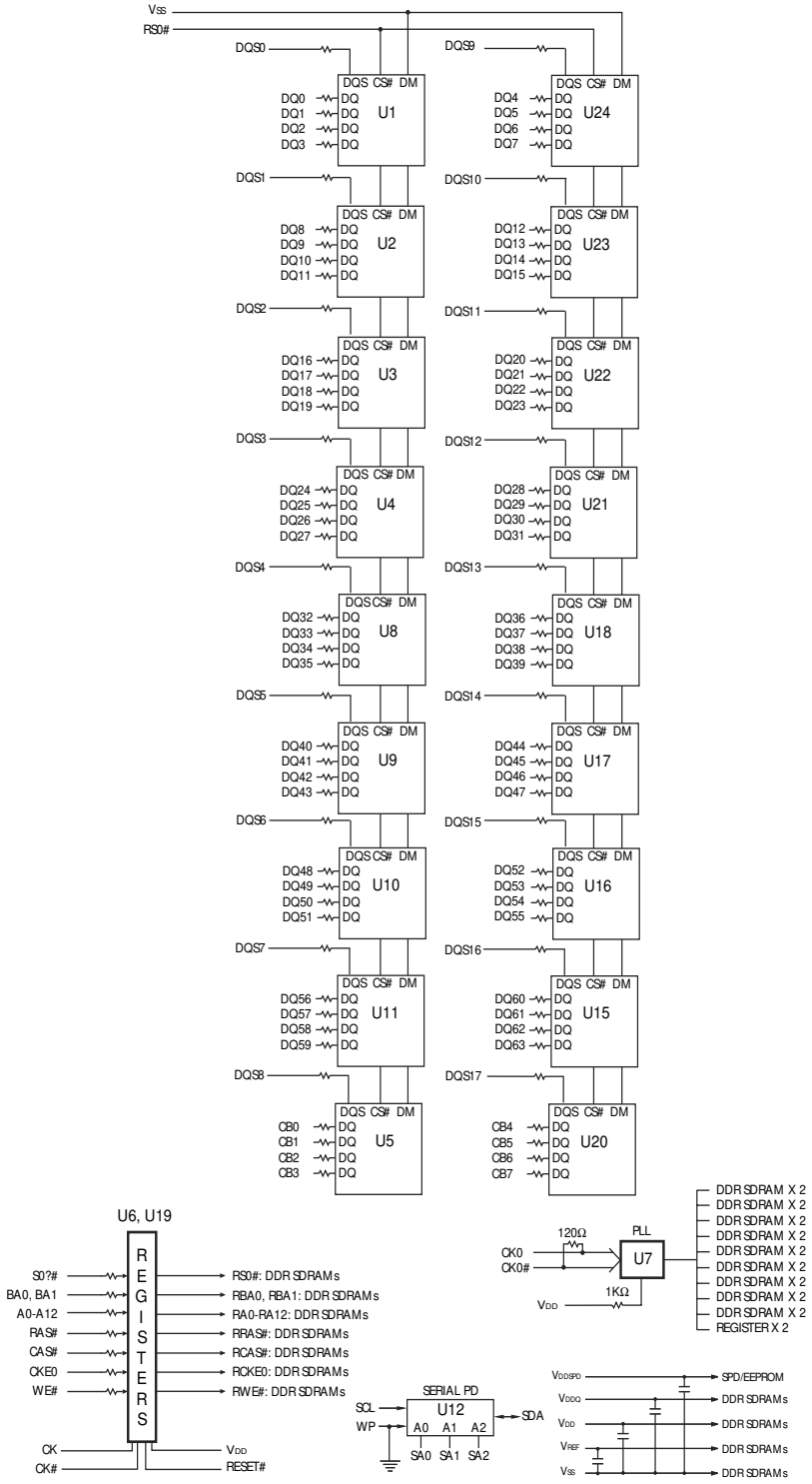
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
10	RESET#	Input	Asynchronously forces all registered ouputs LOW when RESET# is LOW. This signal can be used during power-up to ensure CKE is LOW and DQs are High-Z.
63, 65, 154	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
137, 138	CK0, CK0#	Input	Clock: CK, CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK,and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
21	CKE0	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH. After CKE is brought HIGH, it becomes an SSTL_2 input only.
157	S0#	Input	Chip Selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
52, 59	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 115, 118, 122, 125, 130, 141	A0–A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
5, 14, 25, 36, 47, 56, 67, 78, 86, 97, 107, 119, 129, 140, 149, 159, 169, 177	DQS0–DQS17	Input/ Output	Data Strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
44, 45, 49, 51, 134, 135, 142, 144	CB0–CB7	Input/ Output	Check Bits.

Table 5: Pin Descriptions

Pin numbers may not correlate with symbol; refer to Pin Assignment Tables for pin number and symbol information.

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2, 4, 6, 8, 12,13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0–DQ63	Input/ Output	Data I/Os: Data bus.
92	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
181, 182, 183	SA0–SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
91	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
1	V_{REF}	Supply	SSTL_2 reference voltage.
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V_{DDQ}	Supply	DQ Power Supply: +2.6V ±0.1V.
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	Supply	Power Supply: +2.6V ±0.1V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	Supply	Ground.
184	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
9, 16, 17, 71, 75, 76, 82, 90, 101, 102, 103, 111, 113,158, 163, 167, 173	NC	—	No Connect: These pins should be left unconnected.

Figure 3: Functional Block Diagram – Low-Profile PCB



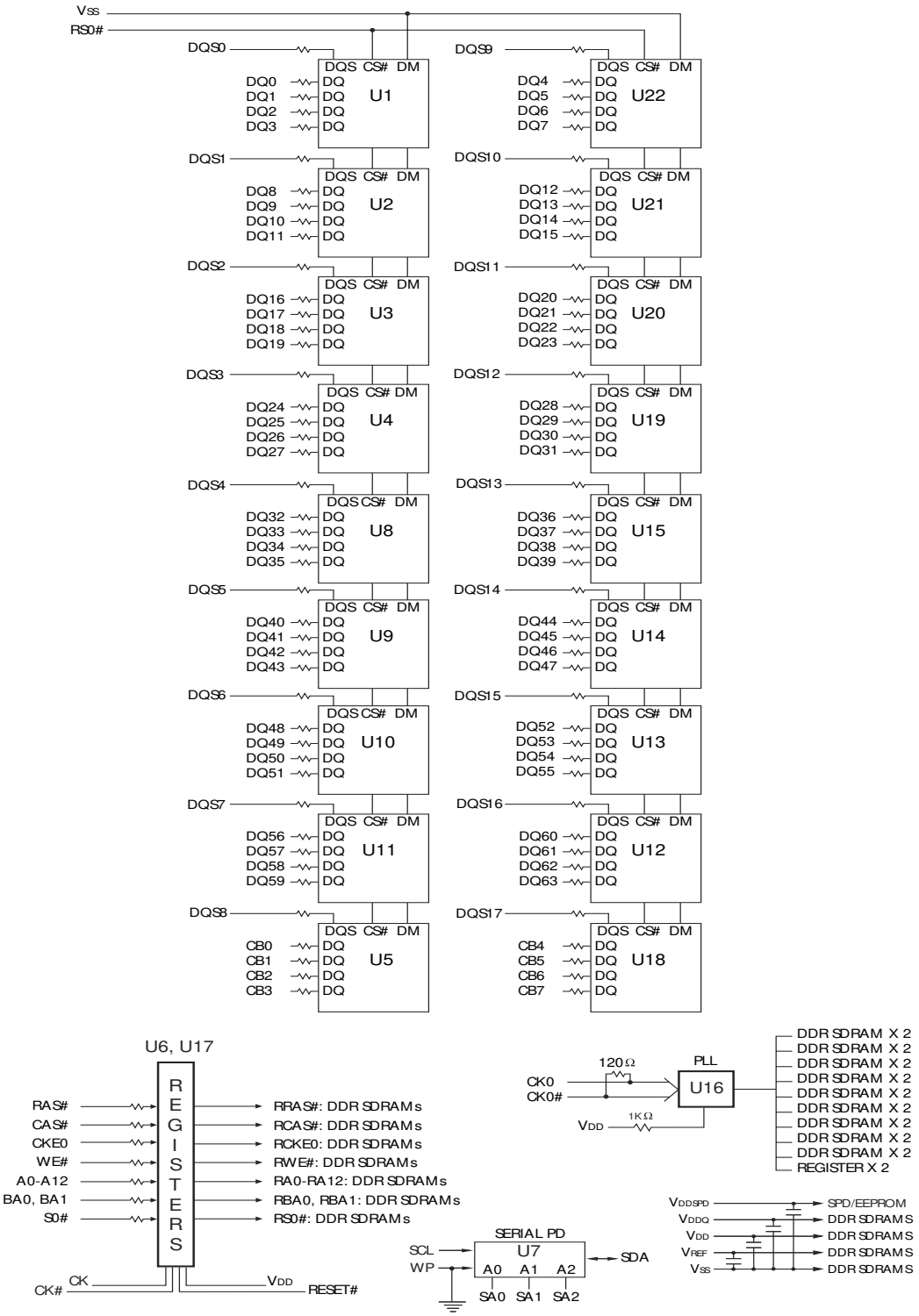
NOTE:

1. All resistor values are 22Ω unless otherwise specified.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

Standard modules use the following DDR SDRAM devices:
MT46V64M4FG (512MB); MT46V128M4FG (1GB)

Lead-free modules use the following DDR SDRAM devices:
MT46V64M4BG (512MB); MT46V128M4BG (1GB)

Figure 4: Functional Block Diagram – Very Low-Profile PCB



NOTE:

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MT46V64M4FG (512MB); MT46V128M4FG (1GB)

Lead-free modules use the following DDR SDRAM devices:
MT46V64M4BG (512MB); MT46V128M4BG (1GB)

General Description

The MT18VDDF6472 and MT18VDDF12872 are high-speed CMOS, dynamic random-access, 512MB and 1GB memory modules organized in x72 (ECC) configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select device bank; A0–A12 select device row). The address bits registered coincident with the READ or WRITE command are used to select the device bank and starting device column location for the burst access.

DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing effective high bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 256Mb or 512Mb DDR SDRAM component data sheets.

PLL and Register Operation

DDR SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL), on the module, receives and redrives the differential clock signals (CK, CK#) to the DDR SDRAM devices. The registers and PLL minimize system and clock loading.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Mode Register Definition

The mode register is used to define the specific mode of operation of DDR SDRAM devices. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in the Mode Register Diagram. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified

time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A12 specify the operating mode.

Burst Length

Read and write accesses to DDR SDRAM devices are burst oriented, with the burst length being programmable, as shown in Figure 5, Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, because unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A*i* when the burst length is set to two, by A2–A*i* when the burst length is set to four and by A3–A*i* when the burst length is set to eight (where A*i* is the most significant column address bit for a given configuration. See Note 5 of Table 6, Burst Definition Table, on page 10, for A*i* values). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 6, Burst Definition Table, on page 10.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 3, 2.5, or 2 clocks, as shown in Figure 6, CAS Latency Diagram, on page 10.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. The CAS Latency Table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used, because unknown operation or incompatibility with future versions may result.

Figure 5: Mode Register Definition Diagram

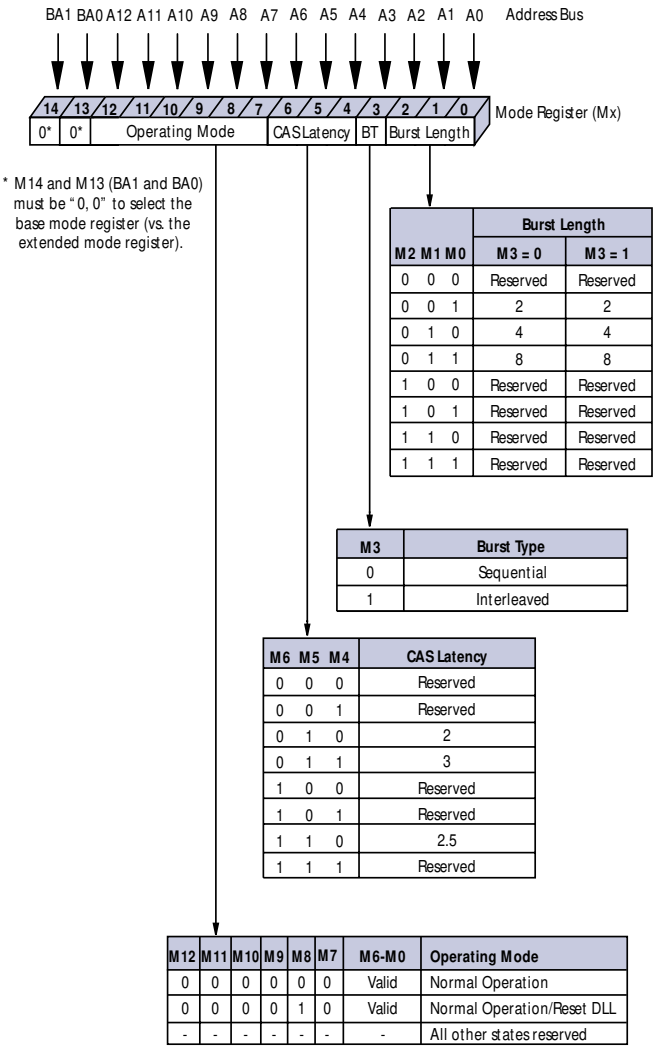


Table 6: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

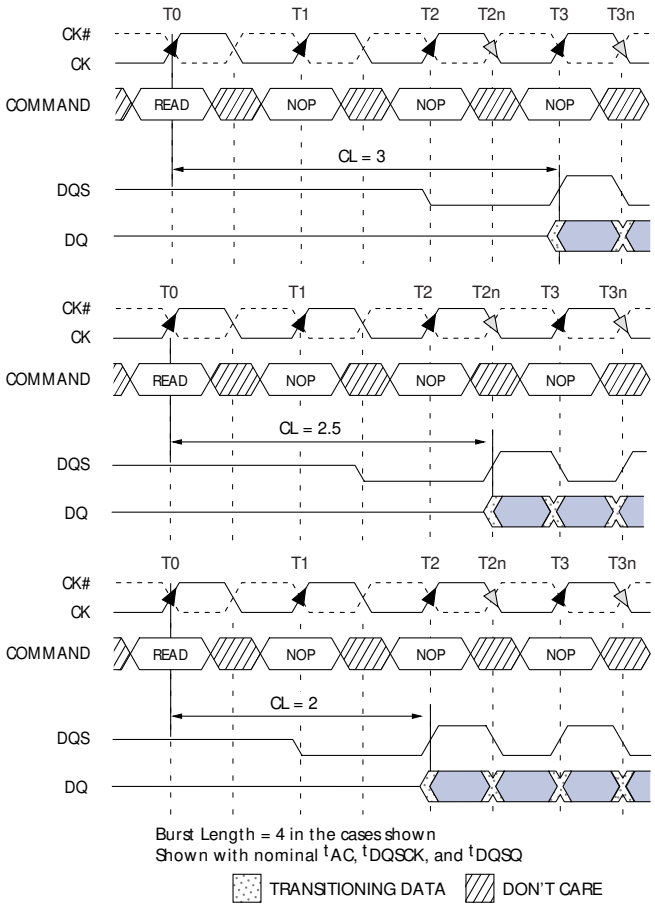
NOTE:

1. For a burst length of two, A1–A*i* select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2–A*i* select the four-data-element block; A0–A1 select the first access within the block.
3. For a burst length of eight, A3–A*i* select the eight-data-element block; A0–A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
5. *i* = 9, 11 (512MB)
   i = 9, 11, 12 (1GB)

Table 7: CAS Latency (CL) Table

	ALLOWABLE OPERATING CLOCK FREQUENCY (MHZ)		
SPEED	CL = 2	CL = 2.5	CL = 3
-40B	75 ≤ f ≤ 133	75 ≤ f ≤ 133	133 ≤ f ≤ 200

Figure 6: CAS Latency Diagram



Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 3, 2.5, or 2 clocks, as shown in Figure 6, CAS Latency Diagram.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. The CAS Latency Table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used, because unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7–A12 each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9–A12 each set

to zero, bit A8 set to one, and bits A0–A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7–A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

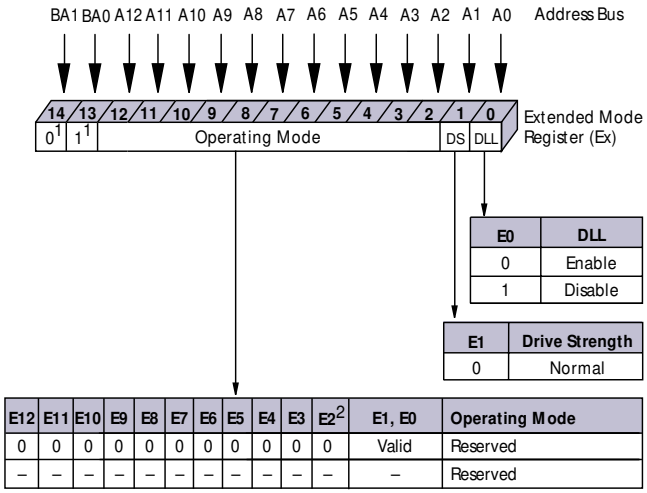
The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in the Extended Mode Register Definition Diagram. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, a DLL Reset and 200 clock cycles with CKE HIGH must occur before a READ command can be issued.

Figure 7: Extended Mode Register Definition Diagram



NOTE:

1. BA1 and BA0 (E14 and E13) must be "0, 1" to select the Extended Mode Register (vs. the base Mode Register).
2. QFC# is not supported.

Commands

Table 8, Commands Truth Table, and Table 9, DM Operation Truth Table, provide a general reference of available commands. For a more detailed description of commands and operations, refer to the 256Mb or 512Mb DDR SDRAM component data sheet.

Table 8: Commands Truth Table

CKE is HIGH for all commands shown except SELF REFRESH; all states and sequences not shown are illegal or reserved

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	1
NO OPERATION (NOP)	L	H	H	H	X	1
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	2
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	3
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	3
BURST TERMINATE	L	H	H	L	X	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	8

NOTE:

1. DESELECT and NOP are functionally interchangeable.
2. BA0–BA1 provide device bank address and A0–A12 provide row address.
3. BA0–BA1 provide device bank address; A0–A9, A11 (512MB) or A0–A9, A11, A12 (1GB) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
4. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
5. A10 LOW: BA0–BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0–BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. BA0–BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0-BA1 are reserved). A0–A12 provide the op-code to be written to the selected mode register.

Table 9: DM Operation Truth Table

Used to mask write data; provided coincident with the corresponding data

NAME (FUNCTION)	DM	DQS
WRITE Enable	L	Valid
WRITE Inhibit	H	X

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on V_{DD} Supply
Relative to V_{SS} . . . . . -1V to +3.6V
Voltage on V_{DDQ} Supply
Relative to V_{SS} . . . . . -1V to +3.6V
Voltage on V_{REF} and Inputs
Relative to V_{SS} . . . . . -1V to +3.6V
Voltage on I/O Pins
Relative to V_{SS} . . . . . -0.5V to V_{DDQ} +0.5V
Operating Temperature
T_A (ambient) . . . . . 0°C to +70°C
Storage Temperature (plastic) . . . . . -55°C to +150°C
Short Circuit Output Current 50mA

DC Electrical Characteristics and Operating Conditions

Notes: 1–5, 14; notes appear on pages 18–20; 0°C ≤ T_A ≤ +70°C

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{DD}	2.5	2.7	V	32, 36
I/O Supply Voltage		V_{DDQ}	2.5	2.7	V	32, 36, 39
I/O Reference Voltage		V_{REF}	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	6, 39
I/O Termination Voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	7, 39
Input High (Logic 1) Voltage		V_{IH}(DC)	V_{REF} + 0.15	V_{DD} + 0.3	V	25
Input Low (Logic 0) Voltage		V_{IL}(DC)	-0.3	V_{REF} - 0.15	V	25
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Command/ Address, RAS#, CAS#, WE#, S#, CKE	I_I	-5	5	µA	47
	CK, CK#		-10	10		
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	DQ, DQS	I_{OZ}	-5	5	µA	47
OUTPUT LEVELS High Current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})		I_{OH}	-16.8	–	mA	33, 34
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})		I_{OL}	16.8	–	mA	

Table 10: AC Input Operating Conditions

Notes: 1–5, 14, 48; notes appear on pages 18–20; 0°C ≤ T_A ≤ +70°C; V_{DD}, V_{DDQ} = +2.6V ±0.1V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF} + 0.310	–	V	12, 25, 35
Input Low (Logic 0) Voltage	V_{IL}(AC)	–	V_{REF} - 0.310	V	12, 25, 35
I/O Reference Voltage	V_{REF}(AC)	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	6

Table 11: IDD Specifications and Conditions – 512MB

DDR SDRAM components only

Notes: 1–5, 8, 10, 12, 48; notes appear on pages 18–20; 0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.6V ±0.1V

			MAX		
PARAMETER/CONDITION		**SYMBOL**	**-40B**	**UNITS**	**NOTES**
OPERATING CURRENT: One device bank; Active-Precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		IDD0	2,430	mA	20, 43
OPERATING CURRENT: One device bank; Active -Read Precharge; Burst = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	3,060	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = (LOW)		IDD2P	72	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^tCK = ^tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	1,080	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		IDD3P	720	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	1,260	mA	42
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); IOUT = 0mA		IDD4R	3,600	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	3,510	mA	20
AUTO REFRESH CURRENT	^tREFC = ^tRFC (MIN)	IDD5	4,680	mA	20, 45
	^tREFC = 7.8125µs	IDD5A	108	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	72	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); Address and control inputs change only during Active READ, or WRITE commands		IDD7	8,460	mA	20, 44

Table 12: IDD Specifications and Conditions – 1GB

DDR SDRAM components only

Notes: 1–5, 8, 10, 12, 48; notes appear on pages 18–20; 0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.6V ±0.1V

			MAX		
PARAMETER/CONDITION		**SYMBOL**	**-40B**	**UNITS**	**NOTES**
OPERATING CURRENT: One device bank; Active-Precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		$I_{DD}0$	2,790	mA	20, 43
OPERATING CURRENT: One device bank; Active -Read Precharge; Burst = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		$I_{DD}1$	3,330	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = (LOW)		$I_{DD}2P$	90	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^tCK = ^tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM		$I_{DD}2F$	990	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		$I_{DD}3P$	810	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		$I_{DD}3N$	1,080	mA	42
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); I_{OUT} = 0mA		$I_{DD}4R$	3,420	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		$I_{DD}4W$	3,510	mA	20
AUTO REFRESH CURRENT	^tREFC = ^tRFC (MIN)	$I_{DD}5$	6,210	mA	20, 45
	^tREFC = 7.8125µs	$I_{DD}5A$	198	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V		$I_{DD}6$	90	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); Address and control inputs change only during Active READ, or WRITE commands		$I_{DD}7$	8,100	mA	20, 44

Table 13: Capacitance

Note: 11; notes appear on pages 18–20

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	C_{IO}	4	5	pF
Input Capacitance: Command and Address, S#, CKE	C_{I1}	2.5	3.5	pF
Input Capacitance: CK, CK#	C_{I2}	2	3	pF

Table 14: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–5, 12-15, 29; notes appear on pages 18–20; 0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.6V ±0.1V

AC CHARACTERISTICS		-40B			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Access window of DQs from CK/CK#	^tAC	-0.70	+0.70	ns	
CK high-level width	^tCH	0.45	0.55	^tCK	26
CK low-level width	^tCL	0.45	0.55	^tCK	26
Clock cycle time CL = 3	^tCK (3)	5.00	7.50		40, 46
Clock cycle time CL = 2.5	^tCK (2.5)	6.00	13.00	ns	40, 46
Clock cycle time CL = 2	^tCK (2)	7.50	13.00	ns	40, 46
DQ and DM input hold time relative to DQS	^tDH	0.40		ns	23, 27
DQ and DM input setup time relative to DQS	^tDS	0.40		ns	23, 27
DQ and DM input pulse width (for each input)	^tDIPW	1.75		ns	27
Access window of DQS from CK/CK#	^tDQSCK	-0.60	+0.60	ns	
DQS input high pulse width	^tDQSH	0.35		^tCK	
DQS input low pulse width	^tDQSL	0.35		^tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access	^tDQSQ		0.40	ns	22, 23
Write command to first DQS latching transition	^tDQSS	0.72	1.28	^tCK	
DQS falling edge to CK rising - setup time	^tDSS	0.20		^tCK	
DQS falling edge from CK rising - hold time	^tDSH	0.20		^tCK	
Half clock period	^tHP	^tCH, ^tCL		ns	30
Data-out high-impedance window from CK/CK#	^tHZ		+0.70	ns	16, 37
Data-out low-impedance window from CK/CK#	^tLZ	-0.70		ns	16, 37
Address and control input hold time (fast slew rate)	^tIH_F	0.60		ns	12
Address and control input setup time (fast slew rate)	^tIS_F	0.60		ns	12
Address and control input hold time (slow slew rate)	^tIH_S	0.60		ns	12
Address and control input setup time (slow slew rate)	^tIS_S	0.60		ns	12
Address and Control input pulse width (for each input)	^tIPW	2.20		ns	
LOAD MODE REGISTER command cycle time	^tMRD	10.00		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	^tQH	^tHP - ^tQHS		ns	22, 23
Data hold skew factor	^tQHS		0.50	ns	
ACTIVE to PRECHARGE command	^tRAS	40	70,000	ns	31
ACTIVE to READ with Auto precharge command	^tRAP	15		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period	^tRC	55		ns	
AUTO REFRESH command period	^tRFC	70		ns	44

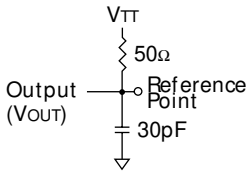
Table 14: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions (Continued)

Notes: 1–5, 12-15, 29; notes appear on pages 18–20; 0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.6V ±0.1V

AC CHARACTERISTICS		-40B			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
ACTIVE to READ or WRITE delay	^tRCD	15		ns	
PRECHARGE command period	^tRP	15		ns	
DQS read preamble	^tRPRE	0.90	1.10	^tCK	38
DQS read postamble	^tRPST	0.40	0.60	^tCK	38
ACTIVE bank a to ACTIVE bank b command	^tRRD	10		ns	
DQS write preamble	^tWPRE	0.25		^tCK	
DQS write preamble setup time	^tWPRES	0		ns	18, 19
DQS write postamble	^tWPST	0.40	0.60	^tCK	17
Write recovery time	^tWR	15		ns	
Internal WRITE to READ command delay	^tWTR	2		^tCK	
Data valid output window	na	$^tQH - ^tDQSQ$		ns	22
REFRESH to REFRESH command interval	^tREFC		70.30	µs	21
Average periodic refresh interval	^tREFI		7.81	µs	21
Terminating voltage delay to V_{DD}	^tVTD	0		ns	
Exit SELF REFRESH to non-READ command	^tXSNR	70		ns	
Exit SELF REFRESH to READ command	^tXSRD	200		^tCK	

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL}(AC)$ and $V_{IH}(AC)$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from $V_{DDQ}/2$, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} by-pass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 3 for -40B with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{DD} = +2.6V ±0.1V, V_{DDQ} = +2.6V ±0.1V, V_{REF} = V_{SS}, f = 100 MHz, T_A = 25°C, V_{OUT} (DC) = $V_{DDQ}/2$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. For slew rates < 1 V/ns and greater ≥ 0.5 V/ns. If slew rate is < 0.5 V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100mV/ns reduction in slew rate from 500mV/ns, while ^{t}IH is unaffected. If slew rate exceeds 4.5 V/ns, functionality is uncertain. For -40B, slew rates must be ≥ 0.5 V/ns.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x V_{DDQ} is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
16. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low, or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions high (above V_{IHDC} (MIN) then it must not transition low (below V_{IHDC}) prior to $^{t}DQSH$ (MIN).
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on $^{t}DQSS$.
20. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
21. The refresh period 64ms. This equates to an average refresh rate of 7.8125µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by

the DRAM controller greater than eight refresh cycles is not allowed.

22. The valid data window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct porportion to the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain.
23. Each byte lane has a corresponding DQS.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, V_{IL} (AC) or V_{IH} (AC).
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, V_{IL} (DC) or V_{IH} (DC).
26. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain. For -40B, slew rates must be ≥ 0.5 V/ns.
28. V_{DD} must not vary more than 4 percent if CKE is not active while any bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
30. ^{t}HP min is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS (MIN) can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch must be less than 1/3 of the clock and not more than +300mV or 2.9V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -200mV or 2.4V, whichever is more positive.
33. Normal Output Drive Curves:
    a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 8.
    b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 8.
    c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 9.
    d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 9.
    e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
    f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.

Figure 8: Pull-Down

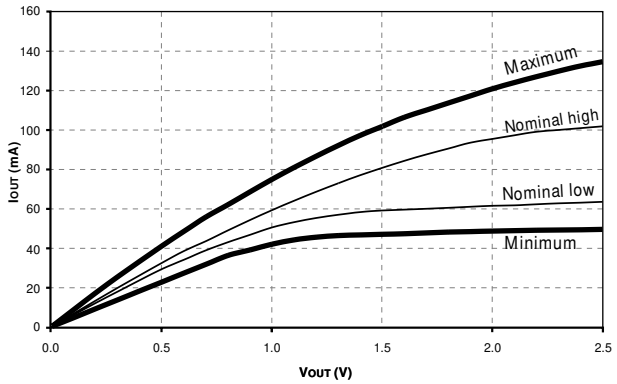
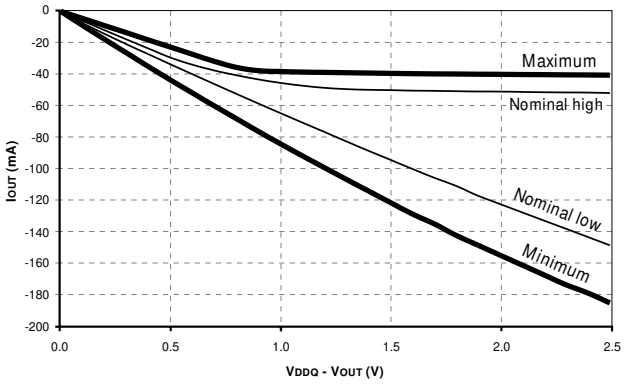


Figure 9: Pull-Up



34. The voltage levels used are derived from a minimum V_{DD} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
36. V_{DD} and $V_{DD}Q$ must track each other.
37. ^{t}HZ (MAX) will prevail over $^{t}DQSCK$ (MAX) + $^{t}RPST$ (MAX) condition. ^{t}LZ (MIN) will prevail over $^{t}DQSCK$ (MIN) + $^{t}RPRE$ (MAX) condition.
38. $^{t}RPST$ end point and $^{t}RPRE$ begin point are not referenced to a specific voltage level but specify when the device output is no longer driving ($^{t}RPST$), or begins driving ($^{t}RPRE$).
39. During initialization, $V_{DD}Q$, V_{TT}, and V_{REF} must be equal to or less than V_{DD} + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power up, even if V_{DD}/$V_{DD}Q$ are 0V, provided a minimum of 42Ω of series resistance is used between the V_{TT} supply and the input pin.
40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. For -40B, I_{DD3N} is specified to be 35mA per DDR SDRAM device at 100 MHz.
42. Random address changing and 50 percent of data changing at every transfer.
43. Random address changing and 100 percent of data changing at every transfer.
44. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
45. I_{DD2N} specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. I_{DD2Q} is similar to I_{DD2F} except I_{DD2Q} specifies the address and control inputs to remain stable. Although I_{DD2F}, I_{DD2N}, and I_{DD2Q} are similar, I_{DD2F} is "worst case."
46. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).
47. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
48. When an input signal is HIGH or LOW, it is defined as a steady state logic high or logic low.

Initialization

To ensure device operation the DRAM must be initialized as described below:

1. Simultaneously apply power to V_{DD} and $V_{DD}Q$.
2. Apply V_{REF} and then V_{TT} power.
3. Assert and hold CKE at a LVCMOS logic low.
4. Provide stable CLOCK signals.
5. Wait at least 200µs.
6. Bring CKE high and provide at least one NOP or DESELECT command. At this point the CKE input changes from a LVCMOS input to a SSTL2 input only and will remain a SSTL_2 input unless a power cycle occurs.
7. Perform a PRECHARGE ALL command.
8. Wait at least ^{t}RP time, during this time NOPs or DESELECT commands must be given.
9. Using the LMR command program the Extended Mode Register (E0 = 0 to enable the DLL and E1 = 0 for normal drive or E1 = 1 for reduced drive, E2 through En must be set to 0; where n = most significant bit).
10. Wait at least ^{t}MRD time, only NOPs or DESELECT commands are allowed.
11. Using the LMR command program the Mode Register to set operating parameters and to reset the DLL. Note at least 200 clock cycles are required between a DLL reset and any READ command.
12. Wait at least ^{t}MRD time, only NOPs or DESELECT commands are allowed.
13. Issue a PRECHARGE ALL command.
14. Wait at least ^{t}RP time, only NOPs or DESELECT commands are allowed.
15. Issue an AUTO REFRESH command (Note this may be moved prior to step 13).
16. Wait at least ^{t}RFC time, only NOPs or DESELECT commands are allowed.
17. Issue an AUTO REFRESH command (Note this may be moved prior to step 13).
18. Wait at least ^{t}RFC time, only NOPs or DESELECT commands are allowed.
19. Although not required by the Micron device, JEDEC requires a LMR command to clear the DLL bit (set M8 = 0). If a LMR command is issued the same operating parameters should be utilized as in step 11.
20. Wait at least ^{t}MRD time, only NOPs or DESELECT commands are allowed.
21. At this point the DRAM is ready for any valid command. Note 200 clock cycles are required between step 11 (DLL Reset) and any READ command.

Figure 10: Initialization Flow Diagram

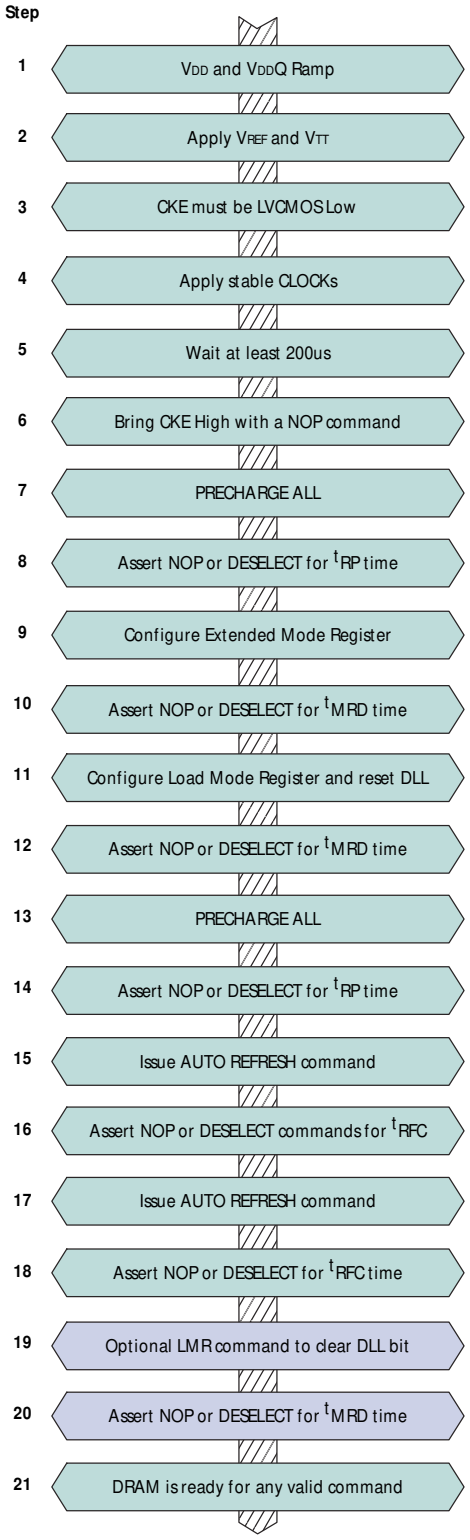


Table 15: PLL Clock Driver Timing Requirements and Switching Characteristics

Note: 1

PARAMETER	SYMBOL	0°C ≤ T_A ≤ +70°C, V_{DD} = +2.6V ±0.1V			UNITS	NOTES
		MIN	NOMINAL	MAX		
Operating Clock Frequency	^{f}CK	60	-	220	MHz	2, 3
Input Duty Cycle	^{t}DC	40	-	60	%	
Stabilization Time	$^{t}STAB$	-	-	100	ms	4
Cycle to Cycle Jitter	$^{t}JIT_{CC}$	-75	-	75	ps	
Static Phase Offset	$^{t}\varnothing$	-50	0	50	ps	5
Output Clock Skew	$^{t}SK_{O}$	-	-	100	ps	
Period Jitter	$^{t}JIT_{PER}$	-75	-	75	ps	6
Half-Period Jitter	$^{t}JIT_{HPER}$	-100	-	100	ps	6
Input Clock Slew Rate	$^{t}LS_{I}$	1.0	-	4	V/ns	
Output Clock Slew Rate	$^{t}LS_{O}$	1.0	-	2	V/ns	7

NOTE:

1. The timing and switching specifications for the PLL listed above are critical for proper operation of DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this PLL is available in JEDEC Standard JESD82.
2. The PLL must be able to handle spread spectrum induced skew.
3. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up.
5. Static Phase Offset does not include Jitter.
6. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
7. The Output Slew Rate is determined from the IBIS model:

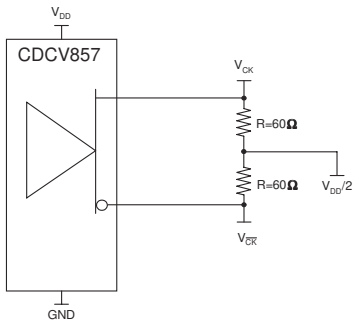


Table 16: Register Timing Requirements and Switching Characteristics

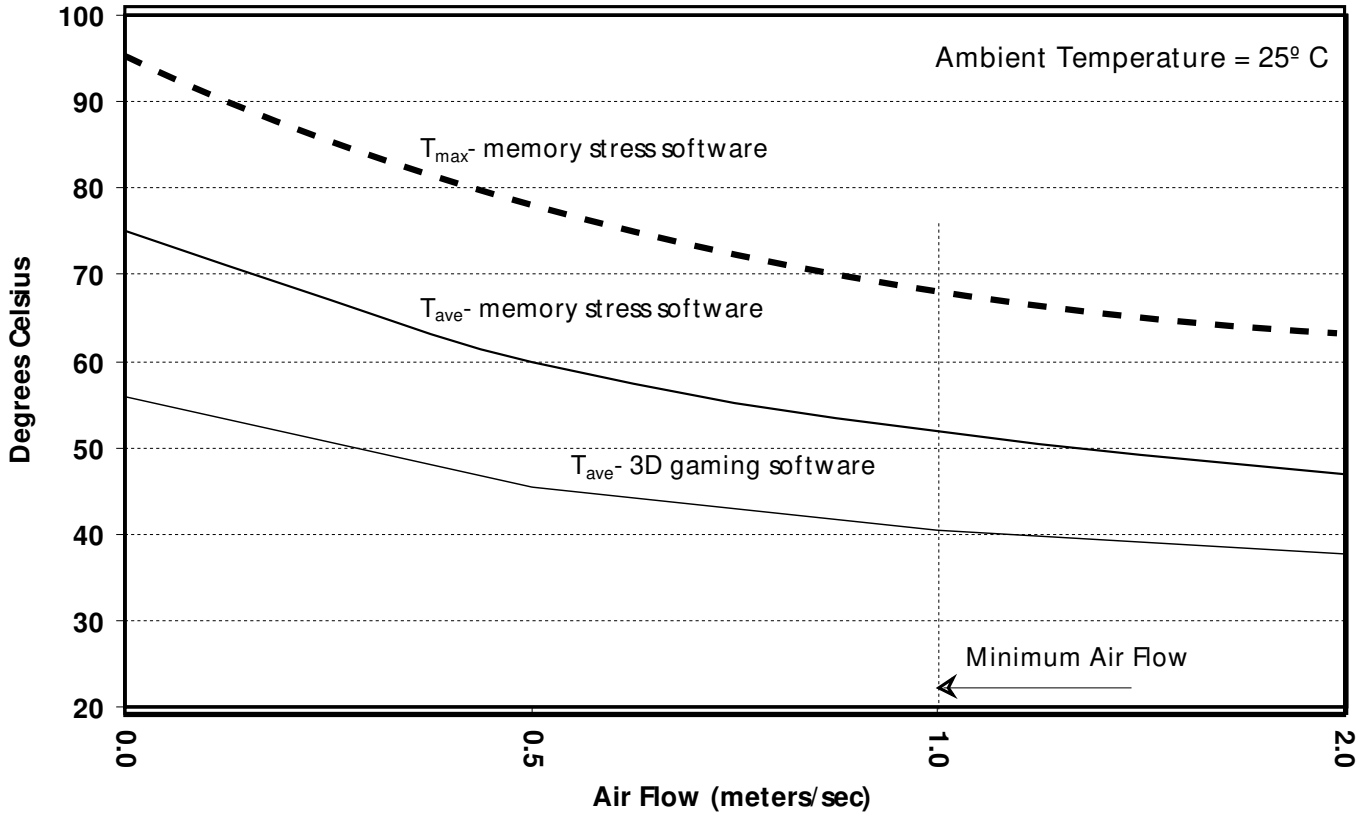
Note: 1

REGISTER	SYMBOL	PARAMERTER	CONDITION	0°C ≤ T_A ≤ +70°C VDD = +2.6V ±0.1V		UNITS	NOTES
				MIN	MAX		
SSTL (bit pattern by JESD82-3 or JESD82-4)	f_{clock}	Clock Frequency		60	220	MHz	
	t_{pd}	Clock to Output Time	30pF to GND and 50Ω to VTT	1.1	2.8	ns	
	t_{PHL}	Reset to Output Time		-	5	ns	
	t_w	Pulse Duration	CK, CK# HIGH or LOW	2.5	-	ns	
	t_{act}	Differential Inputs Active Time		-	22	ns	2
	t_{inact}	Differential Inputs Inactive Time		-	22	ns	3
	t_{su}	Setup Time, Fast Slew Rate	Data Before CK HIGH, CK# LOW	0.75	-	ns	4, 6
		Setup Time, Slow Slew Rate		0.90	-	ns	5, 6
	t_h	Hold Time, Fast Slew Rate	Data After CK HIGH, CK# LOW	0.75	-	ns	4, 6
		Hold Time, Slow Slew Rate		0.90	-	ns	5, 6

NOTE:

1. The timing and switching specifications for the register listed above are critical for proper operation of DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82.
2. Data inputs must be low a minimum time of t_{act} max, after RESET# is taken HIGH.
3. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} max, after RESET# is taken LOW.
4. For data signal input slew rate ≥ 1 V/ns.
5. For data signal input slew rate ≥ 0.5 V/ns and < 1V/ns.
6. CK, CK# signals input slew rate ≥ 1V/ns.

Figure 11: Component Case Temperature vs. Air Flow



NOTE:

1. Micron Technology, Inc. recommends a minimum air flow of 1 meter/second (~197 LFM) across all modules.
2. The component case temperature measurements shown above were obtained experimentally. The typical system to be used for experimental purposes is a dual-processor 600 MHz work station, fully loaded, with four comparable registered memory modules. Case temperatures charted represent worst-case component locations on modules installed in the internal slots of the system.
3. Temperature versus air speed data is obtained by performing experiments with the system motherboard removed from its case and mounted in a Eiffel-type low air speed wind tunnel. Peripheral devices installed on the system motherboard for testing are the processor(s) and video card, all other peripheral devices are mounted outside of the wind tunnel test chamber.
4. The memory diagnostic software used for determining worst-case component temperatures is a memory diagnostic software application developed for internal use by Micron Technology, Inc.

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 12, Data Validity, and Figure 13, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 14, Acknowledge Response From Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 12: Data Validity

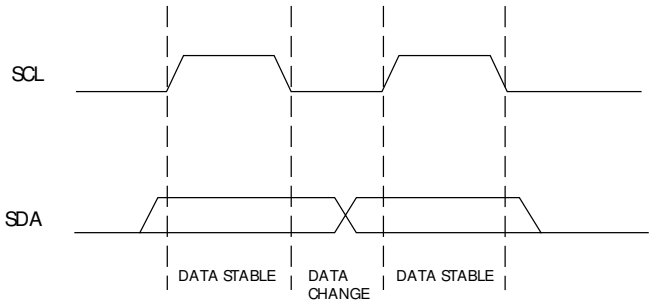


Figure 13: Definition of Start and Stop

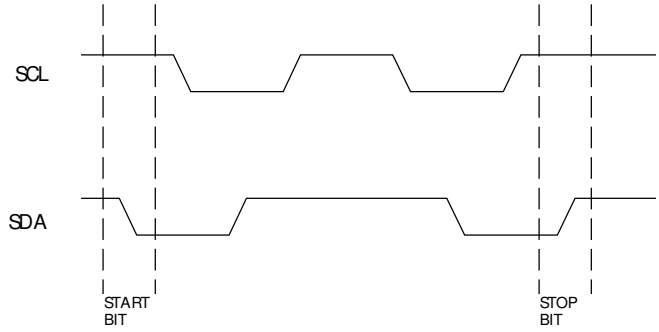


Figure 14: Acknowledge Response From Receiver